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RESEARCH ARTICLE

DESIGN AND IMPLEMENTATION OF HIGH PERFORMANCE ANALOG CMOS BASED CIRCUITS USING PSPICE: AN OVERVIEW.

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Abstract

Current mirror is the basic key element in VLSI design. To obtain high performance analog circuit application, the output impedance and accuracy are the most important parameter to determine the performance of the current mirror. A new current mirror is proposed in this paper to provide high accuracy and very high output impedance. To increase the output impedance and matching accuracy significantly a novel feedback gain is used. The new proposed current mirror also has output swing similar as the traditional two stage cascode current mirror.

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Introduction:-

Due to the better performance the current mode approach [1] - [5] is gaining interest more and more. The decreasing power supply voltage of digital micro electronics makes it suitable for mixed mode application is the reason for using current mode circuit. The current mirror is used for biasing or loading elements in analog circuit design. The most important parameter used to determine the performance of current mirror are accuracy and output impedance. It can be used to find many researches that focus on these two points. To increase the output impedance the cascode current mirror [6] and the RGC current mirror [9] is used. IAFCCM [8] was proposed to increase the accuracy. To achieve higher output impedance, multi stage cascode mirror has been used, although its suffer from low output voltage swing. The output impedance of the two stage cascode current mirror is lower than the output impedance of RGC current mirror and the accuracy of the RGC current mirror is not good enough for high precision application.

The accuracy of IAFCCM is better than RGC current mirror and the output impedance of IAFCCM is equivalent to the RGC current mirror. A new high output impedance current mirror is proposed in the paper to improve the accuracy and the output impedance of the new current mirror, it is based on the RGC circuit. To increase the output impedance and matching accuracy significantly a novel feedback gain stage is used. The new current mirror is similar to the traditional two stage cascode current mirror, so the proposed current mirror is better than that of RGC and IAFCCM.

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Description of previous circuits and the new current mirror:-
Previous current mirror circuits:-

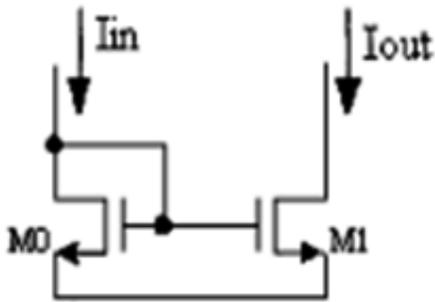


Fig. 1:- Traditional current mirror [1]

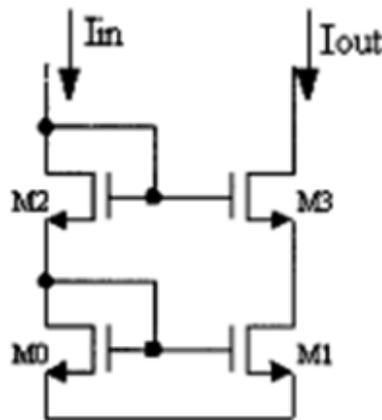


Fig 2:- Cascode current mirror [1]

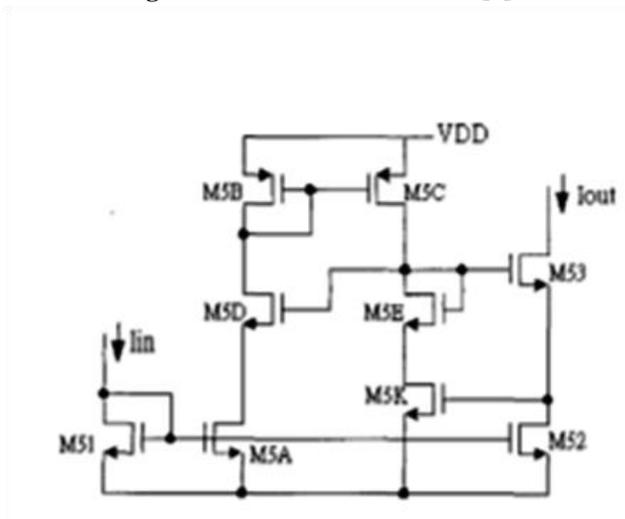


Fig 3:- IAFCM [1]

The traditional current mirror is shown in fig.1. As the traditional current mirror's output impedance is not infinite, it will influence the output current I_{out} by the variation of the output node voltage V_{ds} . It is a drawback in the analog circuits. In fig.2 the cascode current mirror is shown. It has the matching accuracy [7] problem and it was proposed to improve the output impedance. In fig.3 the IAFCM is shown. It was proposed to increase the output impedance,

output voltage swing and matching accuracy. IAFCCM improves lots of output voltage swing, but the output impedance is not high enough. Meanwhile the output node voltage influences the output current I_{out} .

The proposed new current mirror circuit:-

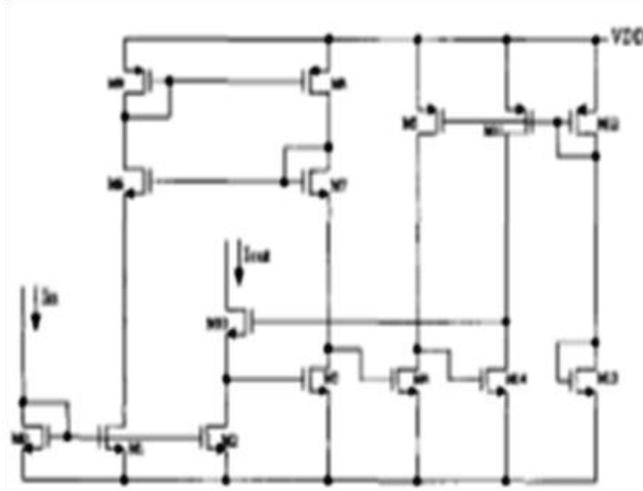


Fig 4:- The proposed current mirror [1]

The proposed new current mirror improves the new key parameters of the current mirror, the matching accuracy and output impedance. The fig.4 shows the schematic diagram of the proposed new current mirror. Here are some MOS transistors such as M0, M2, M10 are used as a two stage cascode current mirror and some MOS transistors such as M1, M6, M9, M7 and M8 are used to improve the matching accuracy of the cascode current mirror. M3, M4 and M14 are the three novel negative feedback gain stages that can increase the output impedance of the current mirror significantly.

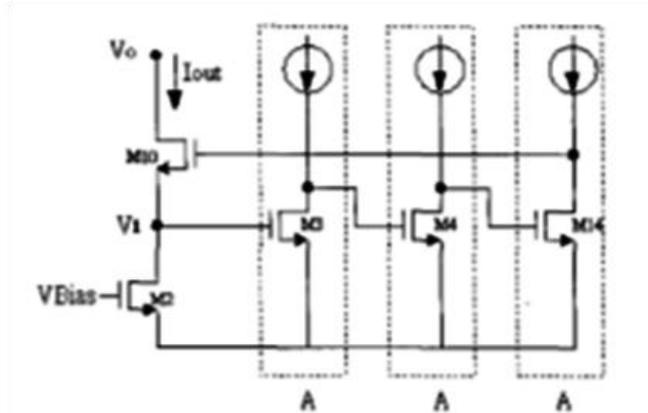


Fig 5:- The feedback circuit [1]

The feedback circuit of the current mirror is shown in fig.5 and the voltage gain of each gain stage is shown as A. The output impedance are out of the new proposed current mirror can be estimated by following.

$$V_1 = i \frac{1}{gd_2} \tag{1}$$

$$i = gm_{10} * (-|A|^3 - 1) * V_1 + gd_{10} * (V_0 - V_1) \tag{2}$$

$$\Rightarrow i * \left(1 + \frac{gm_{10}}{gd_2} |A|^3 + \frac{gm_{10}}{gd_2} + \frac{gd_{10}}{gd_2} \right) = gd_{10} * V_0$$

$$\Rightarrow \frac{V_0}{i} = \left(1 + \frac{gm_{10}}{gd_2} |A|^3 + \frac{gm_{10}}{gd_2} + \frac{gd_{10}}{gd_2} \right) \div gd_{10}$$

$$= \frac{gm_{10}}{gd_{10}} |A|^3 \frac{1}{gd_2} \quad [3]$$

$$R_0 = \frac{gm_{10}}{gd_{10}} \frac{1}{gd_2} |A|^3 \quad [4]$$

As shown in equation (4) where $A \cong \frac{gm_i}{gd_i}$ (i= 3, 4 and 14 respectively), the proposed new current mirror has much larger R_{out} than that of the IAFCCM which has output impedance $R_{out} = gm_{53} gm_{5k} \frac{1}{gd_{52}} \frac{1}{gd_{53}} \left[\frac{1}{gd_{5k}} // \frac{1}{gd_{5c}} \right]$

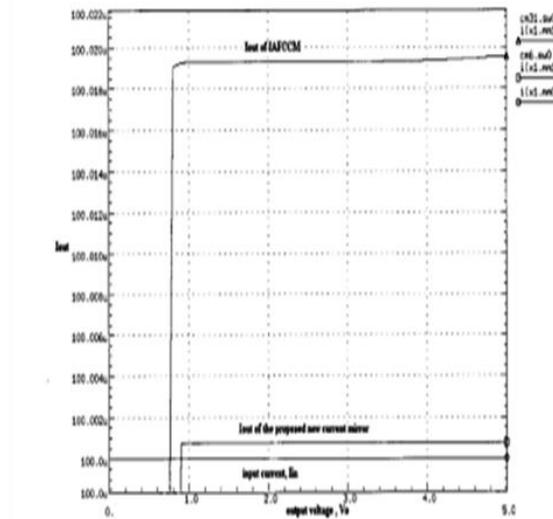


Fig 6:- The I-V curve of the simulation result [1]

In fig.5 the voltage V_1 is independent of V_0 . When V_0 and V_1 are increased then the V_{ds14} is decreased due to the three gain stages. The negative feedback signal is created by connecting V_{ds14} to the gate of M_{10} . Therefore decrease in V_{ds14} decrease the V_1 . Thus the negative feedback loop locks V_1 so that a stable I_{out} is obtained. Now the proposed new current mirror has high output impedance.

For a good current mirror another factor is the matching accuracy [10] between I_{in} and I_{out} . The MOS transistors M_6 , M_7 , M_8 and M_9 are used to match the current I_{m1} and I_{m2} in the new proposed circuit and further make $V_{Gs3} = V_{Gs1}$. From $V_{Gs1} = V_{Gs0} = V_{Ds0}$ and $V_{Gs3} = V_{Ds2}$, we can find $V_{Ds2} = V_{Ds0}$ which results $I_{in} = I_{out}$. The proposed new current mirror has better matching accuracy than the IAFCCM and it is proved by the HSPICE simulation results.

Simulation Results:-

The HSPICE simulation results are based upon 0.35µm 1P4M CMOS process which has a supply voltage of 3.3V where, $L = 1\mu m$ for all transistors except M_8 , M_9 transistors for which $L = 3\mu m$. $W = 20\mu m$ for M_0 , M_1 , M_2 , M_3 , M_6 , M_7 , M_{10} and

$W = 40\mu m$ for M_8 , M_9 to ensure $I_{out} = 100\mu A$

$W = 5\mu m$ for M_4 , M_{14}

$W = 10\mu m$ for M_5 , M_{11}

$W = 1\mu m$ for M_{12} , M_{13}

The I-V curve simulation result of the proposed new current mirror and IAFCCM is shown in fig.6. The I-V plot of the input current I_{in} is the lowest line. The top line is the I-V plot of IAFCCM, it shows that the output impedance is not that much high to avoid the influence of V_{ds} i.e. under the variation of the output voltage V_0 the I_{out} will be changed. The I-V plot of the proposed circuit is the middle line and it indicates that the output impedance of the proposed circuit is higher than IAFCCM. In fig.6 the comparison results of the accuracy is shown. The proposed circuit has a matching accuracy better than IAFCCM when the input current $I_{in} = 100\mu A$.

Table 1:- The proposed CM performance comparison with IAFCCM [1]

Issue	The proposed circuit	IAFCCM
Mirroring error $I_{in}=5\mu A$	0.016%	0.036%
Mirroring error $I_{in}=10\mu A$	0.012%	0.03%
Mirroring error $I_{in}=100\mu A$	0.001%	0.019%
Mirroring error $I_{in}=200\mu A$	0.005%	0.015%
Mirroring error $I_{in}=300\mu A$	0.012%	0.014%
Mirroring error $I_{in}=400\mu A$	0.026%	0.013%
Rout	$\propto \frac{1}{gd} \left(\frac{gm}{gd} \right)^4$	$\propto \frac{1}{gd} \left(\frac{gm}{gd} \right)^2$

Table 1 shows the comparison result between the proposed circuit and IAFCCM under various input circuit. Input current changes from $5\mu A$ to $400\mu A$. When the input current is lower than $400\mu A$ due to the MOS transistor sizes of the proposed circuit are smaller than IAFCCM. But the output impedance R_{out} of the proposed new circuit is larger than that of the IAFCCM.

Conclusion:-

A high output impedance and high accuracy current mirror is proposed and analyzed in this paper. According to the simulation results the accuracy and the output impedance of the proposed circuit is better than IAFCCM. The proposed current mirror is much suitable for using in high linearly, high output impedance current output stages and the operational amplifiers design.

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