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RESEARCH ARTICLE

Review on Double-gate MOSFETs- Scaling, Operation, Challenges and Opportunities.

Aakanksha Lakhanpal¹, Shashi B.Rana² and Ashwani K.Rana³.

1. Department of Electronics and Communication Engg. Guru Nanak Dev University, Regional Campus, Gurdaspur, Punjab India-143521.
2. Department of Electronics and Communication Engg. National Institute of Technology, Hamirpur, H.P. India-177005.

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Abstract

The expansion of VLSI industry has focused on the way to the efficiency of semiconductor devices which is dependent on the advancement in the CMOS technology. As we scale down the device, carrier mobility gets reduced due to dopant fluctuation, gate tunneling effect increases and leakage current increases. More precise structures are required to be developed for satisfying the above requirements. The double-gate Metal Oxide Semiconductor Field-Effect-Transistors control the channel region and most suited for ultra-low-voltage operation. In this paper, the review of double-gate technology, scaling challenges, double-gate structure and operation its challenges and opportunities have been discussed.

Corresponding Author*Aakanksha Lakhanpal.**

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Introduction:-

The future of electronics itself is the future of integrated circuits and electronics. Over the past thirty years, the growth of microelectronics, information sharing, signal processing has strongly dependent on very large scale integrated circuit industry. It all started with the insight of Lilienfeld of Insulated Gate Field Effect Transistor in 1925 which bore the potential to substitute the vacuum tube technology with small sized semiconductor transistor technology [1]. The first practical exhibition took place in 1960 by Kahng and Atilla in the form of the Silicon-based Metal Oxide Semiconductor Field Effect Transistor (MOSFET) [2]. In 1958, Jack Kilby at Texas Instruments conceived the idea of the Integrated Circuits(IC) and Robert Noyce from the Fairchild Corp. fabricated the first IC. The various advantages of integrated circuits have led to the development in many areas of science. In telephone communications, the integrated circuits has performed data processing and switching telephone circuits. Computer memories have been distributed throughout the machine instead of being concentrated in the central unit. These memories have been built with lower costs and with much faster speed. According to Moore's Law, the number of transistors per chip in a dense integrated circuit has doubled approximately every two years [3]. Due to this, packing density of transistors per unit area is increasing in the VLSI microelectronic industries. This has been possible due to the comprehensive scaling, also known as miniaturization. The advantages of scaling are the speed improvements, increased packing density. The increased packing density has resulted in a chip with the same functionality in a lesser area, or chips with more functionality in the identical area. Also, the smaller ICs allow more chips per wafer, decreasing the price per chip. The major device dimensions are the channel length, channel width and the oxide thickness. MOSFETs reduction of the transistor dimensions does not necessarily transform to higher chip speed because the delay due to interconnections is more significant. The reduction of channel length has led to the short channel effects. The shrinking of MOSFET device size has led to the degradation due to short channel effects in bulk device geometries. Integration of billions of transistors on a chip has been realizable due to the possibility to pattern every smaller feature on silicon through optical lithography.

Scaling challenges:-

A. Scaling Problems:-

- Higher subthreshold conduction:-

As MOSFET geometries minimize, the voltage that can be applied to the gate must be reduced to preserve reliability. To preserve performance, the threshold voltage has to be reduced as well. As threshold voltage is reduced, the transistor cannot be turn-on from complete turn-off with the less voltage swing available. Subthreshold leakage which was mistreated in the past, now can consume upwards of half of the total power consumption of recent high-performance VLSI chips [4, 5, 6].

- Increased gate-oxide leakage:-

The gate oxide, which acts as insulator between the gate and channel, should be prepared as thin as possible to enhance the channel conductivity and the performance when the transistor is on and to lessen subthreshold leakage when the transistor is off.

- Increased junction leakage:-

To make devices smaller, junction design has become more complex, forcing to higher doping levels, shallower junctions, halo doping all to reduce drain induced barrier lowering [7,8].

- Interconnect capacitance

Conventionally, switching time was roughly proportional to the gate capacitance of MOSFETs. On the other hand, with transistors becoming smaller and number of transistors being located on the chip, interconnect capacitance is becoming a great percentage of capacitance [9, 10]. Signals have to pass through the interconnection, which leads to amplified delay and degrade performances.

- Heat production:-

The increasing density of MOSFETs on integrated circuit makes difficult of localized heat generation that can damage the circuit operation. Circuits work more slowly at high temperatures. Cooling devices and heat sinks are now necessary for many integrated circuits including microprocessors.

B. Challenges to Scaling:-

Modern ICs are computer-simulated with the aim of obtaining working circuits from the very first manufacturing lot. As devices are miniaturized, the difficulty of the processing makes it hard to predict exactly what the ultimate device look like, and modelling of physical processes becomes more challenging as well. To minimize the difficulties of small size bulk MOSFETs, several alternative device structures has been discovered, by which the technology can be further scaled down with an improved performance. These are, double gate (DG) MOSFETs, Strained MOSFETs, gate all around (GAA) MOSFETs. Double gate MOSFET is one of the improved device structures for reducing short channel effects.

C. Solution to Scaling:-

- Channel Engineering Techniques:-

a) Halo-Doping:-

To overcome the SCEs, various channel engineering like double-halo (DH) and single-halo (SH) have been proposed. In the subthreshold region, the halo doping is found to improve the device performance parameters for analog applications. Halo doping led to a higher drive current in the saturation region. The halo device pinch-off region occurs in the halo implant region, since that region is closest to the drain and has a threshold voltage higher than the uniformly doped region.

b) Strain:-

To maintain a lower junction electric field in the channel and non- overlap of the source and drain depletion in the channel, doping becomes imperative. But mobility degradation due to the impurity scattering comes into play with higher amount of channel doping. Also, threshold voltage variations take place due to random dopant fluctuations inside the channel. The mobility of the charge carriers is enhanced through a concept called strain technology. Strain results in a modified lattice constant of the material; second a modified energy band structure to trap carriers through well formation and finally an enhanced mobility.

- Gate Engineering Techniques:-

- a) High-k dielectric:-

High-k/metal gates were introduced into mass production in 2007 by Intel in the 45nm CMOS technology generation. This is the first time that traditional oxides have been replaced in gate stacks, to enable continuous scaling of the EOT.

- b) Metal Gate:-

Initially, poly-Si/ high-k combination gate stack was considered as a route to improving gate leakage. Theoretical studies show mobility degradation compared to the use of metal gates. Depending on the gate dielectric, the work function varies due to differing band alignments.

- c) Multi-Material Gate:-

One of the prominent means to get rid of hot carrier effect is using cascaded gate structure consisting of two or more metals of different work functions. This structure is known as Double-Material-Gate (DMG) structure as proposed in 1999 by Long et.al [11] or Triple-Material-Gate (TMG) in 2008 proposed by Razavi et.al [12]. The metal gates are so cascaded that the gate near the drain is a metal with lower work function and source side metal is of higher work function. As a result of this, the electron velocity and the lateral electric field along the channel increase sharply at the interface of the two gate material which results in the gate transport efficiency.

- d) Multiple Gate:-

A potential candidate to continue the MOSFET scaling further is the fully-depleted silicon-on-insulator (FDSOI) MOSFET. Research of the FD SOI MOSFETs reveals that this transistor possesses higher transconductance, lower threshold voltage roll-off and steeper subthreshold slope compare to the bulk MOSFET. In the FDSOI MOSFETs, the front gate parasitic junction capacitance reduces resulting in higher switching speeds. The presence of buried oxide further removes drawbacks like leakage current, threshold voltage roll off, higher sub-threshold slope and body effect. Due to the ultra thin source and drain regions, FD SOI MOSFETs possess large series resistance which leads to the poor current drive capability of the device despite having excellent short-channel characteristics. To prevent the electric field lines from the drain on the channel region, special gate structures can be used. Such multiple gate devices include double-gate transistors, triple-gate devices such as quantum wire, the FinFET and quadruple-gate devices such as the gate-all-around device, the DELTA transistor and vertical pillar MOSFETs [13]. In fully depleted SOI device, most of the field lines propagate through the buried oxide before reaching the channel region. Short-channel effects can be reduced in FDSOI MOSFETs by using a thin buried oxide and an underlying ground plane. This approach has the inconvenience of increased junction capacitance and body effect. The more efficient device configuration is obtained by using double-gate transistor structure. Multi-gate MOSFETs realized on thin films are the most promising devices for the ultimate integration of MOS structures due to the volume inversion in the thin layer, leading to an increase of the number and the mobility of electrons and holes as well as drive current, optimum subthreshold swing and the best control of short channel effects and off-state current, which is the main challenge for future nanodevices due to the power consumption crisis and the need to develop sustainable ICs. The double-gate (DG) MOSFET is one of the promising architectures for scaling CMOS devices down to nanometer size, since they allow a significant reduction of the short-channel effects (SCEs) such as threshold voltage roll-off, drain-induced barrier lowering (DIBL), and subthreshold degradation compared to planar single-gate MOSFETs. In DG-MOSFETs, the ultrathin channel material is preferred to be undoped. The absence of dopant atoms in the channel material eliminates adverse effects such as mobility degradation.

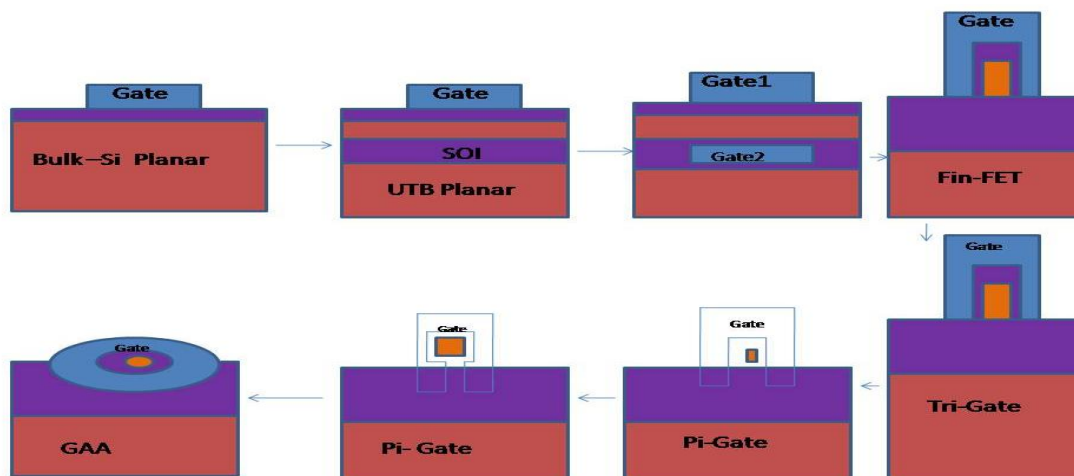


Fig.1. Progress of the MOSFET Technology through multiple-gates [4].

Device structure & operation:-

DG-MOSFET uses two gates which are placed in symmetry covering the channel which are present at the opposite of each other. The channel is formed near the gate. It has two gates simultaneously controlling the charge in the thin silicon body layer, allowing for the two channels for current flow. In this device, both the gates are connected to the same potential and they have same dimensions so it is known as symmetric DG-MOSFET[14]. The presence of double gate reduces the impact of the drain field line over the channel potential distribution that lowers the SCEs. Leakage current is reduced because the substrate is replaced by the second gate. When both gates have the same work function and a single input voltage is applied to both gates, the double-gate is said to be symmetric.

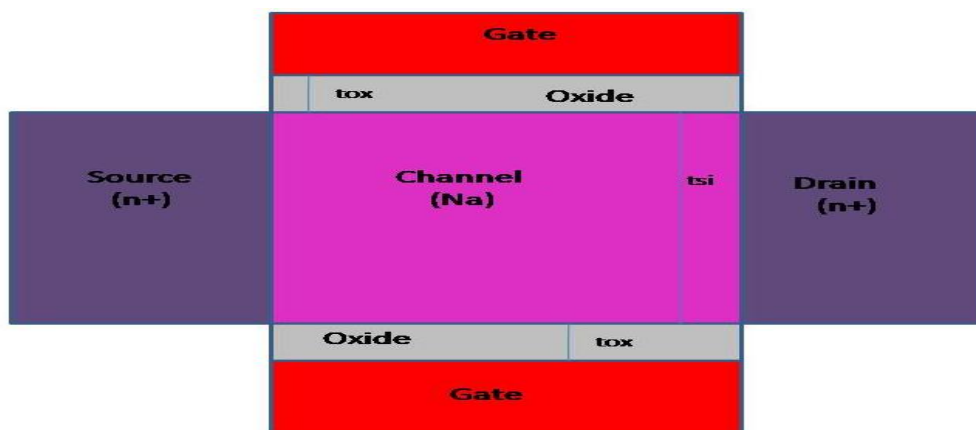


Fig.2. Cross-sectional view of double-gate MOSFET structure.

D. DG-MOSFET Operation:-

The device can be operated in several ways [15]. The voltage applied on the gate terminals controls the electric field, determining the amount of current flow through the channel. The most common mode of operation is to switch both gates simultaneously. Another mode is to switch only one gate and apply a bias to the second gate.

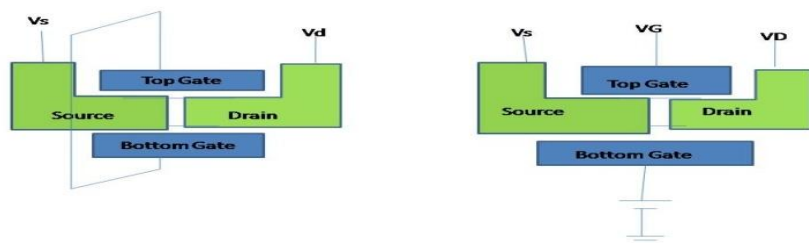


Fig.3.Operation of double gate MOSFET with ground plane and back gate mode.

CHALLENGES OF DG-mosfets:-

E. Fabrication:-

The fabrication of the DG-MOSFET is difficult. There are three possible orientations for fabricating the double-gate MOSFET. As the film thickness on the plane of the wafer has the best uniformity and controllability so the planar structure has the advantage of good channel thickness uniformity [16]. Also, the fabrication of the back gate in planar structure is not straightforward. Further, for device wiring, accessing of bottom gate from the top gate is difficult which has its negative impact on device density. So, the non-planar structure comes into existence with ease of formation of gates on crystalline channels and access of bottom gate. But non-planar structures have worse uniformity than planar structures as the channel thickness is described by the lithography and patterning techniques.

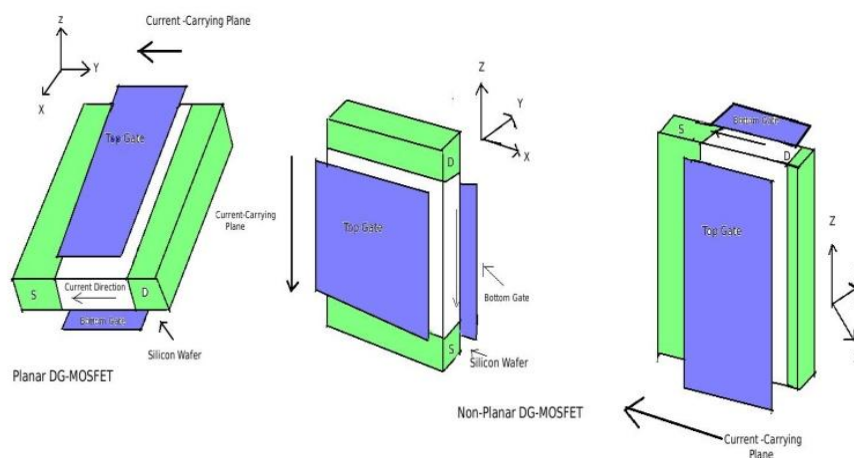


Fig.4.Three possible orientations for DG-MOSFETs

F. Threshold Voltage Adjustment:-

There is a need of different threshold voltages for different applications. To support high performance logic, data communications and low power, the double-gate device technology must be able to offer multiple -threshold voltages. Channel doping, work-function engineering and back-gate bias is the possible solutions for threshold voltage adjustments. Because of doping fluctuations and mobility degradation, the channel doping is not desirable for future MOSFET scaling.

Opportunities

A double-gate device technology offers opportunity for performance improvement for low-power applications. Figure shows the I_d - V_{gs} characteristics of FDSOI MOSFET and the double-gate devices. Because of the better sub-threshold slope in double-gate device, the saturated current could be more than two times higher than that in a single-gate device.

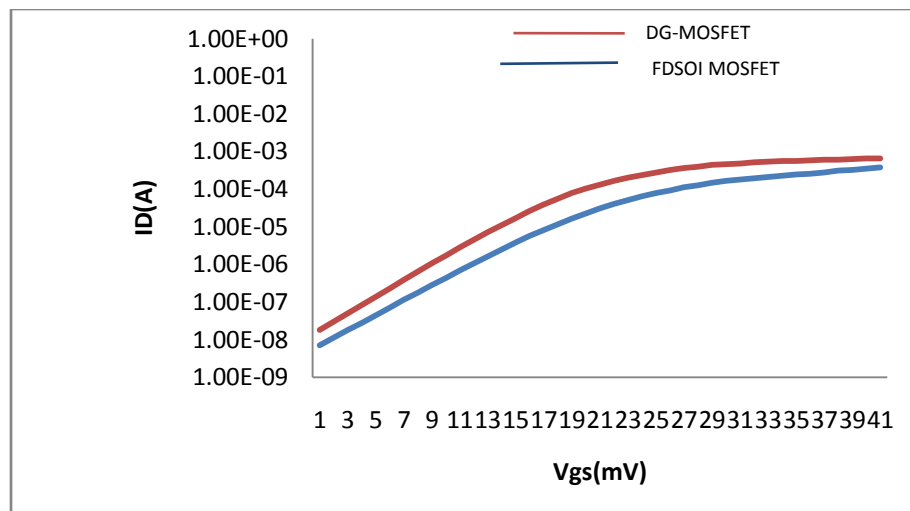


Fig.5. Id-V_{gs} Curve for DG-MOSFET and FDSOI MOSFET

Conclusions:-

The review of recent advancement of scaling, its issues and double-gate device technology has been done in this work. Various issues to the scaling and solution to scaling like channel engineering and gate engineering techniques have been discussed. Also, the double-gate structure and its operation with various challenges to double-gate device technology have been investigated.

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