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RESEARCH ARTICLE

Design and Construction of a Simple Microcontroller Based Conference Electronic Voting Machine with Digital Display

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Abstract

This paper presents the design details and implementation of a simple electronic voting machine with a seven segment digital display. The design is based on around the (AT89C52) microcontroller. The work gives all the design details the building blocks of the whole system. The concept design of this prototype is for two voters and an arbitrator. The arbitrator grants permission for voting and each voter can only vote once and protects the identity of the voter to make the process unbiased and fair. The simplicity of this prototype as presented can easily be replicated to cover multiple voters with little overhead in terms of cost.

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Introduction

Voting is an important process usually employed to reveal the opinion of a group on an issue that is under consideration. The fact that greater efficiency, better scalability, speed, lower cost, and convenience, can be delivered by electronic devices, has made the process shift from manual process to electronics and automated process. Electronic voting means the use of some electronic means in voting in order to ensure security, reliability, guarantee and transparency (Villafiorita, Weldemariam et al. 2009; Balzarotti, Banks et al. 2010). Today a lot of electronic means of voting are employed in shareholder meetings and it's like.

At conferences where crucial issues are deliberated upon often, they end up in deadlock which results in disagreement. Voting is the usual way of sampling the Representatives opinion on the motion under consideration. The manner in which voting "for" or "against" is being done especially in this country is not encouraging. To decide who carries the day, those "for" will move to one end of the building and those "against" to the other end conversely, those

"for" will rise up their hands to be counted, then those "against" will also put up their hands to be counted. The group with the highest number of people carries the day. However, going through these processes, the following were observed:

- The voting in most cases is not a fair one because people voted dependently (godfather) i.e. to please others
- Time wasting

To avoid these, this project is aimed to design and construct a voting machine or system. With this system, Representatives at a conference can vote electronically and independently within the shortest possible time.

The electronic voting system is a system that can be used to simultaneously provide the number of "yes" and the number of "no" votes. For example, this type of system can be used where a group of people are assembled and there is a need for immediately determining opinions (for or against) making decisions, or voting on certain issues or on other matters.

The aim of this paper is to design and implement a microcontroller based electronic voting system with

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working software for efficiency. The construction was carried out in three stages. The first module was the construction of the power unit on the breadboard and then tested; the second module was the construction of the logic unit using the microcontroller on the breadboard and tested while the third module was the construction of the display unit.

The limitations of the system are as follows; our prototype can only be used by two representatives which are referred to as voters and one arbitrator. However, its design makes it easy to extend its usage to multiple users. Also, convenience of wireless technology is lacking and no password security was implemented in the software.

The rest of the paper presents a review of the sun-tracking technologies, specific design methodologies and software/system operation. The paper concludes with a discussion of design results and future work.

2. Review of Relevant Literature

(Chaum 2003) addressed the concepts of untraceable electronic mail and digital pseudonyms, which can apply for electronic voting for anonymity. In the recent years, voting equipment which were widely adopted may be divided into five types (Mercuri 2002): Paper-based voting, Optical voting machine, Lever voting machine, Punch card and direct recording electronic voting machine. Although most electronic voting devices are usually sourced out and customized (McClure and Lohry 2001), various open source E-voting systems are also available (Chaum 2003; Keller, Dechert et al. 2005). It is important to note that some recent studies have shown that most of the electronic voting systems being used today are fatally defective (Kohno, Stubblefield et al. 2004; Proebstel, Riddle et al. 2007; Balzarotti, Banks et al. 2010) and that their quality does not match the importance of the task that they are supposed to carry out. In (Qadah and Taha 2007) design and implementation requirements were presented while (Kumar and Begum 2011) presented a fingerprint based system. Although these designs are quite efficient the intensity involved and complexity of the overall system is an issue which our design answers, the simplicity of our design is the main novelty we present.

3. Materials and Methods

The electronic voting system is a closed loop control system that covers the fields of electronics engineering. This system is used to register the votes of individuals either for or against an issue. The components of the electronic system consist of a

Microcontroller logic circuitry, a Power Unit, a Transformer and sets of seven segment displays. These components are grouped into the following units and illustrated in the block diagram below in figure 1:

- Power Unit.
- Input Unit.
- Microcontroller Unit.
- Display Unit.

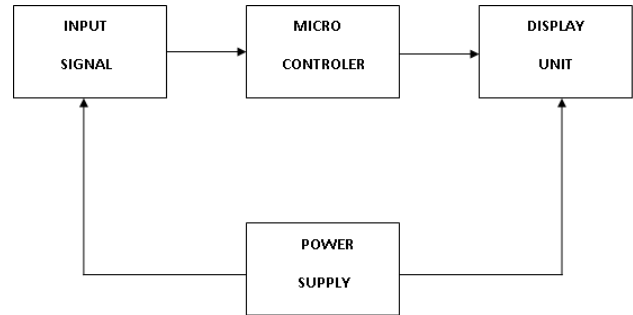
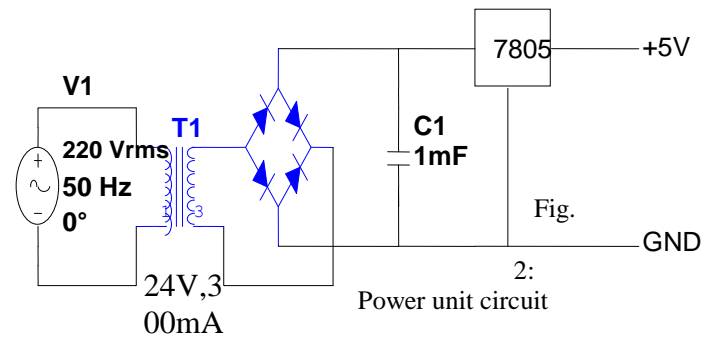


Fig. 1 Block diagram of the system

3.1 Power unit:

This consists of a 220-24V 300mA Step down Transformer with a rectified output of 24V. This rectified output is smoothed by a 1034µF capacitor, the 7805 voltage regulator converts the 24V rectified filtered voltage to a voltage level of +5V which is used by the microcontroller and other units of the system. Circuit is presented in figure 2.



For safe operation, the peak inverse rating of the rectifiers must be greater than V_{peak} , therefore a 220V/35V transformer was chosen.

Calculations involved:

Therefore, $V_p = \sqrt{2} \times V_{rms}$ (1)

Where $V_{rms} = 24V$ since the transformer of 220V/24V was used.

Rectification is a process of changing AC to DC. Diodes are commonly used as rectifiers in power supplies. The 24V AC stepped down from the transformer passes through the full wave bridge rectifier circuit. The aim is to convert it from AC to DC. After the full wave rectification, the signal still contains some AC components.

After rectification, the 24 AC reduces by 1.4V. This is so because for full wave rectification two diodes conduct and two diodes block and since the forward breakdown voltage for a diode is 0.7V, the two voltages add up to give 1.4V. Thus the voltage after full wave rectification is

$$\text{Voltage after rectification} = 24V - (0.7 \times 2) = 24 - 1.4 = 22.6V \text{ DC}$$

It is 22.6V that goes to the filtering circuit.

The frequency of the full wave signal is double the input frequency. A full wave input has twice as many cycles as the sine wave input has. The full wave rectifier inverts each negative half cycle so that we can get double the number of positive half cycles. The effect is to double the frequency.

Therefore the output frequency of the full wave rectifier is:

$$f_{\text{out}} = 2f_{\text{in}} \text{ (i.e twice the input frequency)} \quad (2)$$

This implies that,

$$dt = 1/2f_{\text{in}} = 1/(2 \times 50) = 0.01 \text{ sec}$$

This is on the safer side as the capacitor begins charging up in less than half a cycle. The maximum current that can be drawn by the main circuit is determined by the voltage regulator following the filtering capacitor, the 7805.

Filtering Circuit:

A filter is used to reduce the amount of AC ripple, thus providing a relatively pure form of DC. The main function of the filter is to minimize the ripple content in the rectifier output. An electrolytic capacitor connected in parallel with the output of the rectifier circuit is used as a filter.

Calculation

The main voltage of 220V is stepped down by a 220V/24V transformer. It is then rectified by full wave bridge diode rectifier. The waveform at this stage has no negative component but a lot of ripples. Smoothing capacitors are needed to reduce the

ripples to an acceptable level. The resulting ripple voltage (dv) can be calculated as follows:

If the load current stays constant, as it will for small ripples, then

$$I = Cdv/dt \quad (3)$$

The standard 7800 series can produce output current in excess of 1A when used with adequate heat sink. Therefore, it can supply a maximum of 1A. This current will be drawn from the supply. Thus, $I_{\text{load}} = 1A$ (maximum). The value of C can then be calculated from:

$$C = Idt/dv \quad (4)$$

But generally dv which is the ripple voltage is chosen to be 30% of V_P , where V_P is the peak voltage.

For bridge rectifier, $V_{p(\text{out})} = V_{p(\text{in})} - 1.4V$, since 0.7V dropped across a diode whenever it conducts.

Only two diodes will conduct at a time.

$$\text{Therefore, } V_{p(\text{out})} = 24\sqrt{2} - 1.4 = 32.54V$$

$$dv = (30/100) * 32.54 = 9.76V$$

$$\text{Therefore, } C = (1 * 0.01)/9.76 = 1.034 \times 10^{-3} \text{ F}$$

$$\text{Thus, } C = 1034\mu\text{F}$$

So the commercial value of 1000 μF , 35V was used in order to reduce the ripple to the nearest minimum.

$$f_{\text{out}} = 2f_{\text{in}} \text{ (i.e twice the input frequency)}$$

$$dt = 1/2f_{\text{in}} = 1/(2 \times 50) = 0.01 \text{ sec}$$

Power Regulating Circuit:

A voltage regulator is an electrical regulator designed to automatically maintain a constant voltage level. The entire work will comprise mainly a single microcontroller IC, two 4026 decade counters, two seven segment displays, three light emitting diodes (LEDs), all of which are low power consuming devices that require a 5V d.c voltage for optimum operation. A LM7805 voltage regulator was used to achieve a 5V output voltage. For proper operation of the LM7805 regulator, the input voltage must be at least 2V above the output voltage. Hence, a 9V

transistor radio battery was utilized. The connection is as shown in fig 3. below.

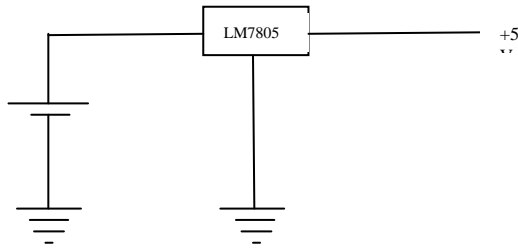


Fig 3. Design of power supply unit

Calculation:

Then the expected ripple voltage using this value of 1000 μ F capacitor is calculated as follows

$$dv = (1 * 0.01) / (1000 \times 10^{-6}) = 10.00V \quad (5)$$

This means that the output waveform goes from a peak value of 32.54V to $(32.54 - 10.00)V = 22.54V$. It may be noted that the input voltage to the IC regulator must be at least 2V above the output voltage. This is required in order to maintain regulation.

Therefore, peak value of 32.54V to 22.54V is acceptable since the output voltage is 5V. The ripple is neglected by the 7805 regulator. The average voltage going to the 7805 is calculated by:

$$V_p - 0.5dv = 32.54 - (0.5 \times 10.00) \\ = 27.54V$$

The output from the 7805 is 5V at maximum current output of 1A. The output remains constant in spite of input voltage variation.

3.2 AT89C52 Microcontroller

Initially all the pins of the microcontroller are high i.e. they are internally pulled to VCC through a high value resistor (the resistor is internally fixed inside the microcontroller by the manufacturer). Switches S1, S2, S3, S4, S5, S6 and S7 are all connecting their pins to the ground so that if any of the switches is closed, the pin's logic level is changed from high to low. The AT89C52 sends a high or low signal to these pins.

Pin 1: S1 which is connected to P1.0 of the microcontroller is the permission/result switch on the senate president's button pad. The microcontroller was programmed so that if this switch is closed, it will give access to the other senators to vote and it will also be used as the result button.

Pin 2: S2 which is connected to P1.1 of the microcontroller is the NO switch on the senate President's button pad. The microcontroller was programmed so that if this switch is closed, a signal is sent to the 4026 to increment the NO register and display the result.

Pin 3: S3 which is connected to P1.2 of the microcontroller is the YES switch on the senate President's button pad. The microcontroller was programmed so that if this switch is closed, a signal is sent to the 4026 to increment the YES register and displays the result.

Pin 4: A BC639 transistor (npn) is connected to P1.3 of the microcontroller. The npn transistor requires its base to be connected to Vcc for proper saturation and conduction of the collector- emitter path. Thus the LED comes on when the base is high. It does not conduct on when the base is low. The microcontroller was programmed to send a high and low signal when required. When LED is ON, permission has not been given so no senator can vote. Senator can only vote if it goes OFF.

Pin 5: S4 which is connected to P1.4 of the microcontroller is the NO switch on the first senator's button pad. The microcontroller was programmed so that if this switch is closed, a signal is sent to the 4026 to increment the NO register and display the result.

Pin 6: S5 which is connected to P1.5 of the microcontroller is the YES switch on the second senator's button pad. The microcontroller was programmed so that if this switch is closed, a signal is sent to the 4026 to increment the YES register and displays the result.

Pin 7: A BC638 transistor (pnp) is connected to P1.6 of the microcontroller. The pnp transistor requires its base to be cleared for proper conduction of the collector-emitter path. Thus the LED comes on when the base is low. It does not conduct on when the base is high. The microcontroller was programmed to send a high and low signal when required. When LED is ON, the first senator has successfully cast his vote.

Pin 9: This is the RESET pin the reset of the microcontroller is activated by pulling the RESET pin to Vcc for at least 2ms and pull it afterwards to the ground. The capacitor-resistor configuration connected to this pin takes care of this effect. On power up of the circuit, the capacitor charges on the time, $t = 1.1RC$ which is greater than 2ms. When it is

fully charged, it stops conduction and then the pin is pulled to the ground through the 10kΩ resistor.

Pin 10: S6 which is connected to P3.0 of the microcontroller is the NO switch on the second senator's button pad. The microcontroller was programmed so that if this switch is closed, a signal is sent to the 4026 to increment the NO register and display the result.

Pin 11: S7 which is connected to P3.1 of the microcontroller is the YES switch on the second senator's button pad. The microcontroller was programmed so that if this switch is closed, a signal is sent to the 4026 to increment the YES register and displays the result.

Pin 18 and Pin 19: The crystal oscillator is connected to this pin. It synchronizes the operation of the microcontroller.

Pin 20: Connected to ground.

Pin 21: Pin 3 of the 4026 IC (display enable) is connected to P2.0 of the microcontroller. The pin shows and hides the count result of the 4026 IC. When the pin is cleared, the display result is hidden but comes on when the pin is set. This is why the pin's logic level is controlled by the microcontroller.

Pin 22: Pin 1 of the first 4026 IC (count) is connected to P2.1 of the microcontroller. A count is successfully carried out by changing the logic level of the pin from high to low for at least 5ms and then taking it to high again. This pin counts the number of NO votes.

Pin 23: Pin 15 of the 4026 IC (RESET) is connected to P2.2 of the microcontroller. The reset pin of the 4026 IC is controlled through a transistor by the microcontroller. The reset pin is connected through 1kΩ to the ground and remains in the state as long as the microcontroller is not conducting. Anytime it is required to reset the 4026, the base of the pnp transistor is cleared to allow conduction for at least 5ms thereby pulling the pin to Vcc for thT time interval and then setting it back to allow normal operation.

Pin 27: Pin 1 (count) of the second 4026 IC is connected to P2.6 of the microcontroller to count the number of NO votes.

Pin 40: it is connected to Vcc

Note: Pin 3 (Display Enable) of the two 4026 counters are looped together. Also, pin 15 (RESET) of the two counters are looped together.

3.3 Design of Output Indicator:

There are three output indicators (LEDs), one for the senators and the other two for each senator. The first LED is powered by BC639 (npn) transistor. The figure 4 below shows how the BC639 transistor is configured.

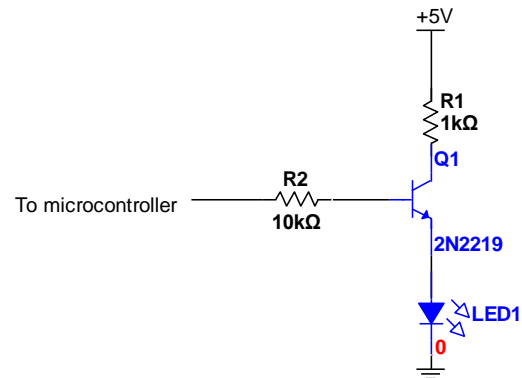


Fig.4: BC639 Configuration

For proper brightness of LED, it must sink a minimum current of 4mA, but maximum current should not exceed 10mA.

This maximum collector current, $I_{c(max)} = 10\text{mA}$.

The minimum value of base current,

$$I_B = I_{c(max)} / h_{FE} \quad (6)$$

$$= 10\text{mA} / 89 = 0.112\text{mA}$$

The maximum value of base resistance, R_B is

$$R_B = (V_{CC} - V_{BE}) / I_B \quad (7)$$

$$= (5 - 0.7) / 0.112$$

$$= 38.39\text{K}\Omega$$

A value of 10 KΩ was used to ensure saturation.

$$R_{lim(min)} = (V_{CC} - V_{BE}) / I_{c(max)} \quad (8)$$

$$= (5 - 0.7) / 10\text{mA}$$

$$= 0.43\text{K}\Omega$$

$$R_{lim(max)} = V_{CC} - V_{BE} \quad (9)$$

$$= (5 - 0.7) / 4\text{mA}$$

$$= 1.08\text{K}\Omega$$

Thus, a value of 1 KΩ was used i.e. $R_{lim} = 1\text{K}\Omega$

The other two senators used a BC638 (pnp) transistor. Both configurations are described using the figure 5 below.

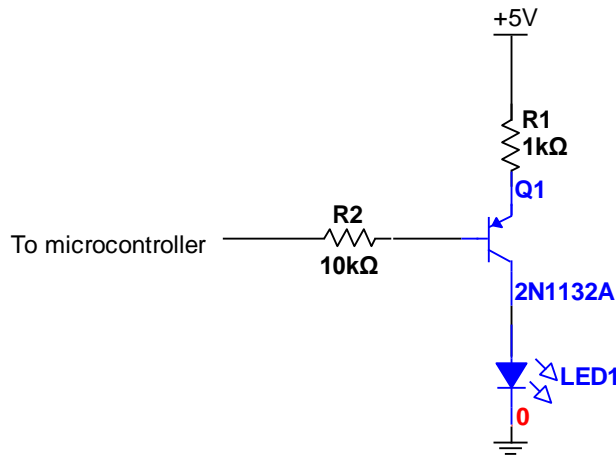


Fig 5: BC638 Configuration

3.4 The 7- Segment Display:

A seven segment display, as its name indicates, is composed of seven elements. Individually on or off, they can be combined to produce simplified representations of the Arabic numerals. The figure below shows a common display format composed of seven elements or segments. Energizing certain combinations of these segments can cause each of the ten decimal digits to be displayed. To produce a 1, segments b and c are energized; to produce a 2, segments a, b, g, e and d are energized; to produce a 3, segments a, b, g, c and d is energized; to produce a 4, segments f, g, b and c is energized; to produce a 5, segments a, f, g, c and d is energized; to produce a 6, segments a, f, g, e, c and d is energized; to produce a 7, segments a, b and c is energized; to produce an 8, segments a, b, c, d, e, f and g is energized; to produce a 9, segments a, b, f, g, c and d is energized.

LED displays: one type of seven segment display consists of light emitting diodes (LED) arranged in the figure as shown below. Each LED emits light when there is current through it. Because of the external source of current attached to the common anode, the common anode will be used for this project. The figure 6 shows a seven segment display.

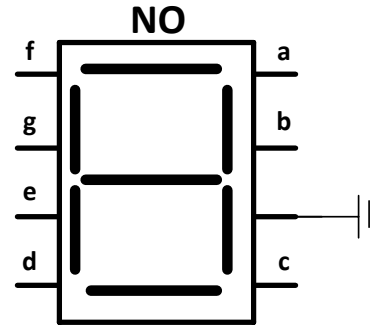


Fig 6: Seven Segment display

3.5 4026 Counter (Decade Counter):

The 4026 IC is a 16-pin CMOS seven-segment counter from the 4000 series. It counts clock pulses and returns the output in a form which can be displayed on a seven-segment display. This avoids using a binary-coded decimal to seven-segment decoder, but it can only be used to display the (decimal) digits 0-9.

3.6 Software and system control unit:

Assembly language was utilized for the project. It was more than accurate to satisfy design objectives while enhancing the level of understanding of the language. The program code is provided in the appendix while the complete circuit diagram is as shown in Fig. 7. And the prototype is shown in figure 8.

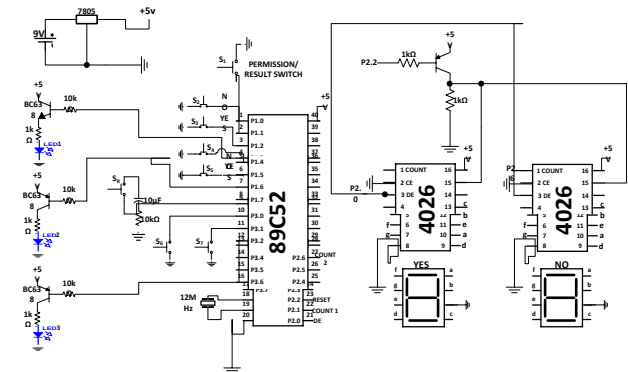


Fig 7 Complete circuit diagram

4. Results and Discussion

The electronic voting system was designed in such a way that no voter can vote except with permission from the arbitrator. The arbitrator has a permission button on his button pad which on pressing gives

permission to the other voters to vote. The arbitrator cannot vote except when there is a tie in the number of votes. The system was designed so because at conferences like a senate, the national assembly the senate president does not vote until there is a tie.

When the system is put on, it automatically resets. The LED on the senate president's button pad is ON indicating no senator can vote. When permission is given to the senators and they cast their votes by pressing yes or no on their button pads respectively, the LED lights on the senator's button pad and the LED on the senate president's button pad goes OFF indicating permission has been given. Immediately the senators cast their vote, the LED on the senator's button pad lights indicating a vote has been cast successfully. When there is a tie in the number of yes and no votes, the LED on the senate president's button pad blinks four times indicating that the senate president can cast his vote.

Table 1 The results obtained after the voting process

Voter 1		Voter 2		7- Segment display	
Yes	No	Yes	No	Yes Votes	No Votes
0	0	0	0	0	0
1	0	1	0	2	0
0	1	0	1	0	2
1	0	0	1	1	1
0	1	1	0	1	1

The system was designed in such a way that all the voters can vote at the same time thereby saving their time and no voter can vote more than one time thereby ensuring a free and fair election. The project as a prototype was designed for only three voters. It implies that when the number of "yes votes" is more than the number of "no votes", the issue under deliberation is implemented and if the number of "no votes" is more than the number of "yes votes", the issue under deliberation is not implemented.



Fig 8: Prototype of Electronic Voting Machine.

5. Conclusion

The design of simple electronics voting systems is very important to the area of applications we have presented. Thus a detail design of an embedded microprocessor system has been presented as demonstrated by the results obtained from the tests carried out. While the project has limitations, this provides an opportunity for expansion of the current project in future years. Our future work is to incorporate a wireless module into the system instead of the wired prototype presented.

References

- Balzarotti, D., G. Banks, et al. (2010). "An experience in testing the security of real-world electronic voting systems." *Software Engineering, IEEE Transactions on* **36**(4): 453-473.
- Chaum, D. (2003). *Untraceable Electronic Mail, Return Addresses and Digital Pseudonyms. Secure Electronic Voting*, Springer: 211-219.
- Keller, A. M., A. Dechert, et al. (2005). *A PC-based open-source voting machine with an accessible voter-verifiable paper ballot*. Proceedings of the annual conference on USENIX Annual Technical Conference, USENIX Association.
- Kohno, T., A. Stubblefield, et al. (2004). *Analysis of an electronic voting system*. Security and Privacy, 2004. Proceedings. 2004 IEEE Symposium on, IEEE.

Kumar, D. A. and T. U. S. Begum (2011). "A Novel design of Electronic Voting System Using Fingerprint." International Journal Of Innovative Technology & Creative Engineering 1(1): 12-19.

McClure, N. and K. Lohry (2001). Electronic voting system, Google Patents.

Mercuri, R. (2002). "A better ballot box?" Spectrum, IEEE 39(10): 46-50.

Proebstel, E., S. Riddle, et al. (2007). An analysis of the Hart Intercivic DAU eSlate. Proceedings of the USENIX Workshop on Accurate Electronic Voting Technology, USENIX Association.

Qadah, G. Z. and R. Taha (2007). "Electronic voting systems: Requirements, design, and implementation." Computer Standards & Interfaces 29(3): 376-386.

Villafiorita, A., K. Weldemariam, et al. (2009). "Development, formal verification, and evaluation of an E-voting system with VVPAT." Information Forensics and Security, IEEE Transactions on 4(4): 651-661.

APPENDIX I

```
ORG 0000H
CLR A
    MOV R0,#00H
    MOV R2,#00H
    MOV R1,#00H
    MOV R3,#00H
    MOV R4,#00H
    MOV R5,#00H
    MOV R6,#00H
    MOV R7,#00H
LJMP SAKAM
OJAY:LCALL OJ
    INC R0
    CJNE R0,#14H, OJAY
    MOV R0,#00H
    RET
OJ:MOV TMOD,#01
    MOV TL0,#0H
    MOV TH0,#3CH
    SETB TR0
    JNB TF0,$
    CLR TF0
    CLR TR0
    RET
RESSET:CLR P2.2
    LCALL OJAY
    SETB P2.2
    RET
ZUBAIR:CJNE A,#0,ONE
    LCALL OJAY
```

```
RET
ONE:CJNE A,#1,TWO
    CLR P2.1
    LCALL OJAY
    SETB P2.1
    LCALL OJAY
    RET
TWO:CLR P2.1
    LCALL OJAY
    SETB P2.1
    LCALL OJAY
    CLR P2.1
    LCALL OJAY
    SETB P2.1
    LCALL OJAY
    RET
ZUBAIRU:CJNE A,#0,ONEE
    LCALL OJAY
    RET
ONEE:CJNE A,#1,TWOO
    CLR P2.6
    LCALL OJAY
    SETB P2.6
    LCALL OJAY
    RET
TWOO:CLR P2.6
    LCALL OJAY
    SETB P2.6
    LCALL OJAY
    CLR P2.6
    LCALL OJAY
    SETB P2.6
    LCALL OJAY
    RET
SAKAM:LCALL RESSET
    CLR P2.0
SAKA:JB P1.2,$;PRESIDENTS PERMISSION
    CLR P1.3; OFF ACK LCD
SEN:JNB P1.4,YESE;YES BUTTON OF SEN1
    JNB P1.5,NOE;NO BUTTON OF SEN1
    JNB P3.0,YESE2;YES BUTTON OF SEN2
    JNB P3.1,NOE2;NO BUTTON OF SEN2
    SJMP SEN
YESE:INC R1
    CLR P1.6
    SJMP SEN2
NOE:INC R2
    CLR P1.6
    SJMP SEN2
YESE2:INC R1
    CLR P3.2
    SJMP SEN1
NOE2:INC R2
    CLR P3.2
    SJMP SEN1
SEN1:JNB P1.4,YAES
```



```
JNB P1.5,NOES
SJMP SEN1
SEN2:JNB P3.0,YAES2
JNB P3.1,NOES2
SJMP SEN2
YAES:INC R1
CLR P1.6
SJMP READY
NOES:INC R2
CLR P1.6
SJMP READY
YAES2:INC R1
CLR P3.2
SJMP READY
NOES2:INC R2
CLR P3.2
SJMP READY
READY:MOV A,R1
MOV DPH,R2
CJNE A,DPH,CONTOUS
BLINK:SETB P1.3
LCALL OJAY
CLR P1.3
LCALL OJAY
INC R3
CJNE R3,#4,BLINK
MOV R3,#00
SETB P1.3
MAS:JNB P1.0,YESSE
JNB P1.1,NEO
SJMP MAS
YESSE:INC R1
CLR P1.3
SJMP RESULT
NEO:INC R2
CLR P1.3
SJMP RESULT
CONTOUS:SETB P1.3
JB P1.2,$
RESULT:MOV A,R1
LCALL ZUBAIR
MOV A,R2
LCALL ZUBAIRU
SETB P2.0
JB P2.0,$
```