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RESEARCH ARTICLE

SCALING CHALLENGES FOR ADVANCED TRANSISTOR DESIGN.

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Abstract

We all are living in the digital world where we are going to use many devices which are fabricated using the CMOS technology. Due to the constraint design of the circuits and long routing schemes we are going to make the chip work a lot harder and it results in high power consumption. In order to reduce the power consumption we prefer to use certain techniques like usage of nano-materials instead of conventional Poly-Silicon. In this technique we are interested to modify certain conditions which results in generation of a new kind of technology which results in low power consumed, high speed circuits and devices which make a new way in the world of electronics. To reduce the power consumption of transistor i.e., when compared with ordinary transistor we has to reduce the power consumption as well as the power dissipation [6]. So we propose the application of nano-materials which have high conductivity as well as low – power dissipation which can be employed in design of Transistors of various technologies (like 200nm., 100nm., 50nm. etc.,).

Introduction:-

CMOS Technology is facing a lot of problems over the last 30 years .In conventional MOSFET we have certain electrostatic limitations like source to drain tunneling, carrier mobility, static leakages etc., [1] [5] .As the size of nano-materials is very small we can use a more number of transistors on a single chip so that size of the chip is reduced its additional features which can relatively reduce the complex fabrication into simple steps of fabrication so device and circuit developers are using this type of devices and also can use different types of materials used to make these type of materials at low cost [2].

For an Ultra-small MOSFET we have to face several problems like high leakage current, high threshold voltage, high inter-connective capacitances, static leakages etc., all these problems can damage the MOSFET by reducing its performance [1] [5].

In the VLSI industry it is critically necessary to have a device which has low power dissipation and has high performance along with long time durability. In order to achieve such characteristic features in a real time operation scenario it will be a hard tenacious task [11]. More in the present modern world the electronic device must have low response time along with low power consumption provided the cost of the device must be in a nominal range [7]. Using a conventional MOSFET device can no longer sustain such a modern day challenge. So if we use Nano-Materials we can meet the modern day challenge [3][4].

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In this paper we had replaced the Poly-Silicon material present on the Gate Terminal of the MOSFET device with different Nano-Materials like Si (Silicon Nano-Wires), ZnO (Zinc Oxide Nano-Wires), CSi (Carbon-Silicon or Silicon Carbide Nano-Wires),Pani (Poly-Aniline Nano-wires), Pedot:pss (Poly Styrene Sulfonate Nano-Wires)[8][9] .

Fig. 1:- Schematic of Nano Wire FET.

In this paper we reduced the gate length i.e, the size of gate is reduced from 200 nm to 50 nm, for all the materials (Poly-Silicon, SiO, ZnO, CSilicon, Pani, PedotPss) and their characteristic parameters like drain current, threshold voltage are extracted.

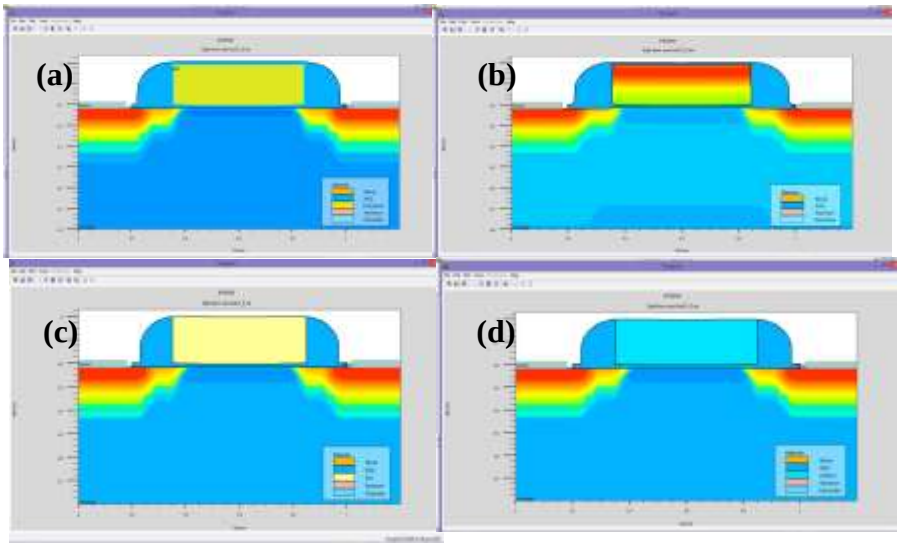
Literature Survey:-

Design Methodology:-

In this paper we have used Silvaco Software for the design of the Nano-Wire FET. Initially we have designed a Nano-Wire FET of 200 nm in size. There are two different design styles which are represented in figures (2) & (3).Basically first we will mention the X co-ordinates and Y co-ordinates in the software which will guide the software to lay the Silicon Wafer to those desired Co-ordinates. Later the Sio (Silicon Oxide) material is laid [10].

Then it is etched to form gate, source and drain terminals. Later, respective impurities are doped accordingly. After doping process is completed, the respective Gate material is laid. Since we have used different gate materials like Pani, Pedot:Pss, Si, ZnO, CSilicon,Polysilicon etc., each material is laid one at a time. Now the Gate material is etched at source and drain terminals. Based on the required sizes i.e. based on required gate lengths it is etched once again [10].

Now over the Gate terminal once again the Silicon Dioxide (SiO_2) material is laid and is etched off at source and drain terminals. Now Aluminum metal is laid which forms the respective metal contacts for the so designed FET [10].



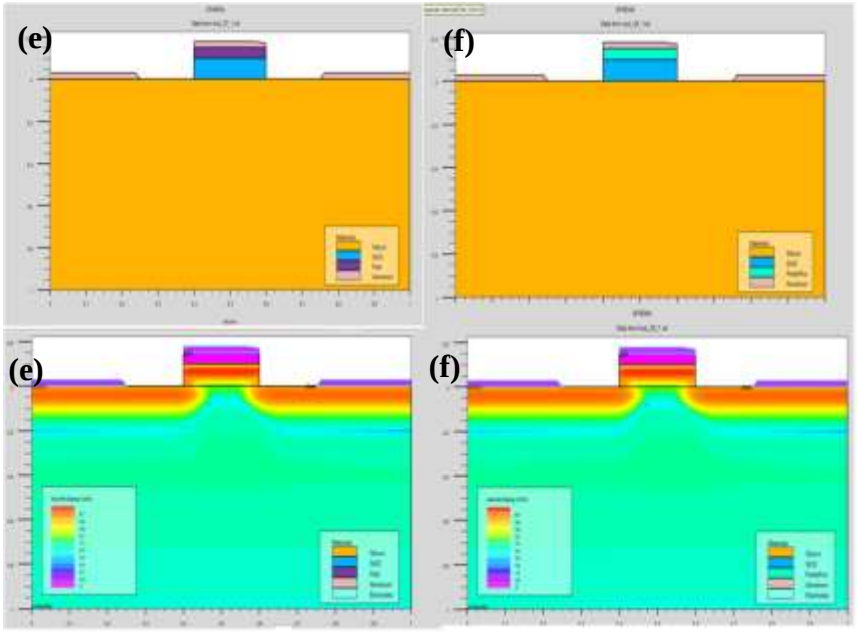


Fig 2:- Schematic of different Nano Wire MOSFETs: a) PolySilicon ; b) Silicon Nano Wire ; c) Zinc Oxide Nano Wire ; d) Carbon Silicon; e) Poly Aniline; f)PEDOT:PSS materials in Silvaco Software.

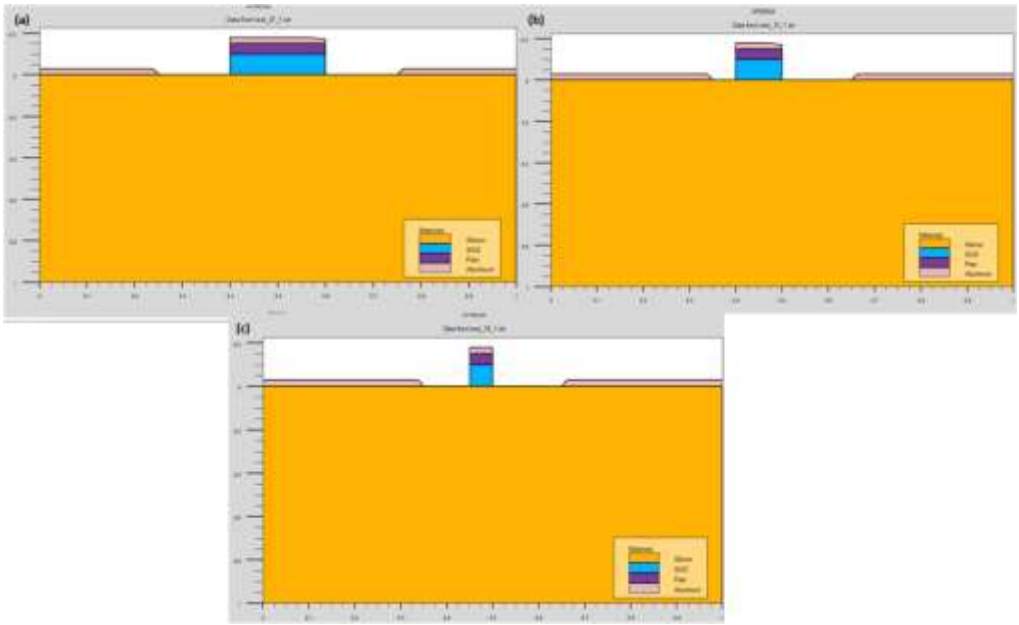


Fig 3(a):- Schematic of different gate sizes of Nano Wire MOSFETs: a) 200 nm; b) 100nm; c) 50nm technologies in Silvaco Software (No Doping Concentrations are shown)

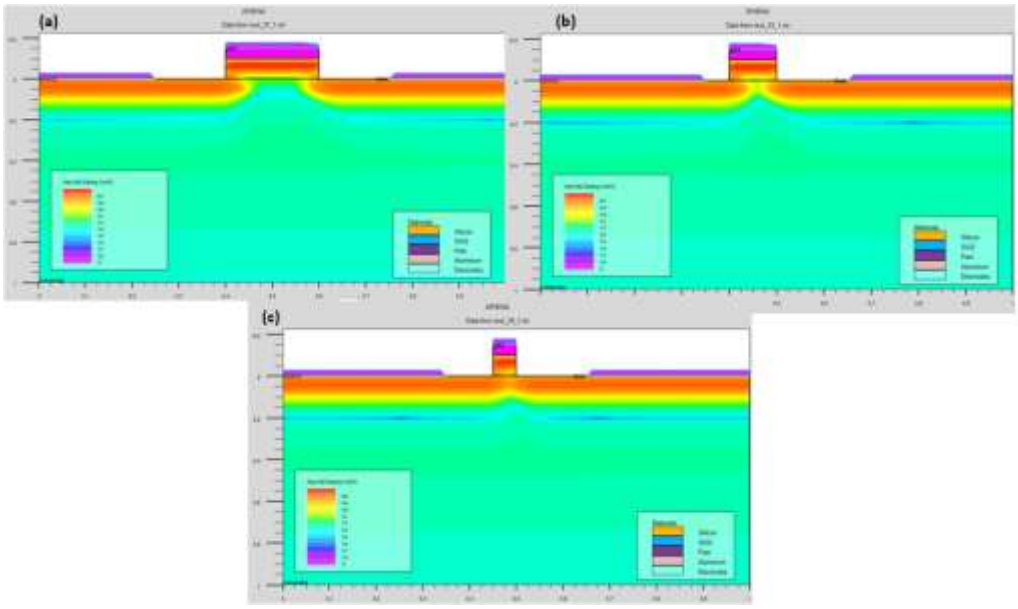


Fig 3(b) :- Schematic of different gate sizes of Nano Wire MOSFETs: a) 200 nm; b) 100nm; c) 50nm technologies in Silvaco Software (Doping Concentrations are shown)

Equations:-

Saturation region drain current: $I_d=(\mu c_{ox}\,\omega)/(2L)*(V_{gs}-V_t)^2*(1-V_{ds}/V_A)$; $V_{ds}>=V_{gs}-V_t$

Ohmic region drain current : $I_d=(\mu c_{ox}\omega)/(2L)*[2*(V_{gs}-V_t)V_{ds}-V_{ds}^2]*(1-V_{ds}/V_A)$; $V_{ds}<V_{gs}-V_t$

Oxide capacitance : $c_{ox} > €_{ox}/t_{ox}$

Transconductance : $g_m>(\mu c_{ox}\,\omega/L)(V_{gs}-V_t)$

Output resistance : $R_o=|V_A|/I_{do}$

Input capacitance : $C_{in}>C_{gs}+C_{gd}=C_{ox}L\omega$

Transition frequency : $F_c>g_m/(2*pi*C_{in})$

Surface mobility holes : $\mu>200cm^2/V\text{-}s$

Surface mobility electrons : $\mu>450cm^2/V\text{-}s$

where

Drain current = I_d; *Oxide capacitance* = c_{ox}; *Transconductance* = g_m; *Output resistance* =R_o; *Input capacitance* = C_{in}; *Transition frequency* = F_c; *Electronic Field Strength in Oxide* = $€_{ox}$; *Gate to Source Voltage* = V_{gs}; *Drain to Source Voltage* = V_{ds}; *Thicknessof Oxide Layer* =t_{ox}; *Threshold Voltage* = V_t.

Results and Discussions:-

After designing the FET the I_{ds} Vs. V_{gs} parameters for different gate materials of different gate lengths has been plotted as shown in figure (4).

The I_{ds} Vs. V_{gs} parameter for various materials of 200 nm is shown in figure (4.a). From the figure we can understand that ZnO (Zinc Oxide) material has low drain current .

Similarly for 100 nm technology shown in figure (4.b) the I_{ds} Vs. V_{gs} parameter has been plotted. From this we can understand that PAni (PolyAnniline) has least drain current value.

For 50 nm technology shown in figure (4.c) the I_{ds} Vs. V_{gs} parameter is taken and is represented as a graph, from which we can conclude that ZnO is ideal material to be used in this technology as it has least drain current parameter.

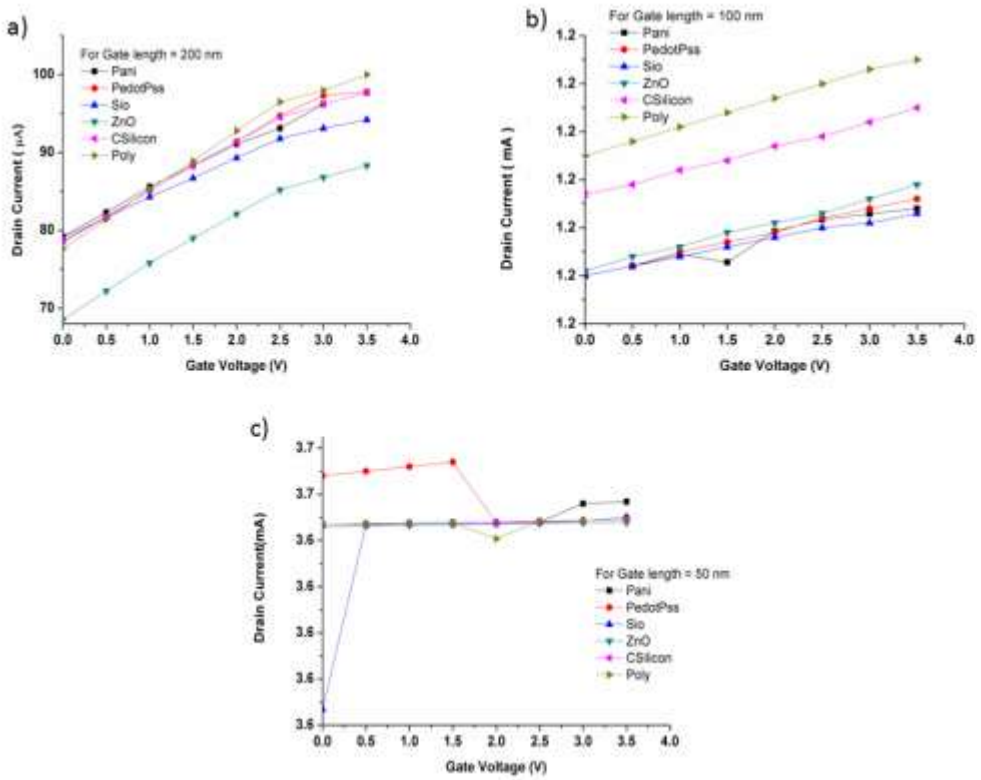


Fig 4:- I_{ds} Vs. V_{gs} Characteristics for Channel lengths a) 200 nm; b) 100 nm; c) 50 nm gate channel lengths (for constant V_{ds} = 0.1 Volts)

Similarly after plotting the Threshold Voltage values we can observe that the ZnO material has least threshold voltage value at 50 nm technology while CSilicon has low threshold voltage for 100nm ; 200 nm technologies. But as the current trend is all about scaling down of IC's it will be ideal to use the ZnO nano material in the design of FET having less gate lengths.

Similarly if we consider the Polymeric compounds PAni (Poly Anniline) has least threshold voltage value but not a good one when compared with ZnO material.

Gate Length	Threshold voltage of Pani	Threshold Voltage of PedotPss	Threshold Voltage of Pani	Threshold Voltage of Csilicon	Threshold Voltage of ZnO	Threshold Voltage of SiO
Nm	Volts					
50	0.75	0.75	0.25	0.15	0.05	0.8
100	1	1.5	0.5	0.45	0.75	1
200	2	2	1	0.89	0.94	2

Fig 5 Threshold Voltages for different Gate Materials and for different Gate lengths.

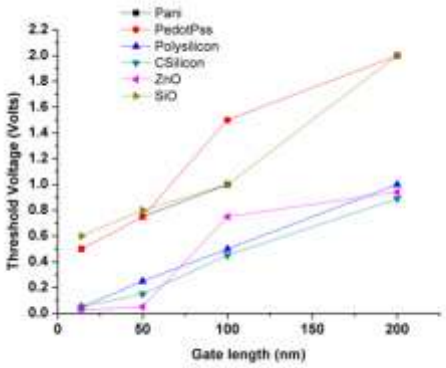


Fig 6:- Threshold Voltages for different Gate Materials and for different Gate lengths.

Conclusion:-

From I_{gs} Vs. V_{gs} THRESHOLD VALUES , I_{ds} Vs. V_{ds} CURVE VALUES, Gate channel length effects, i.e. figures(4),(5),(6) we can observe that the FET designed using the Poly Aniline Nano-wire Material has less drain current , drain voltage , low threshold voltage, when compared with other polymeric compounds, while overall performance parameters are best for Zinc-Oxide (ZnO) material when compared with all the above mentioned materials.

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