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RESEARCH ARTICLE

A Novice Design of CMOS Based VCO for Signal Processing Based Applications.

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Abstract

CMOS based devices are highly recommended for low static power consumption and noise immunity. CMOS technology is used in various analog circuits like Comparator, Amplifier, Digital to Analog, Analog to Digital converter, Voltage Controlled Oscillator and many others. Here in this paper author have introduced a novice CMOS based VCO circuit using an commercially available 0.13µm CMOS technology .The circuit have been designed using Microcap 11 .It can be used in many application in which one want to control the oscillation frequency of the circuit by applying an external voltage and to achieve this we have proposed a VCO circuit using CMOS to reduce the power consumption an to reduce the phase noise

Introduction:-

An oscillator is designed so that we can vary the oscillation frequency over some range by an input current or input voltage .The Voltage Controlled Oscillator is mainly used in Phase Locked Loop in which we need to lock the oscillator's frequency with another oscillator . It is frequent in modern communication circuits which is used in modulator , demodulator ,filters etc . It also has an important part to form the basis of frequency synthesizer circuit which used in tuning of televisions and radios .[1][2] Generally radio Frequency VCO's are made by the combination of varactor diode with the tuned circuit or with the resonator in an oscillator circuit. As we change the DC voltage across the varactor , its capacitance changes and which directly changes the tuned circuit's resonant frequency A VCO is an oscillator circuit in which the oscillation frequency is control by an externally applied voltage. One more features which is required for VCO is a linear relationship between control voltage and oscillation frequency.

VCO are generally divided into two category based on type of waveform it produced :

Linear/Harmonicoscillator:-

Generates the sinusoidal waveform Harmonic oscillators in electronics that usually consists a resonator with a amplifier which replaces the resonator losses (to avoid the amplitude of waveform from decaying) and it isolate the resonator from the output (so that the load does not affect the resonator)

Relaxation oscillators:-

Are able to generate a triangular or a sawtoothwaveform and commonly used in monolithic integrated circuits . They can provide a wide range of operational frequencies with a minimal number of external components

Basicsof VCO:-

A. Basic block diagram:-

Basic block diagram of the type of VCO shown in figure-1 which is used in almost all integrated circuit VCO. In block diagram voltage controlled source is used in charging and discharging of timing capacitor C_t. The time periods of charging and discharging controlled by action of Schmitt trigger circuit. The voltage across C_t is the input voltage for Schmitt trigger. Two threshold voltage switching level , V_L and V_H in Schmitt trigger circuit and width of hysteresis curve of schmitt trigger is given as

$$V_W = V_H - V_L \quad (1)$$

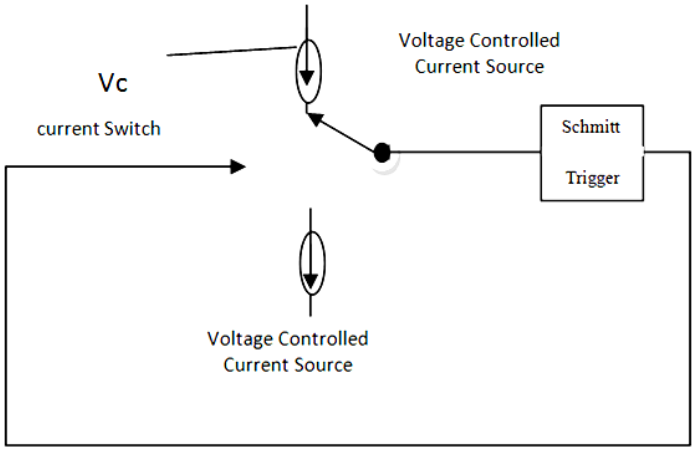

Figure 1: Basic Block diagram of a type of VCO[1][20]

B. Operation:-

The voltage across C_t will vary linearly with time because C_t is charged and discharged by current source. The voltage waveform across C_t will be symmetrical triangular waveform[6]. If the charging and discharging current will be of equal magnitude , the top current source charge the timing capacitor $C_t$upto a voltage level equal to the V_H triggering level and at this time schmitt trigger is activated and it cause the disconnection of top current source from C_t and connects the bottom current source with C_t and is this way the bottom current will discharge the capacitor to lower triggering level V_L and again at this time the schmitt trigger activated and it make the current source to be switched again and the whole cycle is repeated.[5]

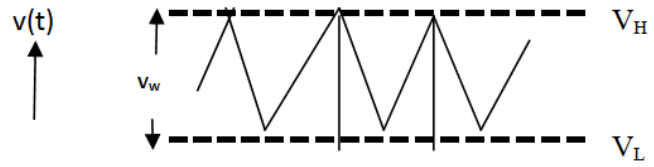

Figure 2: Waveform of VCO

Slope of the voltage across C_t is given as

$$\frac{dv(t)}{dt} = \frac{d(Q/C_t)}{dt} = \left(\frac{1}{C_t}\right)\left(\frac{dQ}{dt}\right) = \pm\frac{I_Q}{C_t} \qquad (2)$$

and the time require to switch capacitor voltage from V_H to V_L or vice versa a given by

$$\frac{V_H - V_L}{\Delta t_2} = \frac{I_Q}{C_t} and \frac{V_L - V_H}{\Delta t_1} = \frac{I_Q}{C_t}$$

It implies

$$\Delta t_1 = \Delta t_2 = \frac{(V_H - V_L)C_t}{I_Q} = \frac{V_W C_t}{I_Q} \qquad (3)$$

so the oscillation period T is given by

$$T = \Delta t_1 + \Delta t_2 = \frac{2V_W C_t}{I_Q} \qquad (4)$$

the oscillation frequency f_o is given by

$$f_o = \frac{1}{T} = \frac{I_Q}{2V_W C_t} \qquad (5)$$

C.Basic VCO characteristics:-

Like all analog circuits , VCO also has certain design requirements which are required for many fundamental aspects of circuits :

- **VCO Tuning Range :**It must be define that the range of the loop at which VCO is expected to operate , for such expected range the VCO must be tunable . This basic requirement is not always very easy to meet . It may bring the VCO or resonant circuit to be switched in other extreme circumstances .
- **VCO Tuning Gain :** Gain of VCO is measured in terms of Volts/Hz . It is defined as the tuning shift for any given change in voltage . It may affects some overall loop gain calculation

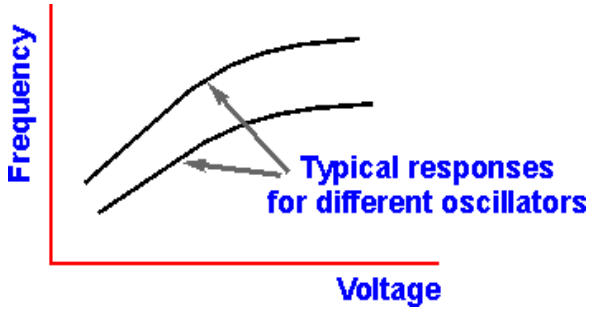

Fig 3 :Voltage controlled oscillator V/f curves

The above curve is relatively straight at lower frequency and become flat at higher voltages.

- **VCO V/f Slope :** It is an important requirement for any VCO which is used in PLL .The Voltage to Frequency curve is monotonic means typically frequency increases for increase in voltage and if any change happens , it may result of spurious resonance which can make the loop unstable . Therefore it must be avoided if the PLL is to operate satisfactorily .

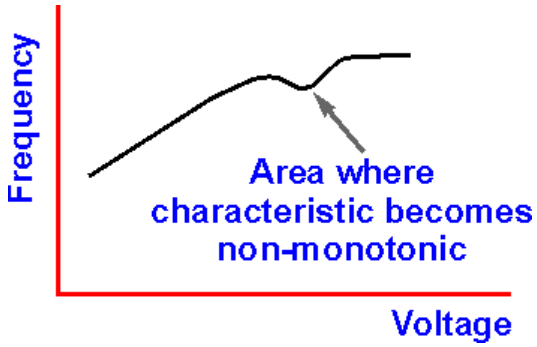

Fig 4 :Voltage controlled oscillator V/f curves

Proposed cmos based vco circuit:-

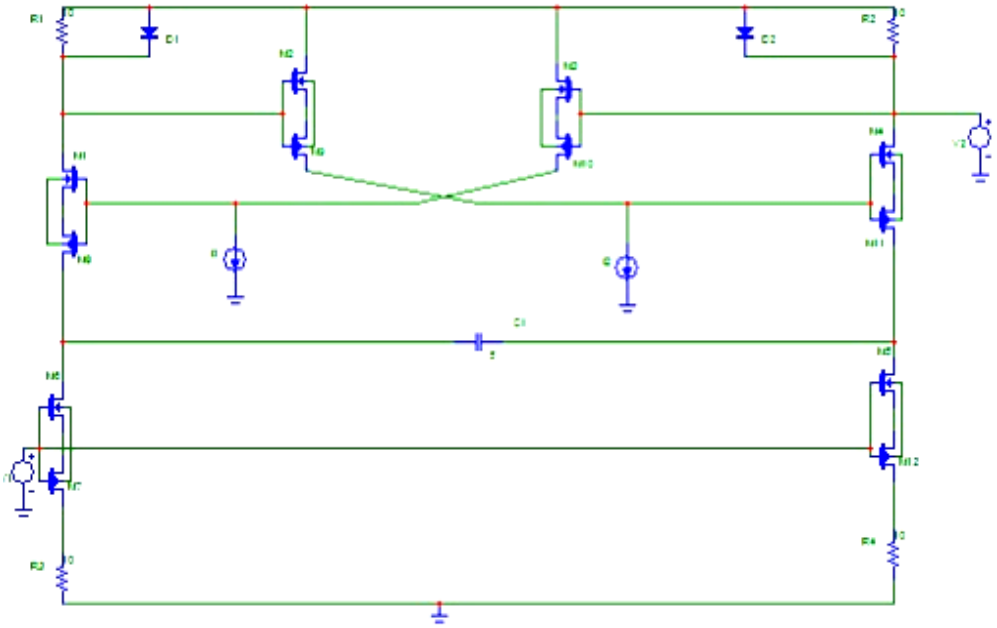

Fig 5 : Proposed CMOS based VCO Circuit

Through the performance of the VCO we can determine various factors like FM distortion , Centre Frequency , Operating Frequency Range etc . In the proposed circuit the charging current is varied with response to the control input . In the proposed circuit we first assume that M1 and M8 is turned OFF and M4 and M11 is turned ON. We first assume that the value of current I is very large so that IR voltage drop is large to make the diode Q6 turn ON , Thus the Gate of M3 and M10 is one diode drop below V_{DD} . and the source is two diode drop below low V_{DD}. If we neglect the gate current of M2and M9 its gate as at V_{DD} and its source is one diode drop below V_{DD}. Thus the source of M4and M11 is two diode drops below $V_{DD.}$ Since M1 and M8 become more negative [8]CMOS (M1 and M8) will then turn ON and the resulting source current in (M1 and M8) turns ON diode Q5 as a result the gate of M2 and M9 move in negative direction by one diode drop and causes the gate of M4and M11 to move positive by one diode drop because Q6also turn OFF[12][13] .As a result the gate source junction of (M4and M11) is reverse biased by one diode drop because the voltage on C can not change instantaneously .Current I_1must now change the capacitor voltage in the negative direction by an amount equal to two diode drops before the circuit will switch back again and the circuit is symmetrical , therefore the half period is given by time required to charge the capacitor [7]

$$\frac{T}{2} = \frac{Q}{I1} \qquad (6)$$

Where $Q = C\Delta V = 2CV_{GS}$ is change on the capacitor and the frequency of oscillator is given as

$$f = \frac{1}{T} = \frac{I1}{4CVGS(ON)} \qquad (7)$$

Experimental results:-

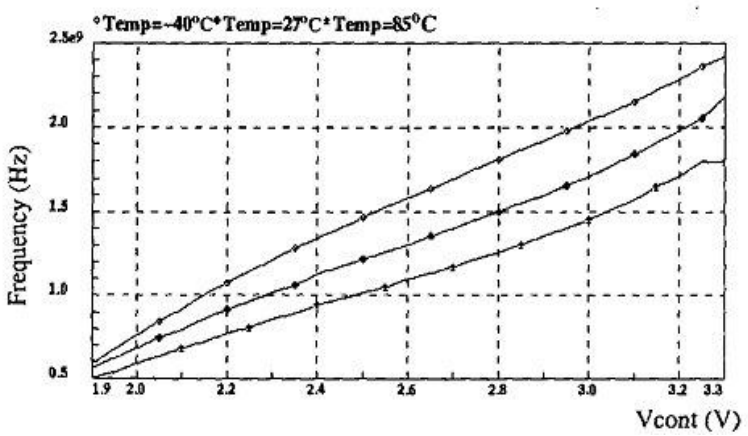

Fig 6 : Transfer Function Of Proposed VCO

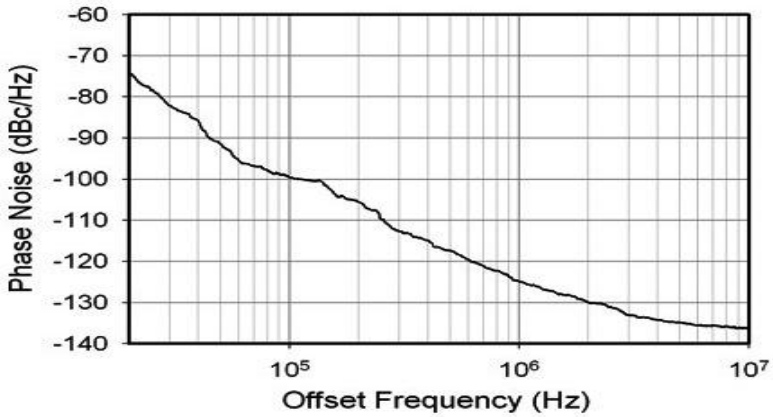

Fig 7 : Noise Measurement Of Proposed VCO

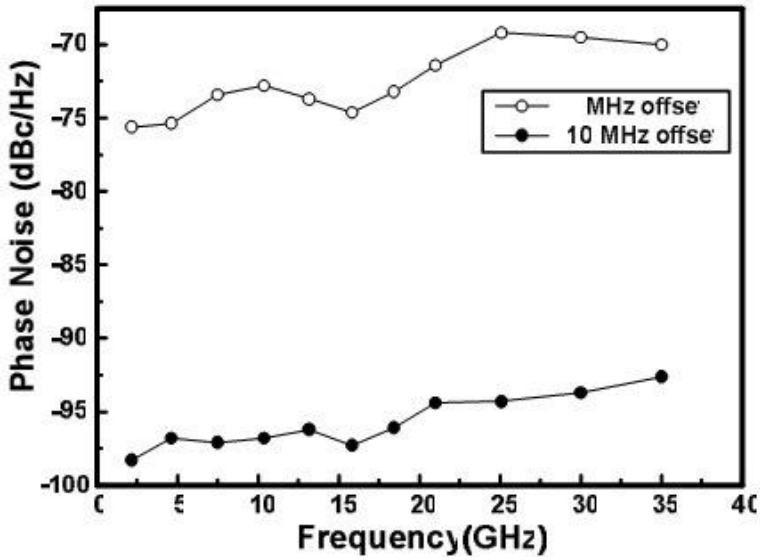

Fig 8 : Harmonic Rejection Of Proposed VCO

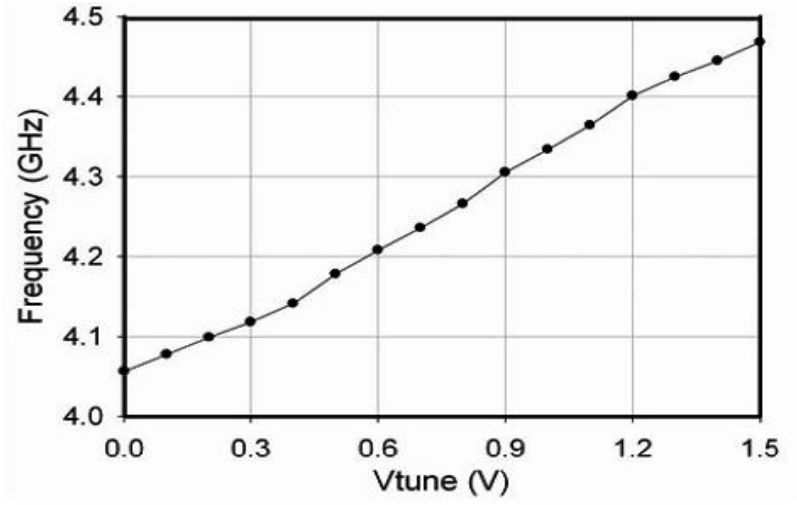

Fig 9 : Frequency Response Of Proposed VCO

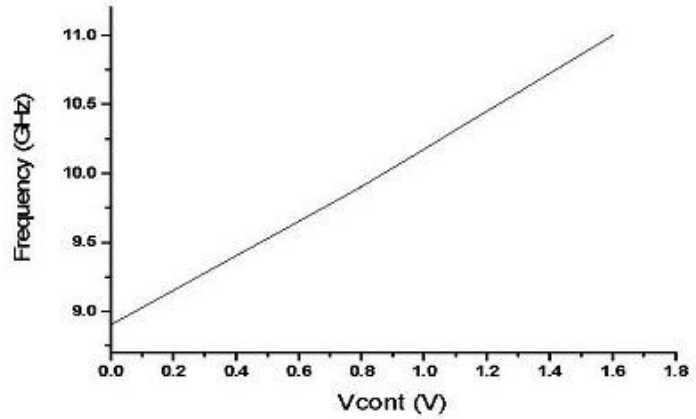

Fig 10 :DC Analysis Of Proposed VCO

This VCO has been designed in ancommercially available 0.13µm CMOS technology. Phase Noise estimations were performed utilizing the Microcap 11 measurement system. Fig. 7 demonstrates the decaying of noise from -85 dbc/Hz to -100 dbc/Hz as we increase the offset frequency from 10^4 to 10^5 Hz again it decays slightly from -100 dbc/Hz to -125 dbc/Hz as we are increasing the offset frequency from 10^5 to 10^6 Hz and it continuously decays and reach value -135 dbc/Hz at 10^7 Hz of offset frequency .Fig 6 demonstrate the transfer function of the given proposed circuit and we have taken several responses at different temperatures i.e at 27^0 C , 40^0C and at 85^0C .the graph shows at temperature 40^0C the grows linearly and start to increase in voltage from 1.9 V and reach the max. value of frequency to 2.35 Hz and as we increase the temperature from 40^0C to 85^0C the max. value of graph decays and at 85^0C its max. value of frequency become 1.65Hz .Fig 8 demonstrate the harmonic rejection of the proposed VCO , Harmonic rejection refers to avoid the spikes generated in the response due to noise and in our proposed circuit from 0 to 20 GHz the spikes generated increase the phase noise from -100 dbc/Hz to the -95 dbc/Hz and as the frequency increases above 20 GHz it increases linearly.Fig 9 demonstrate the frequency response of the proposed VCO and its shows that as we in increase the V_{tune} from 0.0V to 1.5V the frequency increases from 4.06GHz approx. to 4.48GHz approx. linearly . Fig 10 demonstrate the DC analysis of the proposed VCO circuit and it gives a linear relation between Frequency and voltage which is required for any circuit genuine performance .[18][19]

Conclusion:-

This paper proposed the design of a CMOS based VCO circuit in this paper we have demonstrated various results of the given proposed VCO circuit like Phase Noise Response , Harmonic Rejection Response , Frequency Response of the Proposed Circuit etc. This paper provides us a solution to low phase noise and to avoid the Harmonics generated in the response due to Noise. By using VCO circuit built by CMOS instead of BJT or MOS we have achieved the required response .

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