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RESEARCH ARTICLE

Modified decimal matrix codes for error detection in memory using pipeline architecture.

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Abstract

Transient multiple cell upsets (MCUs) are becoming major issues in the reliability of memories exposed to radiation environment. To prevent MCUs from causing data corruption, more complex error correction codes (ECCs) are widely used to protect memory, but the main problem is that they would require higher delay overhead. A novel decimal matrix code (DMC) based on divide-symbol was proposed to enhance memory reliability with lower delay overhead. But DMC required more number of redundant bits. To overcome this issue Modified Decimal Matrix Code (MDMC) was introduced with less number of redundant bits. The MDMC is typically performed using reconfigurable Array Exclusive-OR Logic (ReAXL) to compute the equivalent decimal addition. The MDMC based on ReAXL dynamically reconfigured for both Encoding and decoding and hence reduced the chip area. This MDMC can be extended to 64 bit memory or 128 bit memory by implementing this in pipeline architecture.

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Introduction:-

The digital communication systems have taken a greater leap over the last decade. The technology scales down to the nanotechnology and also the memories are becoming more complex with many advanced electronic systems The major threats to the digital systems are various types of errors like soft errors due to radiations, transient multiple errors etc. Also the rate of errors has increased in the memories. Thus the memories get exposed to the alpha particles or the cosmic rays resulting in single bit or multiple bit errors. To ensure the reliability of the memories, some Error Correcting Codes (ECC) are widely used. But these codes require more area, power, and delay overheads. This is because of the complexity of the encoder and decoder circuits. Initially interleaving technique was implemented where the same logical word has been rearranged into different physical words. The tight coupling of hardware structures from both cells and comparison circuit structures made the interleaving method less reliable. Following this was the Single Error Correcting Codes (ECC) like Hamming codes. But this could correct only single error. Later these codes were extended to the Single Error Correction Double Error Detection Double Adjacent Error Correction (SEC-DED-DAEC) codes. These SECDED-DAEC codes were modified later on by adapting some peculiar properties of the Orthogonal Latin Square (OLS) Codes and Golay codes. Afterwards the matrix codes based on the hamming codes were introduced. Matrix codes successfully reduced the decoding delay. However the number of redundant bits required was elevated. To reduce this Decimal Matrix codes were designed. The basic error correcting codes comprises of an encoder and a decoder units. The encoder unit generates the required redundant bits according to the Error correcting scheme that is being used. Once the redundant bits are generated, then the digital information is transmitted or stored in the memory. During the decoding, the previously generated redundant bits are compared with the newly calculated redundant bits. Any mismatch in the redundant bits indicates the presence of an error. In order to correct these errors an error locator and error correction units are also employed. The error locating unit identifies the error location through the proper processing of the redundant bits. The error correcting circuit corrects the errors and retrieves the initial digital data lucratively. The encoding and the decoding

units require an encoder circuit in order to generate the redundant bits. This makes the circuit complex. To reduce the complexity the Encoder Reuse Technique (ERT) was introduced, where the same encoder is reused in the decoding section. This research work was carried out to come up with a better Error Correcting Scheme with less delay over head and power consumption. For this purpose, various existing systems were studied in detail and their advantages and disadvantages were noted down. From these details a design was developed with lower delay that contains some adapted qualities from the other models.

Existing System:-

The Decimal Matrix Code (DMC) is a potential Error Correcting Scheme employing decimal algorithm. First, during the encoding (write) process, information bits D are fed to the DMC encoder, and then the horizontal redundant bits H and vertical redundant bit V are obtained from the DMC encoder. Once the encoding process is over, the coded DMC code word is stored in the memory. If any MCUs occur in the memory, these can be corrected during decoding (read) process. The schematic of the DMC System is depicted in the Fig.1.

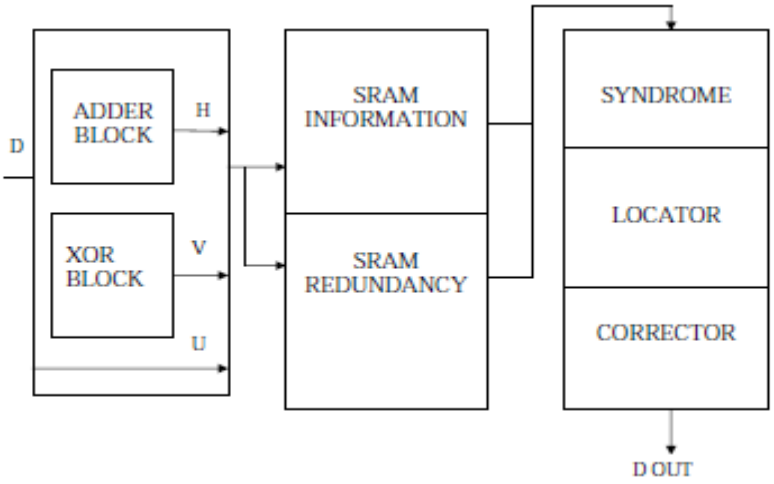

Fig.1:- Schematic of DMC System

These codes employs the simple decimal operations such as addition, XOR operation etc for the check bit generation. This scheme of error correction is explained with an example of a 32 bit data. The 32 bit data is converted in to a matrix of 2*4 dimensions. Now along with this we add the Check bits both in the horizontal direction and the vertical direction. The horizontal check bits are calculated by the addition of two 4 bit data. Such 4 bit data are called symbols. Hence the horizontal check bits are generated by the addition of two symbols. Thus by adding two 4 bit data we get 5 bit horizontal check bits along with the carry. Thus for a complete of 32 bit data, we have 8 set of 4 bit data symbols. Thus by adding them we get total of 20 horizontal check bits. The vertical check bits are calculated by simply carrying out the bit wise XOR operation of the vertical data bits. Thus for a 32 bit data, we have 16 vertical check bits. Thus the total number of redundant bits are 20+16=36. From this we can conclude that the main limitation of this codes is the higher number of check bits. The main reason for higher check bit is the higher number of the horizontal check bits. To reduce this, the horizontal check bits are calculated by the XOR operation of the 4 bit alternative symbols. This block is called the Re-configurable Exclusive or Logic (Re-AXL). This reduces the number of check bits from 36 to 32. The encoding can be performed by decimal and binary addition operations. This system consists of an encoder, a decoder, an error locator and an error corrector. The encoder is reused in the decoder to reduce the complexity of the system. Here encoder receives the data and process the data to generate the horizontal and the vertical check bits. Once the check bits are generated, then the data along with the check bits are stored in the memory or transmitted in the case of data communication systems. This complete process is termed as the write process. For retrieving the data, the system receives the stored or transmitted data along with the initially calculated check bits. Now the encoder unit is reused to generate a new set of check bits from the received data by the same method. For the easier understanding, this set of check bits are known as the syndromes. These syndromes are then compared with the previously calculated check bits. Any mismatch in the check bits refers to the possibility of any errors. The location of the errors can also be deduced by processing the horizontal and vertical check bits together. Then the error corrector corrects the errors by toggling the data at the

error locations. This complete process is termed as the read operation. The encoder that computes the redundant bits using multi bit adders and XOR gates is shown in Fig.2.

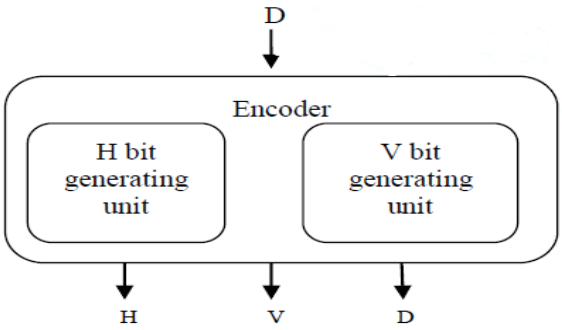

Fig.2:- DMC Encoder unit

For the convenience, the encoder system is reused in the decoder system. In order to make this possible, a 2 bit enable signal is employed. Whenever the enable signal is 01, the encoder will carry out the write operation. When the enable signal is 10, the encoder will act as a part of decoder to perform the read operation. Table I gives the enable signals and the corresponding operation of the encoder.

Table I:- ENCODER OPERATION

Enable Signal	Encoder Operation
01	Write Operation
10	Read Operation

Proposed System:-

The speed of execution of any system is influenced by many factors. By using a faster circuit technology to build the processor and the main memory, the performance can be enhanced. Another possibility is to arrange the hardware in such a way that more than one operation can be performed at the same time. Thus the number of operations performed per second is increased even though the elapsed time needed to perform any one operation is not changed. This is the basic concept behind the pipelining of the systems. The schematic representation of the idea of pipelining is depicted in the Fig.3.

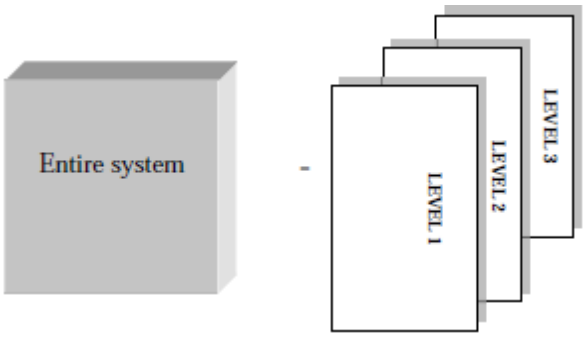

Fig.3:- The schematic representation of pipelining

In the Pipelined MDMC, the entire DMC is divided in to small units that function simultaneously. The DMC system consists of read and write processes. Initially the inputted data has to be processed for the calculation of horizontal and vertical redundant bits. Then these data along with the vertical and horizontal redundant bits will be stored in the memory. This process is called the write operation. Then the Written data should be retrieved, along with the calculated vertical and horizontal redundant bits. Here the dividing of the DMC is explained in the Fig.4. and Fig.5.

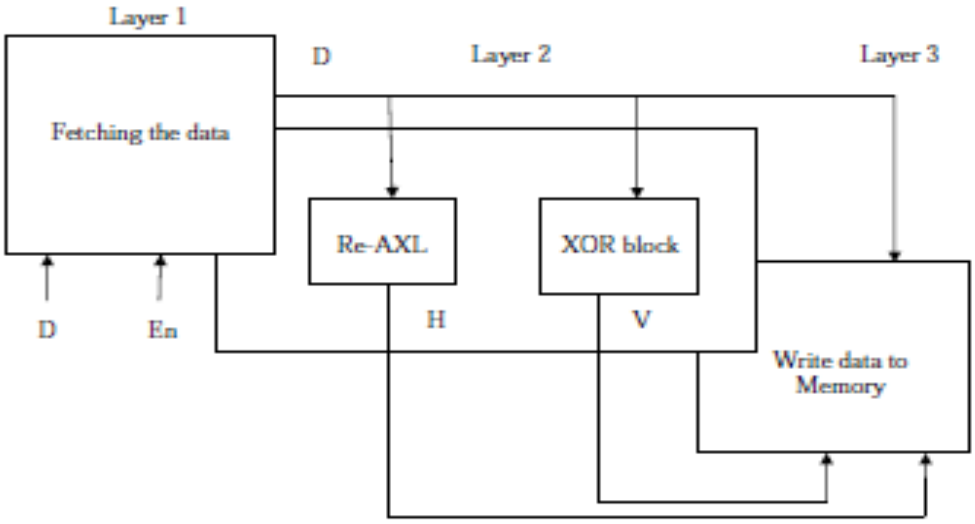

Fig.4:- Pipelined MDMC encoder

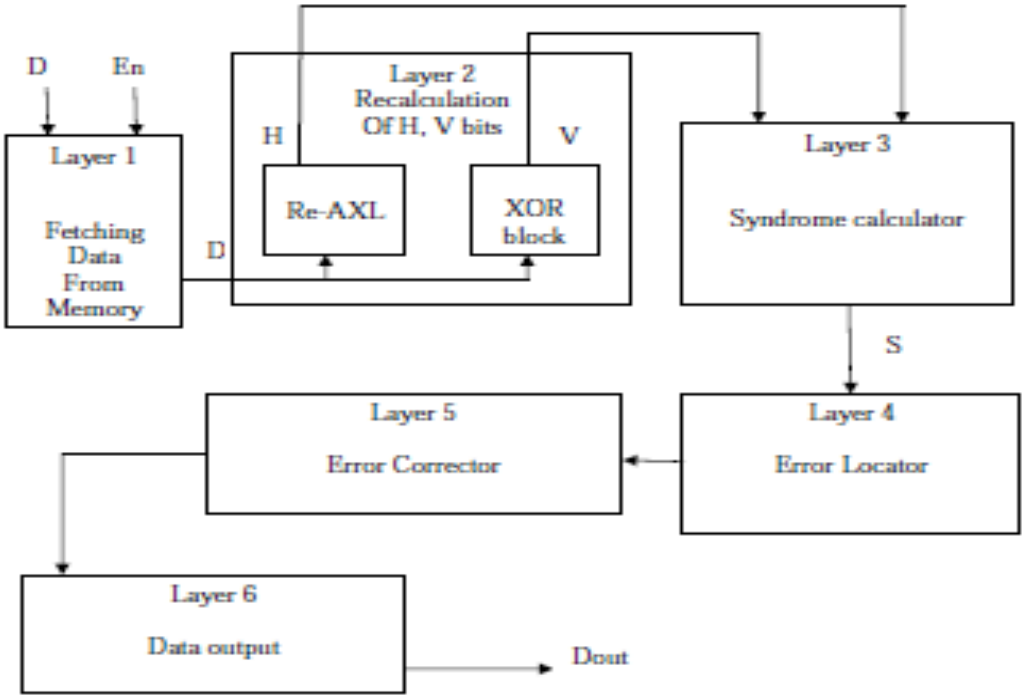

Fig.5:- Pipelined MDMC decoder

Later the horizontal and vertical redundant bits will be recalculated from the retrieved data following the same process. These calculated redundant bits and the earlier obtained data bits will be compared. If any variations are there in these redundant bits, that refers to errors in the retrieved data. Now if there are no variations in the retrieved data, then there exist no errors. Inorder to locate the errors if any, the syndromes are calculated. The syndrome is calculated by simply taking the XOR of the earlier calculated redundant bits and the newly calculated redundant bits. The presences of errors are indicated and located by the nonzero syndromes. After locating the errors, these errors will be corrected with an error corrector. Here actually at the location of the erroneous data bit, the stored data is toggled to get the exact data. Finally the corrected data will be fed to the output. This is the entire MDMC system. This can be divided in to the encoding process and the decoding process. By implementing pipelining in the encoding Process, the entire process is divided in to the following layers. Fetching the data, H and V bit calculation

and write data, H, V bits in to the memory. Here all these layers function simultaneously. While calculating the redundant bits of the second data set, the third data set can be fetched. Also the first data set can be written in to the memory. Similarly the decoding process is also divided in to different layers. They are fetching the data, Recalculation of redundant bits, Syndrome calculation, Error locator, Error Corrector and Corrected data out. The first layer extracts the data along with the redundant bits from the memory. The second layer recalculates the vertical and the horizontal redundant bits. The third layer calculates the syndromes. The fourth layer locates the errors with the help of the syndromes that are calculated. The fifth layer corrects the errors in the located erroneous bit positions. Finally the corrected data is obtained as the output in the last layer. As we have already seen, these layers work simultaneously and hence the delay over head can be reduced to a greater extend. The pipelined structures will more complex compared to the ordinary structures. The main reason for this is the presence of different layers. In this pipelined structured MDMC, the Re-AXL blocks are employed for the calculation of the horizontal redundant bits. This is much better that the adder blocks used in the DMC systems. This replacement helps in reducing the redundant bits number. Also this has another advantage. By replacing the adder with the Re-AXL block, the rippling will be reduced in the calculation of the horizontal bits. This will also contribute to the reduction in the delay overhead. Also the power consumption will reduce when the rippling reduces. The Encoder Reuse Technique (ERT) is also employed in the Pipelined MDMC. This is because at a time either encoding or decoding is carried out and hence here the encoder can be reused in the decoding also. By adapting the ERT, the complexity of the pipelined structure can be reduced. However, by adapting this method, either the system can act as an encoder or decoder at a time. For the determination of the mode of operation of the encoder an En (enable) signal is used.

Result and Discussion:-

The pipelined MDMC system has been implemented in HDL, simulated with ModelSim and tested for functionality by giving various inputs. The area, power, and critical path delay of extra circuits have been obtained. For the comparison work, the hamming code, DMC and MDMC codes were also simulated. The Pipelined MDMC has superior protection level compared to the hamming, DMC and MDMC codes. The pipelined MDMC also provide effective tolerance against the Multiple Bit Upsets. For each protection code, area, power, and delay overheads of encoder and decoder have been shown in Table II. From Table II, we can observe that the pipelined MDMC has a significant reduction compared with other codes. The area and delay overheads of the hamming code are 58409.1 μm^2 and 6.7 ns respectively. The power consumption is 132.3 mW. In the case of the DMC code area delay and power overheads are 41572.6 μm^2 4.9 ns and 164.24 mW. For the MDMC code area delay and power overheads are 10393.2 μm^2, 3.2 ns and 122.59 mW. Coming to the pipelined MDMC system the area overhead becomes 25632.9 μm2, delay is 2.76 ns and power consumption is 118.42 mW.

Table II:- Overhead Analysis

ECC	AREA(μm2)	DELAY(ns)	POWER(milli Watt)
Hamming	58409.1	6.7	132.3
DMC	41572.6	4.9	164.24
MDMC	10393.2	3.2	122.59
PipelinedMDMC	25632.9	2.76	118.42

From this information we can understand that the pipelined MDMC has the least power and delay. However in the case of area since the pipelined structure is more complex compared to the other systems. The adder in the DMC was replaced with the Re-AXL which will prevent the rippling of carry. This is also a reason for the reduction in power and delay. However the main source of delay in this circuit (critical path) is the error locator. Here each redundant bit is compared with each other and this requires more time. The synthesized report reveals that the implementation of this pipelined MDMC system requires 140 IO pins, 3 registers, 32 multiplexers, 68 flipflops and latches. The maximum frequency of operation is 186.637 MHz.

Conclusion:-

This paper analyses the various existing coding techniques that are used for error correction in the digital systems. Some systems show adequate improvement in area and power analysis but fails in the delay analysis. Some other works that are considered fails to give improvement in any fields. By analyzing table, it can be concluded that the Modified Decimal Matrix Codes (MDMC) is efficient among the existing method. The MDMC code provides single and double error correction .It also provides higher tolerance against large MCUs. However this research work succeeds in developing a better Error Correcting System with reduced delay area and power consumption. A

Pipelined MDMC reduces the time delay by carrying out multiple works at same time. Here the total work is divided into different levels. Each of these levels will function simultaneously and hence the total time required will reduce. This structure gives improvement not only in delay overhead but also in the area and power.

Future Scope:-

The study carried out in this paper can be extended to many other potential fields. Major possibility is to develop an error correcting system which can provide better performance, with less delay overhead, lower power requirements and less area consumption. The study can be carried out by pipelining the existing codes in to an efficient form so that the delay overhead is reduced. Also by changing the adders and other elements used in realization, the area can be reduced, by the proper implementation of the above indicated two ideas the power consideration can also be considerably reduced. Also by adapting some ideas or methods from other papers and by merging them, a better pipeline structure can be developed.

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