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*RESEARCH ARTICLE*

# ANALYTICAL MODELING OF COST EFFICIENT QUAD MATERIAL GATE ALL AROUND STACK ARCHITECTURE OF TUNNEL FET.

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## *Abstract*

Increase in speed is achieved by shrinking the dimensions of MOSFET's. But scaling of parameters leads to short channel effects which degrade the device performance. The predominating problems associated with SCE's are change in threshold voltage, drain-induced barrier lowering (DIBL) and sub threshold leakage current. SCE's causes degradation of sub threshold slope and increase in drain off-current.

Among the different possible solutions, TFETs are chosen to be the potential candidate because of its immunity against the SCEs, low leakage current and CMOS compatible technology.

In order to incorporate the advantages of Surrounding Gate (SG), Quad Material Gate (QMG), Gate Stack Architecture (GSA) and Tunnel Field Effect Transistor (TFET), novel device architecture has been proposed known as Quad Material Gate All around Stack Architecture - Tunnel Field Effect Transistor (QMGAASA- TFET).

Materials used:

Oxide1: TiO2 (Titanium dioxide) Oxide2: HfO2 (Hafnium dioxide)
Oxide3: SiO2 (Silicon dioxide) Oxide4: ZrO2 (Zirconium dioxide)
Metal1: Gold Metal2: Silver
Metal3: Aluminum Metal4: Copper



## Introduction:-

The **Tunnel Field-Effect** transistor (TFET) is a new type of transistor. Even though its structure is very similar to a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), the fundamental switching mechanism differs, making this device a promising candidate for low energy electronics. TFETs switch by modulating quantum tunneling through a barrier instead of modulating thermionic emission over a barrier as in traditional MOSFETs.

The field-effect transistor was first patented by Julius Edgar Lilienfeld in 1926 and by Oskar Heil in 1934.The **field-effect transistor** (**FET**) is a transistor that uses an electric field to control the shape and hence the electrical conductivity of a channel of one type of charge carrier in a semiconductor material. FETs are also known as **unipolar transistors** and as they involve single-carrier-type operation. The FET has high input impedance.

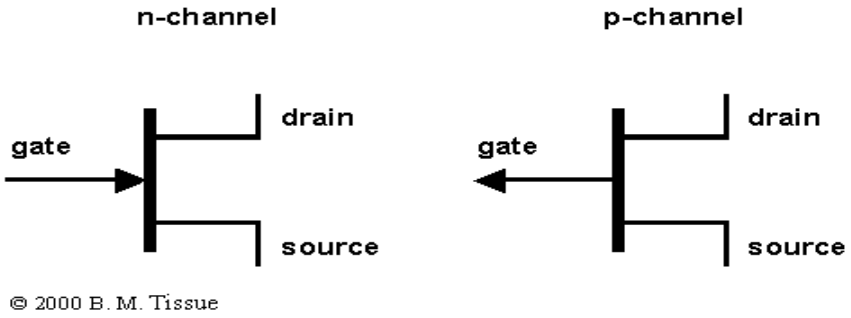


**Fig 1: - Symbols for n-channel and p-channel FET**

This fourth terminal serves to bias the transistor into operation. The device consists of an active channel through which charge carriers, electrons or holes, flow from the source to the drain. The conductivity of the channel is a function of the potential applied across the gate and source terminals.

**Types:-**

The channel of a FET is doped to produce either an n-type semiconductor or a p-type semiconductor. The drain and source may be doped of opposite type to the channel, in the case of enhancement mode FETs, or doped of similar type to the channel as in depletion mode FETs. Field-effect transistors are also distinguished by the method of insulation between channel and gate. Types of FETs include:

- The **JFET** (junction field-effect transistor) uses a reverse biased p–n junction to separate the gate from the body.
- The **MOSFET** (metal–oxide–semiconductor field-effect transistor) utilizes an insulator (typically $SiO_2$) between the gate and the body.

## Operation of fet:-

With no external Gate voltage (VG = 0), and a small voltage (VDS) applied between the Drain and the Source, maximum saturation current (IDSS) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions.

If a small negative voltage ( $-V_{GS}$ ) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of "squeezing" effect takes place. So by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel.

Since the PN-junction is reverse biased, little current will flow into the gate connection. As the Gate voltage ( $-V_{GS}$ ) is made more negative, the width of the channel decreases until no more current flows between the Drain and the Source and the FET is said to be "pinched-off" (similar to the cut-off region for a BJT).

It is essential that the Gate voltage is never positive since if it is all the channel current will flow to the Gate and not to the Source, the result is damage to the JFET.

The characteristics curves example shown above shows the four different regions of operation for a JFET and these are given as:

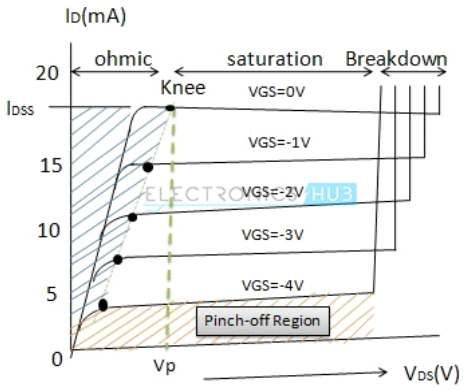


**Fig2:- V-I characteristics of FET**

- **Ohmic Region** – When $V_{GS}$ = 0 the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.
- **Cut-off Region** – This is also known as the pinch-off region were the Gate voltage, $V_{GS}$ is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- **Saturation or Active Region** – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (VGS) while the Drain-Source voltage, (VDS) has little or no effect.
- **Breakdown Region** – The voltage between the Drain and the Source, (VDS) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

## Structure of tfet:

The basic TFET structure is similar to a MOSFET except that the source and drain terminals of a TFET are doped of opposite type (see figure).

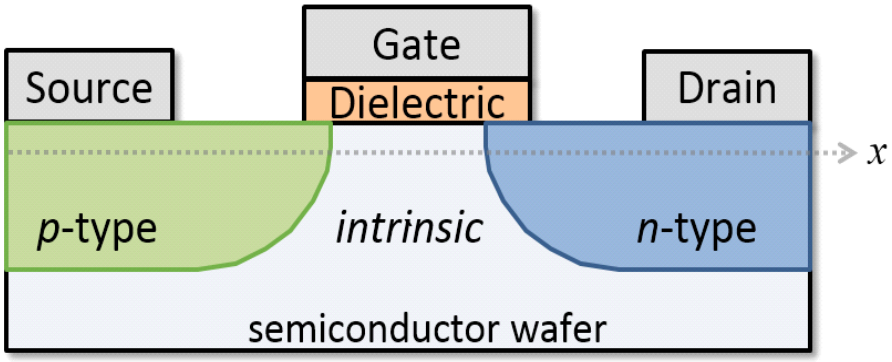


**Fig3: TFET Structure**

**Symbol of TFET:**

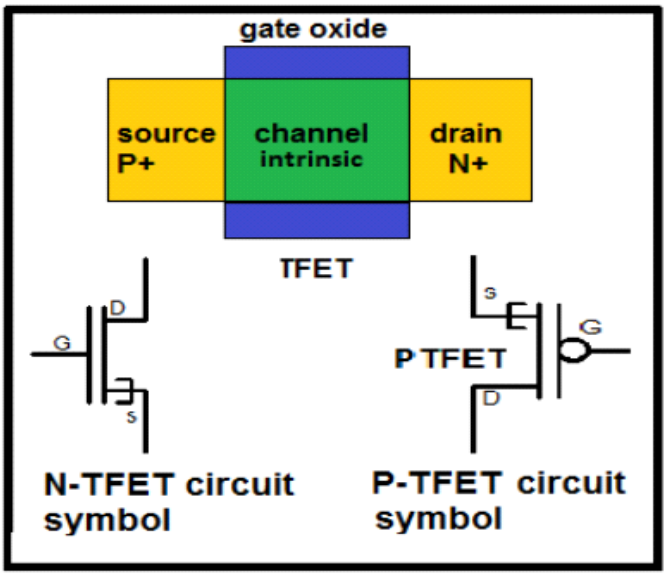


**Fig4: Symbol of N-TFET and P-TFET**

## Device operation:-

The device is operated by applying gate bias so that electron accumulation occurs in the intrinsic region. At sufficient gate bias, band-to-band tunneling (BTBT) occurs when the Conduction band of the intrinsic region aligns with the valence band of the P region. Electrons from the valence band of the p-type region tunnel into the conduction band of the intrinsic region and current can flow across the device. As the gate bias is reduced, the bands become misaligned and current can no longer flow.

### 5.1 BAND-TO BAND TUNNELING:-

Tunneling is a quantum mechanical process where electrons move through potential energy barriers. Band-to-band tunneling is the effect when electrons travel from the valence band to the conduction band (or vice versa) through the forbidden energy band gap.

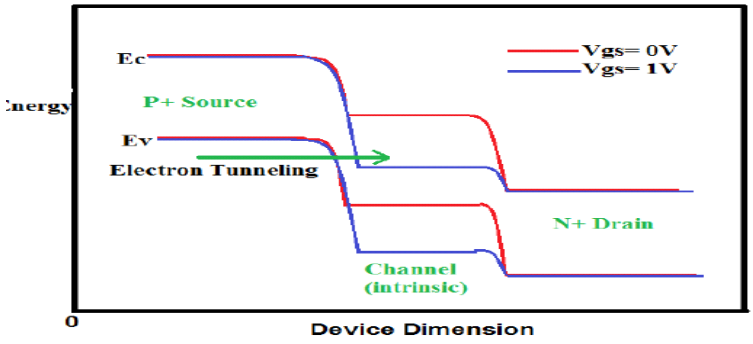


**Fig5: Energy band diagram showing band to band tunneling**

## Types of tfet's:-

Below device structures of Silicon based double gate N-channel TFET and P-channel TFET with a body thickness of 7 nm. This are called P+- I - N+ structure. The dielectric medium for the gate can be SiO2 (relative permittivity, = $\epsilon_r$ =3.9) or HfO2 (Hafnium Oxide) ($\epsilon_r$ = 21). The HfO2dielectric used in this case has a thickness of 1 nm and the channel length of the device is 30 nm for both the structures. The source and drain are heavily doped regions with channel being intrinsic. The N-type TFET consist of a source region which is P+ and has a boron doping

concentration of 1x1020cm−3. The N+ drain region has a phosphorus doping concentration of 1x1020cm−3. Similarly, the-type TFET consists of N+ source region doped with phosphorus doping con-cent ration of 1x1020cm−3. It's P+drain region has a boron doping concentration of 1x1020cm−3.

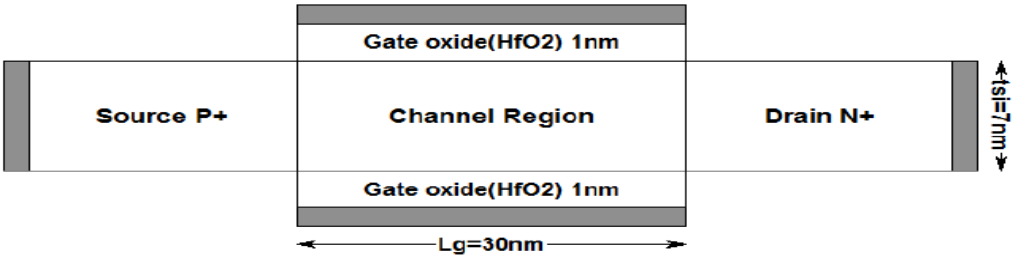


**Fig6: Cross sectional view of N-type TFET**

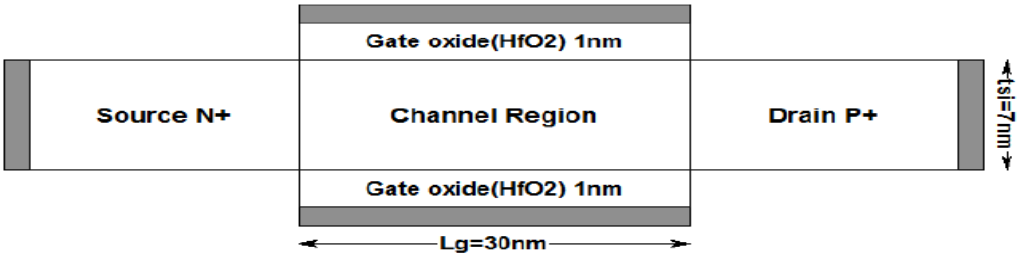


**Fig7: Cross sectional view of P-type TFET**

## CONSTRUCTION OF QMGAASA TUNNEL FET:-

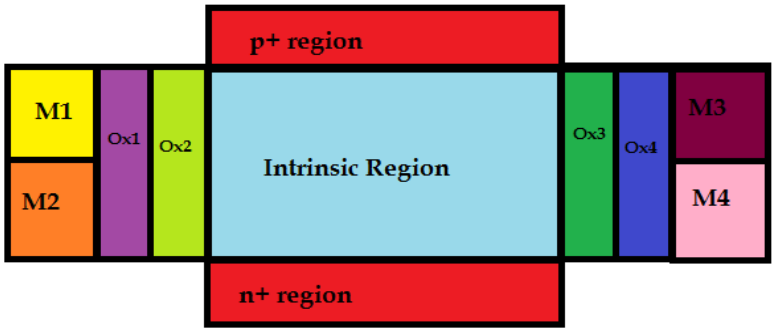


**Fig 8: QMGAASA TUNNEL FET**

TFETs are chosen to be the potential candidate because of its immunity against the SCEs, low leakage current and CMOS compatible technology. Various device structures such as Double Gate, Pi Gate, Triple Gate, Omega Gate, Surrounding Gate, Gate Stack structures have been proposed to overcome the scaling limitations and to increase the device performance. Among these structures Surrounding Gate offers higher packing density, steep sub threshold characteristics and higher current drive.

Quad Material Gate Architecture has also been investigated as one of the possible solution for reducing short channel effects. In this design four different metal gate electrodes are used having different work functions. Due to this work function difference carrier transport efficiency is increased thereby suppressing the short channel effects. Steady downscaling of device dimensions leads to reduction in voltage level as well as the gate oxide thickness. This causes an increase in static power consumption, which can hamper the circuit operation. In order to overcome the above limitations intensive stress has been made for the use of four gate oxides among which two have high K dielectric value and the other two oxides have comparatively less dielectric value namely SiO2, HfO2, TiO2, ZrO2 to prevent direct tunneling leakage current. As we are using two high K dielectrics and two normal dielectric oxides the device is cost efficient. This new structure is called as Gate Stack Architecture.

In order to incorporate the advantages of Surrounding Gate (SG), Quad Material Gate (QMG), Gate Stack Architecture (GSA) and Tunnel Field Effect Transistor (TFET), novel device architecture has been proposed known as Quad Material Gate All around Stack Architecture - Tunnel Field Effect Transistor (QMGAASA- TFET). In this work, a 2-dimensional analytical model is presented to examine the impact of the structure on various device characteristics.

## RESULTS AND DISCUSSION:-

In the below mesh plot gives the 3-D view of the device. It shows how the device will look after it is designed.

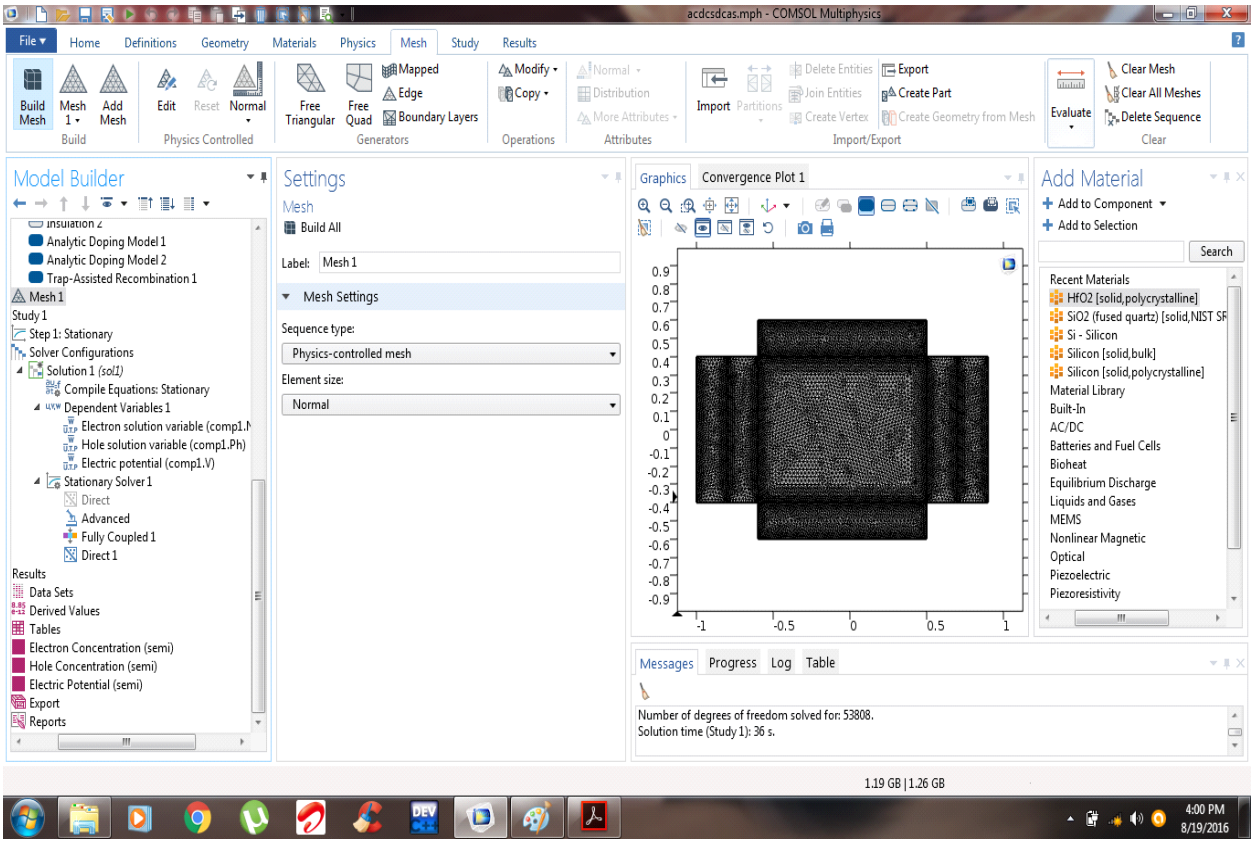


**Fig9:-** plot showing mesh for QMGAASA of TFET

The below plot shows how the electrons are distributed across the device. Different colors represent different levels of electron concentration distribution across the device

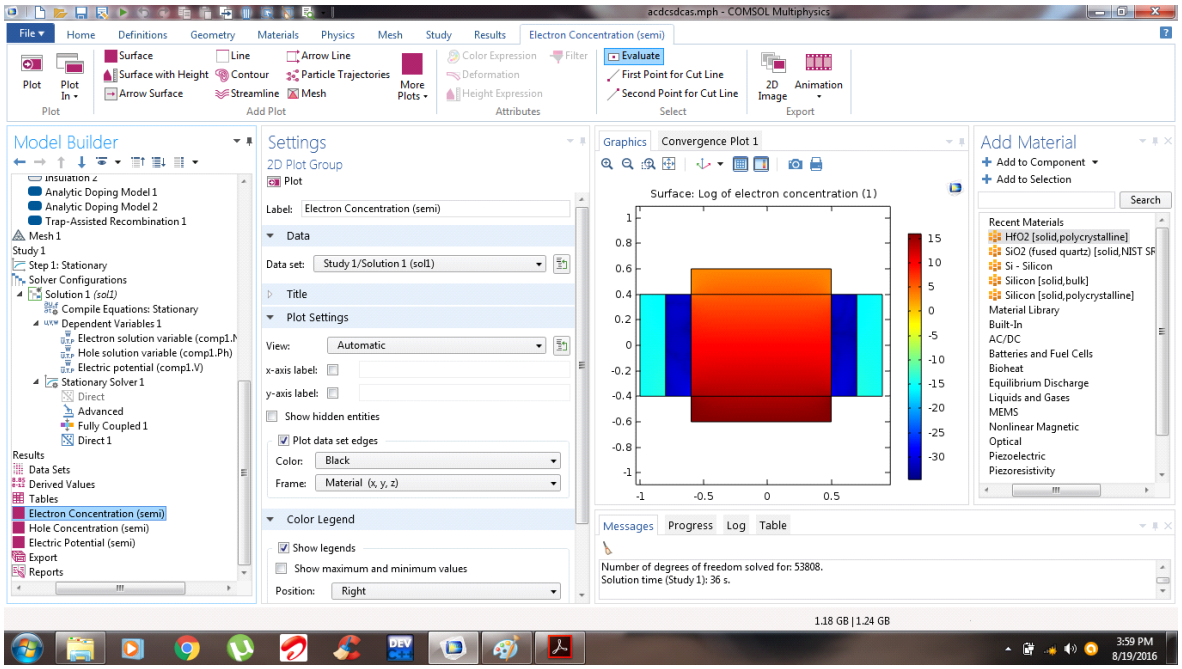


**Fig 10:-** Plot showing electron concentration of QMGAASA of TFET

The below plot shows how the holes are distributed across the device. Different colors represent different levels of hole concentration

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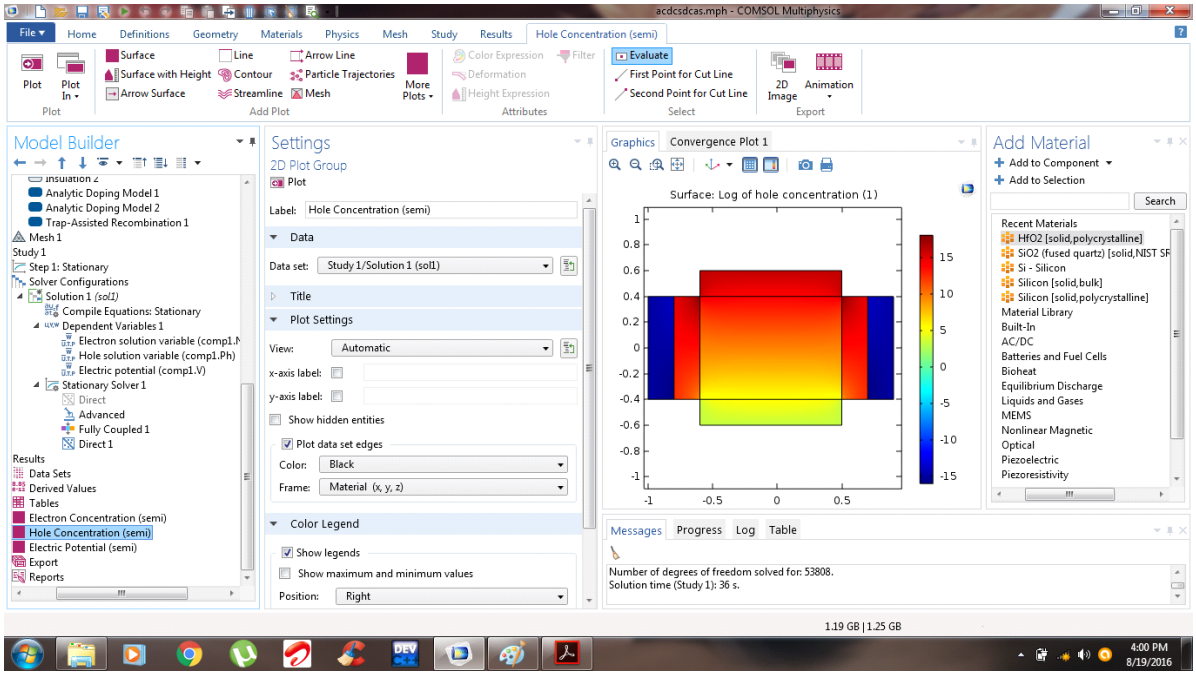


**Fig11: -** Plot showing hole concentration of QMGAASA of TFET

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**Final result**

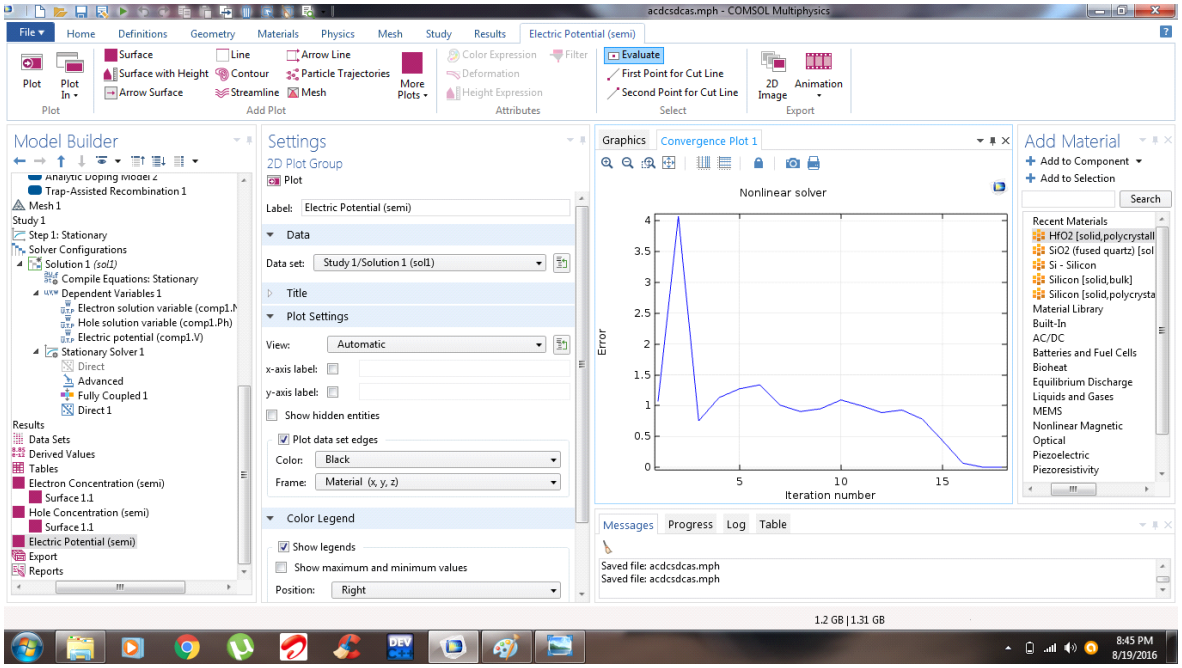


Fig 12. Plot showing electric potential of QMGAASA of TFET

## CONCLUSION:-

TFETs are used in digital circuit implementation due to their low sub-threshold loss and low voltage operation

It was observed that TFETs have steep sub-threshold swing (< 60 mV/decade) compared to MOSFETs which is the primary reason behind low sub-threshold power loss. The reason behind the steeper sub-threshold slope is band-to-band tunneling transmission. However, TFETs have a higher gate to drain capacitance compared to a MOSFET. For a 30 nm N type TFET it was observed that the Cgdequals 3.2 fF compared to a MOSFET which has 0.15 fF in saturation region. This results in higher overshoots during dynamic operation of gates.

A TFET based 6T-SRAM was implemented and verified using Cadence. The read and write operation was observed to be satisfactory.

Thus it has been demonstrated that incorporation of Quad Material Gate All Around electrode design along with Gate Stack Architecture leads to an improvement in short channel immunity and hot carrier reliability thereby ensures better carrier transport efficiency which results in better performance .

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