ISSN NO. 2320-5407

Journal homepage: http://www.journalijar.com
Journal DOI: 10.21474/IJAR01

INTERNATIONAL JOURNAL OF ADVANCED RESEARCH

RESEARCH ARTICLE

A REVIEW ON RECONFIGURABLE PROCESSOR FOR BINARY IMAGE PROCESSING.

Kishan Shivhare[1], Gaurav Bhardwaj[2].

1. PG Student, RJIT BSF Academy, Tekanpur (M.P.)
2. Asst. Prof., RJIT BSF Academy, Tekanpur (M.P.)

Manuscript Info

Manuscript History:

Received: 25 April 2016
Final Accepted: 19 May 2016
Published Online: June 2016

Key words:
Binary image processing, field-programmable gate array (FPGA), mathematical morphology, real time, mixed grained, reconfigurable.

Corresponding Author

Kishan Shivhare.

Abstract

An important tool which is used in image as well as video analysis is Binary image processing. Among various types of binary image processors, reconfigurable binary image processors are the most useful processors. This paper presents a review on reconfigurable processors for the Binary image processing techniques. The architecture of a binary image processor contains a reconfigurable binary processing module, input and output image control units and peripheral circuits. The reconfigurable binary processing module contains a mixed-grained reconfigurable binary compute unit and a output control logic. The reconfigurable binary processing module performs binary image processing operations, especially mathematical morphology operations and implements related algorithms more than 200 f/s for 1024 x 1024 image.

Introduction:-

Image processing is a type of signal processing where the input is an image, such as a photograph or video signal and the output of image processing may be an image or a set of characteristics or parameters related to the image. Binary image processing has been commonly implemented with the help of such processors like CPU or DSP. Binary image processing is a powerful tool and extremely used in various areas, such as object recognition, tracking, motion detection and machine intelligence, image analysis, video processing, computer vision, and identification & authentication systems.

By using specialized chips for binary image processing, high-speed implementation of binary image processing operations can be efficiently realized. Therefore, binary image processing module chips have attracted much more attention in the field of image processing. However, lack of flexibility is the major drawback of application-specific chips. The reconfigurable processing technique can bridge the gap between application-specific integrated circuits and flexibility.

A binary image processor which consists of a reconfigurable binary processing module, including reconfigurable binary compute units and output control logic, I/O image control units, and peripheral circuits. The reconfigurable binary compute units are of a mixed grained architecture. It has the characteristics of high flexibility, efficiency, and performance. By using the dynamic reconfiguration approach . the performance of the processor is enhanced. The processor is implemented to perform real time binary image processing. It is found that the pixel-level images can be processes by this processor and processor can extract image features, such as boundary and motion images. With the processor having the merit of high speed, simple structure, and wide application range, basic mathematical morphology operations and complicated algorithms can easily be implemented on it.

Literature review:-

Vision chip has attracted the attention of many researchers which provides properties such as compact size, high speed and low power consumption for performing parallel image processing. In today's life binary image processing system has been implemented using a processor such as CPU or DSP but these processors are inefficient and difficult for complex mathematical operation or algorithm of binary image processing. Therefore reconfigurable chips are used for binary image processing to achieve high speed implementation of binary image processing operations.

Application specific - chip (ASIP) and hardware have been proposed in various image processing application. To verify and enhanced fingerprint images this conventional chip with high resolution cellular logic processing array was developed and another application of a specific chip is motion detection using ModPod algorithm for simple operations. ASIPs are less flexible. Because of some problems, these chips are made up of analog circuit, and some are made of an analog part or digital part, while implementing analog part the results shows the low robustness, accuracy, small area and low power consumptions.

The general purpose processor chips are of digital processor array architecture, in which each processor handles one pixel only. The chip size totally depends on the size of the image. Therefore to design a chip with high speed, high performance and small size, a reconfigurable processor has been introduced for binary image processing using morphological operations.

Architecture:-

The processor we are currently using for binary image processing has been designed for applications in image or video processing, computer vision, machine intelligence, identification and authentication systems. These types of systems must contain a processor with high flexibility and high performance for wide applications; therefore, the processor design is focused mainly on high flexibility and speed. Some of the conventional works are designed for specific applications and some have large areas and high power consumption with many other disadvantages. Then, a reconfigurable binary processing module with high speed and simple structure is implemented in this task for wide use and consuming fewer resources provided.

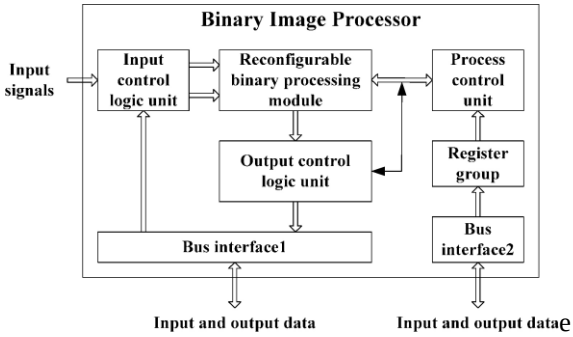

Fig. 1:- Architecture of the binary image processor.

The architecture of the proposed processor is shown in Fig. 1. It is showing the core of the processor is a reconfigurable binary processing module containing of binary compute units and output control logic. The processor also contains two bus interfaces, the I/O control logic units, the process control unit, and a configuration register group.

Reconfigurable binary processing module:-

The basic block diagram of the reconfigurable binary processing module (RBPM) is shown in Fig. 2. It can be divided into 2 parts. The first part is the output control logic, This selects the output from all the binary compute unit outputs with respect to the given parameters and converts the series data of 1-b binary images into parallel data.

Its second part contains many binary compute units which performs binary logic and binary image operations at a high speed. The operations in the individual binary compute units realize the binary image algorithms and the connection technique of these units. These units can execute binary image operations in a pipelined or parallel manner.

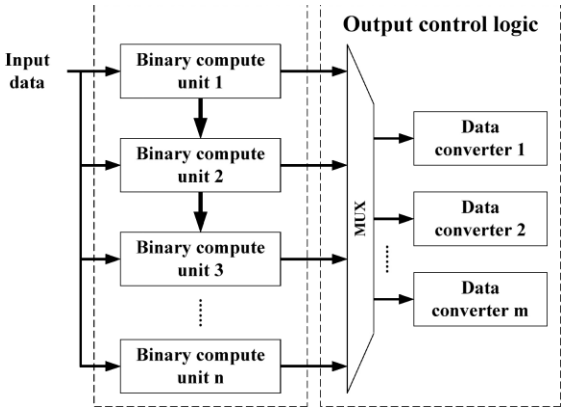

Fig. 2:- Diagram of a reconfigurable binary processing module.

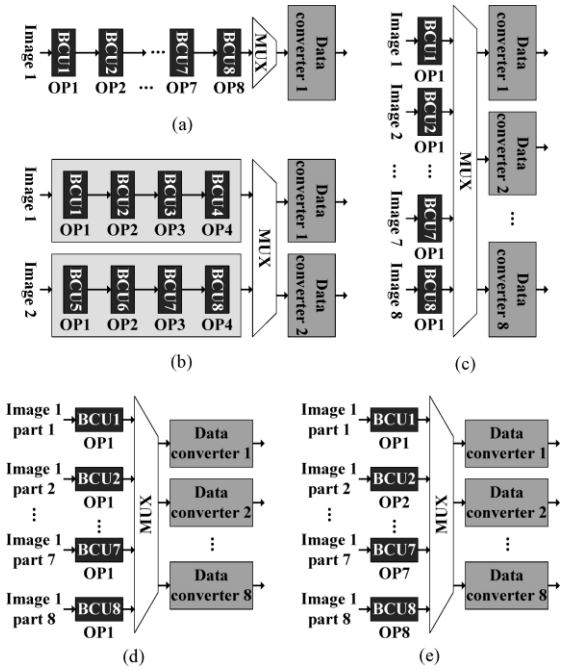

Fig.3:- Some examples of the reconfigurable binary processing module in pipelined manners.

The operation executed in a binary compute unit is operated by configurable registers, includes parameters of logic operation, image resolution, mask sizes, input and output selection, and auxiliary parameters.

Fig. 3 shows the reconfigurable working binary processing module with eight binary compute unit.. In Fig. 3(a), the RBPM is reconfigured to an eight-stage pipelined architecture. In Fig. 3(b), the RBPM is reconfigured to two four-stage pipelined architectures such that the two images can be processed simultaneously at a time. In Fig. 3(c)–(e), the RBPM are reconfigured in parallel structure. In Fig. 3(c), eight images undergo the same image processing operation in the same number of binary compute units, respectively. In Fig. 3(d), the same operation is performed on eight different parts of that image. In Fig. 3(e), eight different operations are performed on eight parts of an image. The reconfigurable architecture provides higher hardware utilization as compared to the pipelined architecture. For example, if one image just needs one operation, the pipelined architecture shown in Fig. 3(a) gives rise to low hardware utilization and it has less efficiency. The parallel architecture reconfigured, as shown in Fig. 3(d) can increase hardware utilization, and the process time is 1/8 that of the pipelined architecture, as shown in Fig. 3(a).

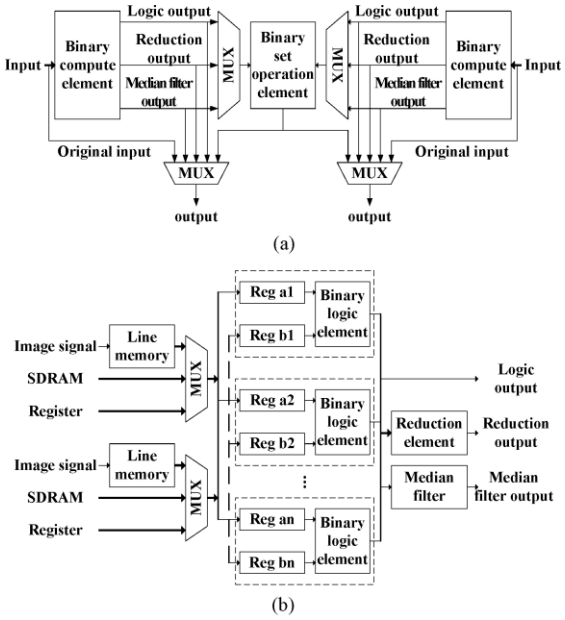

Fig. 4:- (a) Architecture of the binary compute unit.
(b) Architecture of the binary compute element.

The architecture of the binary compute unit and binary compute element is shown in Fig. 4. Each binary compute unit which contains two binary compute elements and one set of operation elements, can perform logic, reduction and median filtering. The binary compute unit has a mixed grained architecture which has high flexibility, efficiency, and performance, and short reconfiguration time. Usually, two types of granularity are distinguished: fine-grained corresponds to the bit-level manipulation of data, and coarse-grained, this corresponds to the word level. The fine-grained architecture has high flexibility, and the coarse-grained architecture has less reconfiguration parameters and high efficiency. The mixed-grained architecture has more flexibility and efficiency than the coarse-grained architecture, and has fewer reconfiguration parameters than the fine-grained architecture. The comparison of the fine-grained, coarse-grained, and mixed grained architectures of one binary compute unit is listed in Table I.

Table I:- Comparison of Fine-, Coarse-, and Mixed-grained architecture.

	Fine-grained	Coarse-grained	Mixed-grained
Hardware resource (ALUTs)	641	734	641
Flexibility	High	Low	Medium
Reconfiguration parameters (bits)	264	54	116

The set operation element can perform binary set operations, such as union, intersection, complement, subtraction, addition, and straight-through output. The two sets of multiplexers transmit the inputs of the set operation element and the outputs of the binary compute unit respectively, which makes the unit architecture more flexible. The inputs which transmitted to the set operation element through the multiplexers can be the operation results of the binary logic elements, the reduction result, and the median filtering result. The outputs of the binary compute unit which transmitted through multiplexers can be the original input of the binary compute unit and the results of operation of the binary logic elements, the reduction, the median filtering, and of the set operation element. The set element has a fine-grained architecture. The operands of the set element are 1 b; therefore, the set element has a 1-blogic block and shows high flexibility and efficiency.

The detailed architecture of the binary compute element is shown in Fig. 4(b). The binary compute element contains of two input control multiplexers, n binary logic elements, a binary reduction element, and a binary median filter. The input data is selected by multiplexer for the binary logic element from the line memories, the SDRAM, and the parameters in the register group. Line memories are needed to buffer image signals when a video image is processed before they become input to binary logic elements. When the block size of the image to be processed is nxn, n-1 line

memories with a depth equal to the image width are needed to buffer the image signals. The parameters in the register group or SDRAM selects the input data when images other than videos are processed. The binary logic element can perform AND, OR, NOT, NAND, NOR, XOR, XNOR operations and straight-through output. The reduction element performs operations such as reduction AND, reduction OR, reduction NAND, reduction NOR, reduction XOR, reduction XNOR, and straight through output. The set element performs operations such as union, intersection, complement, subtraction, and XOR. The binary logic elements results, the reduction element result, and the binary median filter results are synchronized and give output via multiplexers to the next binary compute unit. The binary compute element has a coarse-grained architecture featured by high performance and short reconfigurable time. The binary compute unit has the characteristic of programmability and configurability since the programmable logic is applied in the design of the binary logic element, reduction element and binary median filter in the binary compute element, the set element, and the multiplexers. In sum, the binary compute unit is appropriate for binary image processing due to its high performance, flexibility, and short configuration time.

Input and output control logic units:-

Before being input to the reconfigurable binary processing module, image signals need to be synchronized by the input control logic unit because one-to-one matching is needed between the pixels in different images. The inputs from video images, SDRAM, and registers are selected and synchronized by the input control logic unit to the synchronization circuit.

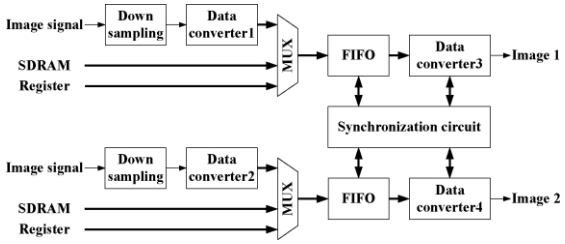

Fig. 5:- Block diagram of the input control logic unit.

Fig.5 shows the block diagram of the input control logic unit. The unit contains four data converters and a synchronization circuit. Data converters 1 and 2 convert 1-b image signals into 32-b parallel data of same format as the data from SDRAM and registers. Converters 3 and 4 convert the parallel data into 1-b image signals, which are then synchronized by the synchronization circuit. Two down sampling circuits are added to increase the processing rate, down-sample image signals before they are processed by the data converters 1 and 2. The output control logic unit writes the selected parallel image data from the reconfigurable binary processing module into SDRAM through the bus interface 1.

Process Control Unit and Configuration Register Group:-

The configuration information in the configuration registers is read by process control unit. The input and output control logic units and bus interfaces are controlled by this unit during data access. It also controls the operation process of the reconfigurable binary processing module. After the processed image data is written to SDRAM, the process control unit transmits interrupt requests to complete the interaction of the processor with external systems.

The configuration register group is an extremely important part in the proposed processor. It has control parameters, reconfiguration information, operation parameters, and interaction information. An external CPU writes in most of the registers in the configuration register group via the system bus, and the rest are written by the internal modules in the proposed processor.

Morphological operations:-

A powerful tool for image processing and analysis in a wide range of applications is mathematical morphology also used for shape recognition, image processing, video processing, document authentication, and computer vision.

Two basic binary morphological operations are dilation and erosion. Either of the two operations has two operands: the input signal, which is usually an image, and the structuring element characterized by its shape, size, and center location. The other binary morphological operations such as opening, closing, and hit-and-miss operation are based on various combinations of the two basic operations, dilation, and erosion.

Dilation:-
It generally enlarges the boundaries of regions of foreground pixels (i.e. white pixels, typically) by one pixel. Therefore the areas of foreground pixels grow in size and holes within those regions get smaller.

In other words, for each background (input) pixel, overlap the structuring element with the input image. If at least one pixel in the structuring element coincides with a foreground pixel in the image underneath, then the input pixel is set to the foreground value. If all the corresponding pixels in the image are background however, the input pixel is left at the background value.

The dilation of X by the structuring element K is defined by:

$$X \oplus K = \{ x \, [\, (K^{\wedge})x \cap X \,] \neq \emptyset \, \}$$

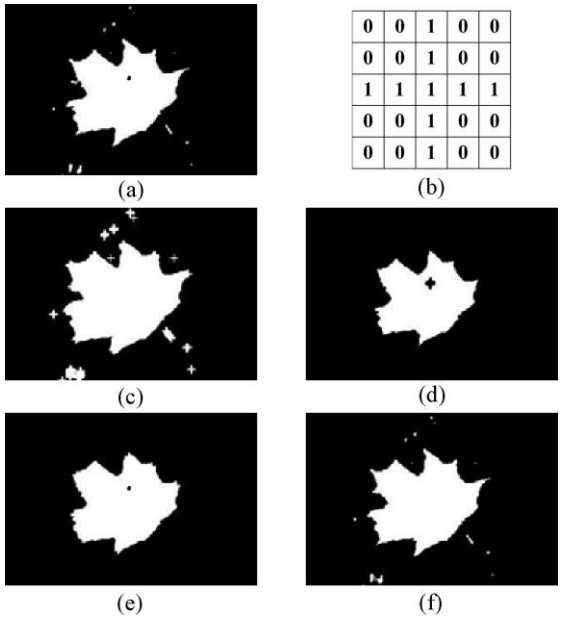

Fig. 10:- Binary image processing results. (a) Input image. (b) Structuring element. (c) Dilation. (d) Erosion. (e) Opening. (f) Closing.

Erosion:-
The eroding away of boundaries of regions of foreground (i.e. white pixels typically) is a basic effect of the operator on a binary image. Hence, shrink areas of foreground pixels in size and holes within those areas become larger.

That is, for each foreground (input) pixel, superimpose the structuring element with the input image. The input pixel is left as it is when it is the foreground pixel in the structuring element. If any of the corresponding pixels in the image are background however, the input pixel is also set to background value.

The erosion of the binary image X by the structuring element K is defined by:

$$X\Theta \; = \{ x \, [\, (K)_x \subseteq X \, \}$$

Where K_x is the translation of K by the vector x.

Opening:-
Erosion is followed by a dilation using the same structuring element for both operations.

Simply grey level opening consists of grey-level erosion followed by grey-level dilation. The opening of X by K is obtained by the erosion of X by K, followed by dilation of the resulting image by B:

$$X \circ K = X \Theta K \oplus K$$

Closing

The closing operation is nothing but the reverse of opening operation. It is defined as dilation followed by an erosion operation with the same structuring element, therefore it requires two inputs: an image to be closed and a structuring element. This can be defined by,

$$X \bullet K = X \oplus K \Theta K$$

Conclusion:-

The mixed grained architecture is used by binary reconfigurable processor which increases the performance of the processor. The mathematical morphological operations and algorithms can easily be implemented on Field Programmable Gate Array (FPGA). Thus using such morphological operations like Dilation, Erosion, Opening, Closing and Median filter, it is simple and easy to implement edge and motion detection morphological applications.

References:-

1. Bin Zhang, Kuizhi Mei and Nanning Zheng, (MAY 2013), ''Reconfigurable Processor for Binary Image Processing'', IEEE Transactions On Circuits And Systems For Video Technology.
2. W. Miao, Q. Lin, W. Zhang et al., "A programmable SIMD vision chip for real-time vision applications," IEEE J. Solid-State Circuits, vol. 43, no. 6, pp. 1470–1479, Jun. 2008.
3. A. Lopich and P. Dudek, "A SIMD cellular processor array vision chip with asynchronous processing capabilities," IEEE Trans. Circuits Syst. I, vol. 58, no. 10, pp. 2420–2431, Oct. 2011.
4. S. Chien and L. Chen, "Reconfigurable morphological image processing accelerator for video object segmentation," J. Signal Process. Syst., vol. 62, no. 1, pp. 77–96, 2011.
5. K. M. Shaaban, S. A. Ali, and Y. B. Mahdy, "A chip design for binary and binary morphological operations," in Proc. Int. Conf. Inform. Intell. Syst., 1999, pp. 554–559.
6. K. Fujii, M. Nakanishi, S. Shigematsuet al., "A 500-dpi cellular-logic processing array for fingerprint-image enhancement and verification," in Proc. IEEE Custom Integr. Circuits Conf.,May 2002, pp. 261–264.
7. H. J. Park, K. B. Kim, J. H. Kim et al., "A novel motion detection pointing device using a binary CMOS image sensor," in Proc. IEEE Int. Symp. Circuits Syst., May 2007, pp. 837–840.
8. R. Dominguez-Castro, S. Espejo,A. Rodriguez-Vazquez et al., "A 0.8-µm CMOS 2-D programmable mixed-signal focal-plane array processor With on-chip binary imaging and instructions storage," IEEE J. Solid- State Circuits, vol. 32, no. 7, pp.1013–1026, Jul. 1997.