RESEARCH ARTICLE

DESIGN OF A DEMULTIPLEXER USING DOUBLE BASED NUMBER SYSTEM

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Abstract

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This paper presents an innovative method for designing a double based demultiplexer. This demultiplexer is designed using binary number system combined with ternary number system. A binary demultiplexer selects one out of 2^n number of output lines and passes the single input to one out of 2^n number of output lines whereas a ternary demultiplexer selects one out of 3^m number of output lines and passes the single input to one out of 3^m number of output lines. We propose a double based demultiplexer that selects one out of $2^n \times 3^m$ number of output lines and passes the single input to one out of $2^n \times 3^m$ number of output lines.

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Introduction:-
The demultiplexer is a combinational logic circuit designed to switch one common input line to one of several output lines by the appliacation of a control signal. Demultiplexer is a circuit that has a single input line and more than a single output line. It is used when a circuit requires to send a signal to one of many devices.

It is well known that the binary numerical systems are used in most computers and some people consider about ternary number system also. This paper discusses the double based number system (2, 3), that is the combination of base 2 and base 3. Demultiplexers have been designed using base 2, but no literature could be found on demultiplexers developed by considering both bases together. Observing complexity of today's circuits, it is essential to improve circuits at higher than binary logic system. Therefore, design complexity of circuits can be reduced using higher number systems than binary number system.

Binary and Ternary Digits and Logic Gates:
In this section, binary and ternary digits, physical implementation, and binary and ternary logic gates are discussed.

Binary and Ternary Digits:
0 and 1, are entitled binary digits in binary number system. In Boolean logic (two valued logic), 0 is reflected as false and 1 as true. 0, 1 and 2, are entitled ternary digits in ternary number system. Three valued logic is an extension of two valued logic. In three valued logic 1 is concerned as True, 0 is concerned as False while, 2 is concerned as Unknown. Here, Unknown means 'undefined', 'neither' or both True and False.

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Before ternary digit operation, binary digit operation should be considered. In logic, bit 1 intends 3.3 voltage and 0 intends zero voltage while in ternary digit operation bit 1 intends 3.3 voltage, 0 intends zero voltage and 2 intends -3.3 voltage.

Binary and Ternary Logic Gates:
A logic gate is an idealized or physical device implementing a Boolean function, that is, it performs a logical operation on one or more logic inputs and produces a single logic output[5].

In demultiplexer design, NOT gate, AND gate and OR gate are mainly concerned in the case of binary and ternary logic gates. In binary logic gates, the truth value of NOT gate is defined as complement of input, truth value of AND gate is defined as product of inputs of truth values and truth value of OR gate is defined as maximum of inputs of truth values.

In ternary logic gates, truth value of AND gate is defined as minimum of inputs of truth values, truth value of OR gate is defined as maximum of inputs of truth values and truth value of NOT gate is defined as cyclical transformation of input. Since there are several non-cyclical ways to define truth value of NOT gate, according to cyclical and non-cyclical ways, different double based demultiplexers can be implemented.

Designing Double Based Demultiplexer:
In this design, we have first desingned BinaryTernary AND gate and BinaryTernary OR gate considering binary and ternary logic gates. Binary NOT gate and ternary NOT gate have been used in this design. $1 \times 2^n 3^m$ demultiplexer has been designed using BinaryTernary AND gates, binary NOT gates and ternary NOT gates.

Binary gates:
In this design, binary NOT gate has been used and $\mathcal{B}$ symbolizes binary NOT gate. Figure 1 shows binary NOT gate and truth values of binary NOT gate is given in Table 1.
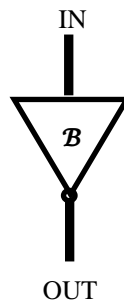
IN

$\mathcal{B}$

OUT

Figure 1:- Binary NOT gate

Tabel 1:-Truth table of binary NOT gate.

IN	OUT
A	**$\bar{A}$**
0	1
1	0

Design of Ternary gates:
Ternary NOT gate has been used here. $\mathcal{T}$ symbolizes ternary gates. Figure 2 shows cyclic transformation of input system and truth values of ternary NOT gate is given in Table 2.
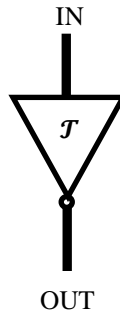
IN

OUT

Figure 2:- Ternary NOT gate

According to cyclic or non-cylic nature of the ternary NOT gate, different double based multiplexers can be desinged, but here cyclical transformation of input system has been considered (Figure 3).
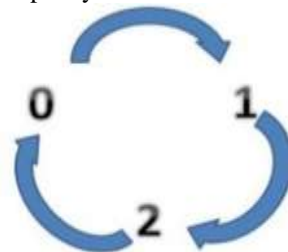
0   1

2

Figure 3:- Cyclical transformation of input system

Table 2:- Truth table of ternary NOT gate.

Input	Cyclical transformation of B	Cyclical transformation of $\tilde{B}$	Cyclical transformation of $\tilde{\tilde{B}}$
B	$\tilde{B}$	$\tilde{\tilde{B}}$	$\tilde{\tilde{\tilde{B}}}$
0	1	2	0
1	2	0	1
2	0	1	2

Design of Double Based gates:
In this design, function of AND and OR gates are switched. Output of the BinaryTernary (Double Based) AND gate is always the maximum of the inputs (Table 3), whereas output of the BinaryTernary (Double Based) OR gate is always the minimum of the inputs (Table 4). $\mathcal{BT}$ symbolizes the BinaryTernary (Double Based) gates[1].
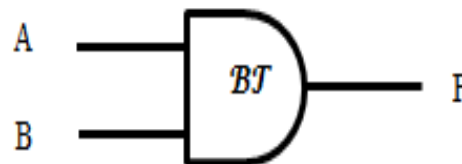
A

B $\mathcal{BT}$ F

Figure 4:- BinaryTernary AND gate.

Table 3:- Truth table of BinaryTeranary AND gate.

A	B	F=Max(A,B)
0	0	0
0	1	1
0	2	2
1	0	1
1	1	1
1	2	2
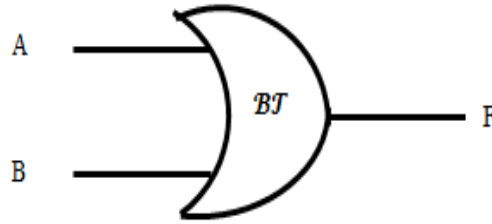
Figure 5:- BinaryTernary OR gate.

Table 4: Truth table of BinaryTernary OR gate.

A	B	F=Min(A,B)
0	0	0
0	1	0
0	2	0
1	0	0
1	1	1
1	2	1

Block diagram of $1 \times 2^n 3^m$ Demultiplexer:

The block diagram shown in Figure 6 gives an overview of how many outputs and selection lines have been used in designing the 1×6 demultiplexer. Different combinations of selection lines enable different outputs. Table 5 shows the different values of selection lines and what outputs are enabled in this double based demultiplexer. It consists of a single input and six outputs. According to selection lines, one of six outputs is enabled to pass the input.
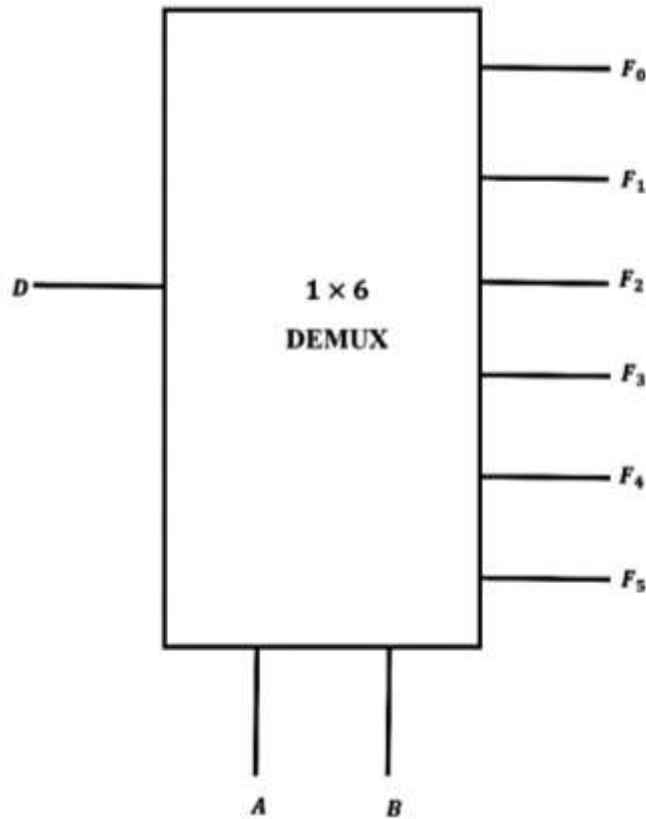

Figure 6:- Block diagram of 1×6 Demultiplexer.

Table 5:- Truth tabel of 1×6 Demultiplexer.

Input		Output					
A	**B**	F_0	F_1	F_2	F_3	F_4	F_5
0	0	D	0	0	0	0	0
0	1	0	D	0	0	0	0
0	2	0	0	D	0	0	0
1	0	0	0	0	D	0	0
1	1	0	0	0	0	D	0
1	2	0	0	0	0	0	D

Design of 1×6 Demultiplexer:
In this design, six BinaryTernary AND gates, two ternary NOT gates, and one binary NOT gate have been used. There are six outputs named F_0, F_1, F_2, F_3, F_4 and F_5. According to the values of two selection lines A and B, one output is enabled (Figure 7). There is a single input labeled D. According to the values of two selection lines A and B, input D selects one of the outputs.
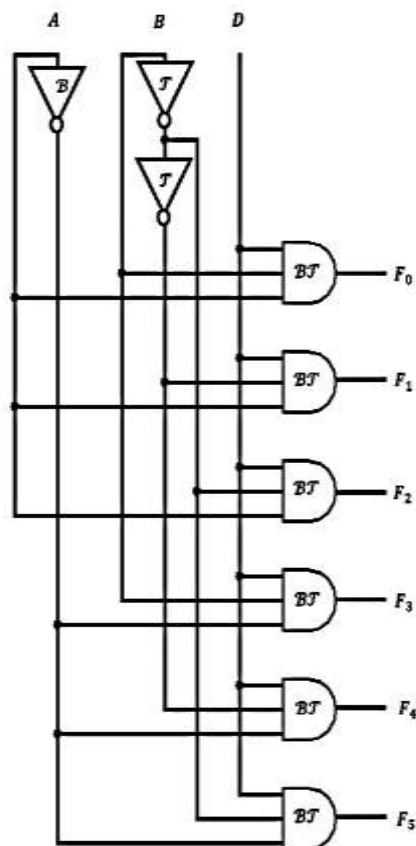
Figure 7:- Design of 1×6 Demultiplexer.

Conclusion:-
A new design of a device can be implemented by combining two different logics, two valued logic and three valued logic. Reduction of power consumption of the device is also important. Using the same number of selection lines, different number of outputs can be implemented.

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