Journal Homepage: - www.journalijar.com
INTERNATIONAL JOURNAL OF ADVANCED RESEARCH (IJAR)
Article DOI:10.21474/IJAR01/4898
DOI URL: http://dx.doi.org/10.21474/IJAR01/4898
ISSN NO. 2320-5407

RESEARCH ARTICLE

AN IN-SITU TIMING-ERROR PREDICTION AND PREVENTION TECHNIQUE FOR VARIATION-TOLERANT MAC-UNIT.

Jasmer Singh[1], Saha K[2] and GL Pahuja[1].
1. Electrical Engineering Department, N.I.T. Kurukshetra, India.
2. IIT-Delhi, New Delhi.

Manuscript Info

Manuscript History

Received: 20 May 2017
Final Accepted: 22 June 2017
Published: July 2017

Key words:-
Dynamic Threshold Voltage V_{th} Scaling (DVTS), Dynamic Voltage Scaling (DVS) and Dynamic Voltage and Frequency Scaling (DVFS), Razor flip- flop, CANARY flip-flop, error prediction, error prevention.

Abstract

In this paper, a CANARY based Dynamic Voltage Scaling (DVS) technique is applied on a 17-bit Multiplier Accumulator (MAC) Unit in 0.55- nm technology to critically analyze the voltage safety margins and energy efficiency during the worst case of Process, Voltage and Temperature (PVT) conditions. The CANARY based DVS technique incorporates an inherent *in situ* error prediction feature, with a mechanism to prevent the errors to impact the Design under Test (DUT). In CANARY based DVS technique, the supply voltage is reduced automatically. Error prediction and prevention mechanism ensures correct operation and lesser voltage supply. Supply voltage is intentionally scaled down till the first failure point of MAC unit to reach at an optimal tradeoff [17] between voltage supply and energy consumption. It is observed from the simulation results that the energy savings up to 38.5% is achieved with CANARY based adaptive DVS as compared to classical DVS technique over the wide spectrum of functional frequency range. The SPICE platform is used for the detailed analysis and step by step implementation of CANARY based DVS technique.

Introduction:-

In deep submicron Integrated Circuits (IC) technologies, process-induced parameter variations cause performance fluctuations, which is an important challenge to be addressed. Due to this, the traditional worst-case methodology of design is no more effective as process variations require more design margins. To deal with this problem, the prediction of parameter variations can play a vital role in manufacturability of silicon devices [1, 2, 3]. Lower technology nodes are setting a trend of lowering supply-voltage and tremendous increase in clock frequency. These changes of voltage and temperature variations make the design more and more tedious. To achieve a robust design along with above discussed constraints, designers are focusing on Design for Manufacturability (DFM), which is a key to solve these serious problems. As the worst cases rarely occur, so it is always better for the designers to focus on typical cases, called as typical-case design methodology. In recent time, different typical-case design methodologies are proposed, such as Razor circuit [4-5], Canary circuit [12], approximation-circuits [6], Algorithmic Noise Tolerance (ANT) [9], Constructive Timing Violation (CTV) [7], TEA time [10] etc. This paper, focuses on the Canary based DVS technique to critically analyze the voltage safety margins and energy efficiency during, worst case PVT conditions.

Corresponding Author:-Jasmer Singh.
Address:- **NIT Kurukshetra**, Kurukshetra, Haryana, India.

As out of these techniques some compromises with throughput of the system like approximation, CTV, some techniques like ANT is highly dependent on EDA. Techniques like Razor and CANARY are error correction and detection based where Razor technique results in circuit overhead for re-execution. So we have adopted here the Canary technique just to focus on power reduction without any overhead or compromise in throughput.

Explosive, exceptional and exhilarating kind of growth is observed in semiconductor and computational operations, which is carried out by Digital Signal Processing (DSP). In a DSP, the computational operations are threaded through some mathematical algorithms of different forms. These operations are processed with the help of different kind of normal or application specific MAC units. The Block diagram of a classical DSP is presented [13] in Fig. 1.

Being a main stream unit of processing, the MAC unit performs, most of the time, at maximum throughput as per amount of data processed per unit time. Moreover, in handy systems, the MAC units are expected to consume high power and as a result of it the MAC unit governs the speed and power of the system. The most efficient MAC utilization in terms of power and speed depends upon the technology chosen, its characterization, architecture type, its fundamental blocks and primitive cell realization.

In this paper, a CANARY based DVS technique is applied on a 17-bit Multiplier Accumulator (MAC) unit in 0.55-nm technology to critically analyze the voltage safety margins [8] and energy efficiency during, worst case PVT conditions. The performance of CANARY based DVS technique is also compared with classical design technique over the wide spectrum of frequency range. The comparative analysis is based on some constant supply-voltage versus adaptively varying supply-voltage to enhance the speed and performance whenever required. This study will help researchers to adopt some new technologies and techniques, while designing a suitable MAC block for any Application Specific Integrated Circuit (ASIC) in signal processing applications.

The Mac Unit:-

Generally, the architecture of a MAC unit is classified as parallel [14], recursive [15] and shared segmented structure. The architecture named as recursive, is based on "divide and conquer" methodology. Larger data is divided into smaller ones to be processed by individual units.

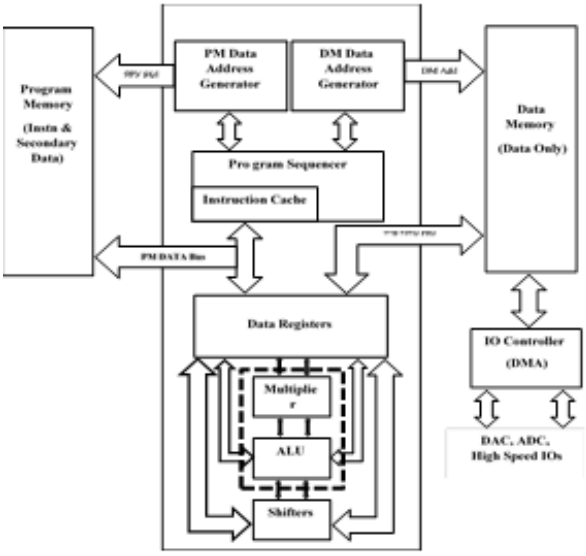


Fig. 1:- Classical DSP Processor Architecture.

In MAC unit, the multiply-accumulation is an iterative calculation process performed by smaller units through several cycles. The number of multipliers and adders called recursively are responsible for latency and throughput of the complete MAC unit. Ideally, the MAC unit operation can be understood in four phases like:

Data to be processed, fetched from internal memory

- Multiplication is performed
- Summation is performed

- Performed A.B + Acc, stored in the internal memory.

Hence, the function of MAC unit can be understood well from the arithmetic relation mentioned in equation (1):

$$\text{MAC OUTPUT} = A_1.B_1 + A_2.B_2 + A_3.B_3 + \ldots + A_n.B_n \ldots. (1)$$

Where A, B are the multiplicand and multiplier respectively. The 'n' is the numbers of pairs to be multiplied and accumulated.

MAC Architecture:-

Fig. 2 shows a typical MAC architecture in detail. There are two inputs, multiplicand and multiplier of some bit widths. The width of the MAC final output is defined by the width of

$$Y = X1 + X2 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

$$Z = Y + 1 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

inputs and is defined by equations (2) and (3) and also presented in Fig. 2. This extra bit for 'Z' is always needed and is named as Guard Bits, also named as Extension Bits, which is essentially required for more robust design. Being a main stream and most critical unit of processing, the MAC unit is adopted as the most suitable module to analyze and study the effectiveness of the adaptive supply-voltage system.

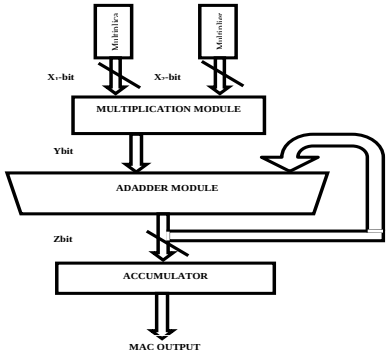


Fig. 2:- MAC Architecture.

The MAC Design:-

The complete details of the MAC unit under observation are shown in Fig. 3 and its pin details are depicted in Table 1.

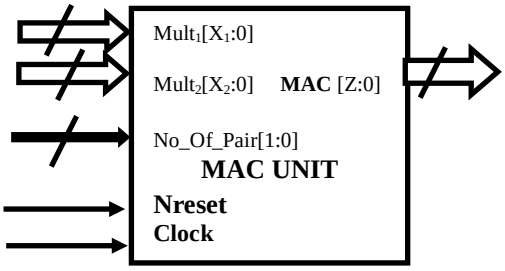


Fig. 3:- MAC Unit Pin Diagram

Three Guard / Extension Bits are kept to avoid overflow of the MAC output as presented in equation (4):

$$Z = (X_1 + X_2) + 3 \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Table 1:- MAC Unit Pin Description

Pin Name	Direction	Function
Mult1	Input	Multiplicand
Mult2	Input	Multiplier
No_Of_Pair	Input	Number of Pairs
Nreset	Input	Reset of the Module
Clock	Input	Clock Signal
MAC	Output	Multiplied and Accumulated Output

In this work the MAC unity is designed and developed in Verilog RTL and the functionality of RTL and synthesized netlist is verified through simulations. In the next sections of the paper, the development, integration and analysis of the system are given in details. It also shares the variation of results in terms of power efficiency and functional range of MAC unit, w.r.t., the system without DVS sub-system.

The CANARY Integration:-

To getridof the worst case margin, the Flip-Flops of MAC are paired with CANARY Flip-Flop [12, 16] as per shown inFig.4. Input of the CANARY Flip-Flop is delayed little more with a delay cell. Output of Main Flip-Flop and of respective CANARY flip-flop which is compared through XOR gate as comparator logic, output of XOR gate is named as WARN or Error Signal.

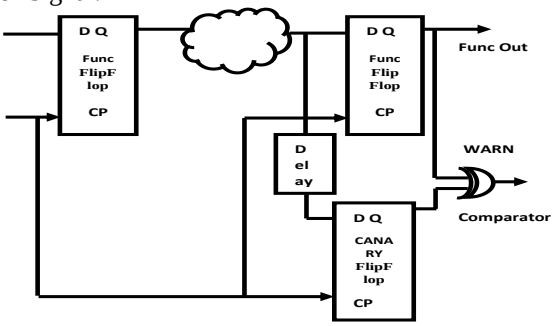


Fig. 4:- CANARY Module Integration.

This is connected to the Monitor and Voltage Control unit as an input. There are different type of errors [11] presented from time to time but this is hardware generated comparative error.

Adaptive DVS System Architecture:-

The CANARY integrated MAC unit is integrated in In-Situ Adaptive DVS sub-system as presented in Fig. 5 with the help of block diagram [4, 18]. Different supply-voltages are applied to the active supply-voltage block which acts as per the instruction of Units 'Supply Select & Timer' and 'Monitor and Voltage Control', respectively. Unit Monitor and Voltage Control reacts as per the output WARN/Error, of CANARY comparator unit.

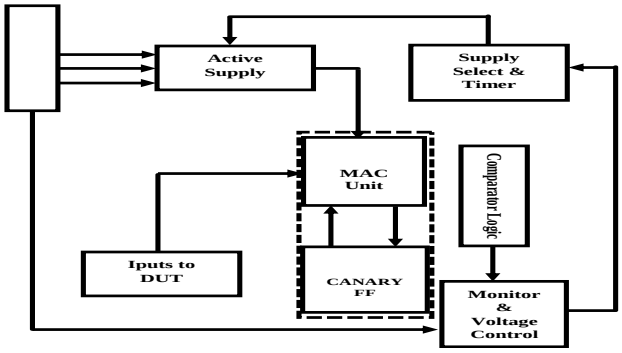


Fig. 5:- Adaptive DVS Sub-System Block Diagram

The complete sub-system [18] as shown in Fig.5 is a kind of closed loop feedback system, where the system reacts on the error prediction mechanism of CANARY module and completes the loop by adjusting the supply-voltage adaptively. As per the block diagram, it is clear that 'Supply Select & Timer' and 'Monitor and Voltage Control' units play a vital role in the complete sub-system. In the upcoming sections, these units are described in detail.

Monitor and Voltage Control Unit:-

The 'Monitor and Voltage Control' unit decides about stepping up/down the supply-voltage adaptively, to avoid any assertion of Error/WARN signal by CANARY cell. This unit is realized with the help of state machine, where numbers of states are directly proportional to the number of quantized supply-voltages. In this work we have quantized the supply-voltage in eight levels with constant difference of 100mV.

Accordingly, eight different states are shown in the state diagram in Fig. 6 and are also depicted in Table 2 in detail.

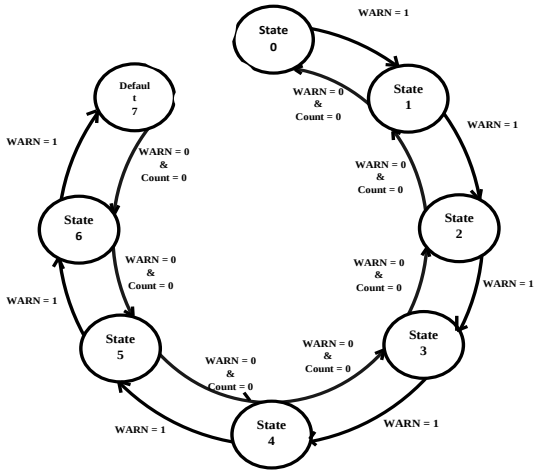


Fig. 6:- State Machine of Monitor and Voltage Control Unit

On releasing the reset of the system, this unit starts with State7 with highest voltage level and adaptively resumes the consecutive state as per the WARN / Error signal activated by CANARY module. Once there is no WARN / Error signal asserted, this unit adaptively switches to the lower state to step down the supply-voltage. On the other side, if there is any WARN / Error signal asserted by CANARY module, system resumes the next respective state to step-up the supply-voltage. As it is the most critical part of the sub-system, this unit is always connected to the highest available voltage level.

Table 2:- Monitor and Voltage Control Unit States.

State	Active Supply-Voltage
$State_0$	**2.6 Volt**
$State_1$	**2.7 Volt**
$State_2$	**2.8 Volt**
$State_3$	**2.9 Volt**
$State_4$	**3.0 Volt**
$State_5$	**3.1 Volt**
$State_6$	**3.2 Volt**
$State_7$(Default)	**3.3 Volt**

The Supply Unit:-

There are eight different voltage supplies starting from 2.6 Volt till 3.3Volt. Practically, we need an accurate voltage regulator to supply this kinds of supply-voltage, but this is beyond the scope of this study, so we have used here the digitalized version of voltage regulator, implemented by pass gates switches, as shown in Fig. 7.

Fig. 6:- Supply Unit

Signals $Active\_Supply_0$, $Active\_Supply_1$ …… $Active\_Supply_7$ are controlled by Monitor and Voltage Control unit through its respective states and accordingly that supply-voltage will be available at Pin V_{DD}.

The Sub-System Integration:-

The MAC unit Verilog netlist with CANARY flip-flop paired at each MAC unit critical path capture side Flip-Flop is created. Monitor and Voltage Control unit Verilog netlist is integrated with MAC unit netlist and the integrated netlist is streamed in Virtuoso to get the transistor level SPICE netlist. The other units like supply voltages unit and all are also integrated to the schematic and a complete sub-system are integrated as per schematic shown in Fig. 8.

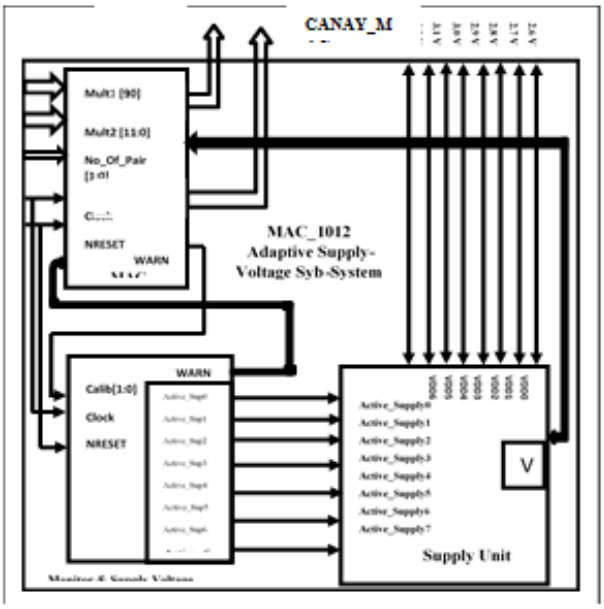


Fig 8:-Adaptive DVS Architecture

The System And Simulation Statistics:-

The complete MAC Unit statistics and simulation scenarios are summarized in Table 3 and 5, respectively. The light corners are chosen for MAC unit without the CANARY technique but the complete adaptive system with CANARY technique is simulated over the complete range of Supply-Voltage and Temperature mentioned in Table 5.

Table 3:- MAC Unit Statistics

Inputs	**Signal Name**	**Bus Width**	**Simulation Input Status**
	Mult1	10-Bits	10'b01_0101_0101= 341
	Mult2	12-Bits	12'b01_0101_0101= 341
	No_Of_Pair	2-Bits	2'b00
Outputs	**MAC [24:0] =116281, 232562, 348843, 465124, ……**		
Inst. Count	28.43K		
Area Ratio	8.4% (Monitor & Voltage Control Unit v/s MAC Unit)		

Spice Simulation Results:-

In this section of the paper the simulation results of the MAC unit without adaptive technique and afterwards the simulation results of the MAC unit with adaptive technique are discussed.

Table 4:- Simulation Corners

Temp	**-40 ^{O}C**	**0 ^{O}C**	**27 ^{O}C**	**50 ^{O}C**	**75 ^{O}C**	**100 ^{O}C**	**125 ^{O}C**
Supply-Voltage	2.7V	2.7V	2.7V	2.7V	2.7V	2.7V	2.7V
	2.8V	2.8V	2.8V	2.8V	2.8V	2.8V	2.8V
	2.9V	2.9V	2.9V	2.9V	2.9V	2.9V	2.9V
	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V
	3.1V	3.1V	3.1V	3.1V	3.1V	3.1V	3.1V
	3.2 V	3.2 V	3.2V	3.2 V	3.2 V	3.2V	3.2V
	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V

MAC Unit without Adaptive Technique:-

The SPICE simulation results of the MAC unit without adaptive technique at different frequencies and a fixed supply-voltage each time. The simulation results are presented in two different group like:

- Functional Range
- Power Consumption

The Functional Range of MAC unit at different voltage and temperature is presented with the help of Shmoo-Plot as depicted in Table 5 and 6. It is observed from the results that the MAC unit is behaving correctly in range of BC Freq Limit = 500 MHz and WC Freq Limit =312 MHz

Table 5:-Shmoo-Plot at -40 ^{O}C and 27 ^{O}C

	m40^{O}C Functional Range				27^{O}C Functional Range			
Frequency	**2.7V**	**2.9V**	**3.1V**	**3.3V**	**2.7V**	**2.9V**	**3.1V**	**3.3V**
357.143								
370.37								
384.615								
400								
416.667								
434.783								
454.545								
476.19								
500				**BC**				
526.316								

Table 6:-Shmoo-Plot at 75^{O}C and 125^{O}C

	75^{O}C Functional Range				125^{O}C Functional Range			
Frequency	**2.7V**	**2.9V**	**3.1V**	**3.3V**	**2.7V**	**2.9V**	**3.1V**	**3.3V**
303.03								
312.5					**WC**			
322.581								
333.333								
344.828								
357.143								
370.37								
384.615								
400								
416.667								
434.783								

The system power is evaluated over the wide spectrum of frequency at each temperature and fixed supply voltage range as shown in Fig.9. In Fig.9, the power consumption at different operational frequencies at -40 ^{O}C, 27 ^{O}C, 75 ^{O}C and 125 ^{O}C are shown from upper left corner respectively.

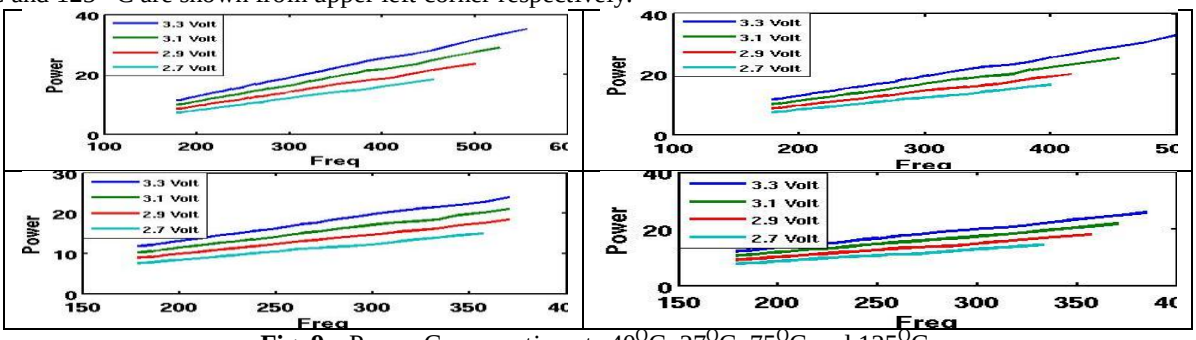


Fig. 9:- Power Consumption at -40^{O}C, 27^{O}C, 75^{O}C and 125^{O}C.

MAC Unit with Adaptive Technique Results:-

The MAC unit with CANARY based adaptive technique is simulated at a wide range of frequency at different temperature ranges as per the Table 4. The simulation results are presented in this section in detail:

As per the CANARY based adaptive technique, CANARY flip-flop setup time is violated before main flip-flop by an defined time depending upon delay unit. On failure of CANARY flip-flop WARN / Error signal is asserted. Numbers of WARN / Errors signals asserted by different CANARY cell at different temperature and average supply-voltage w.r.t. different frequencies and respective temperature are presented in Fig.10 and 11, respectively. Each time there is mismatch between the main Flip-Flop and the CANARY Flip-Flop, the system adaptively switches to next level of supply-voltage and vice versa. Hence, the supply-voltage applied at the system is different at a different time frame. The average voltage applied for a fixed (1000ns) simulation period can be understood from Fig. 10. If there is no error, the supply-voltage is reduced to lower level and frequency is increased in next simulation. Subsequently, after a certain limit, the further increase in frequency require an increase in supply-voltage. As per the Fig 10, there is increase in number of CANARY mismatches with increase once frequency-increase cross some threshold which is different at different temperature. As per Fig 11, for lower range of frequencies average supply-voltage reduces as adaptive system able to drag down the supply-voltage and then for middle range of frequency it gradually increases. For further frequencies the system is only able to sustain at highest supply-voltage.

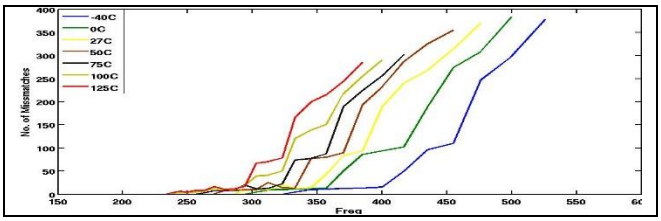


Fig. 10:- Number of CANARY Mismatch.

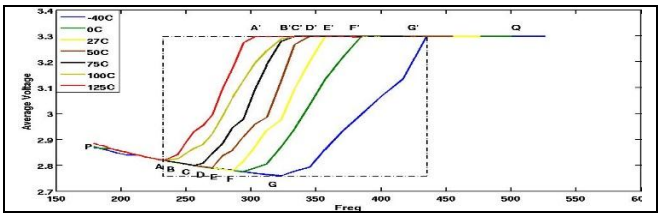


Fig. 11:- Average Supply Voltage

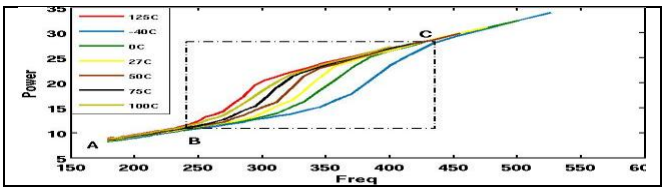
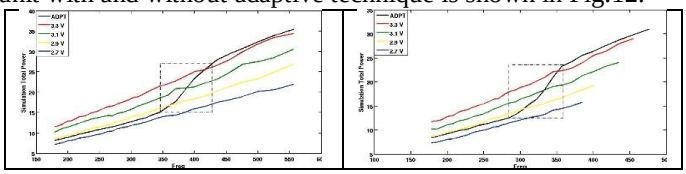


Figure 12:- ADPT System Power Consumption at different Temperature

Result Analysis:-

Power Consumption Comparison:-

It is observed from the SPICE simulation results that the active supply-voltage will be at some lower level as compared to the worst case simulations at different fixed supply voltage initially till the CANARY module starts giving warning signals and then gradually increases at higher frequencies and graph follows the highest supply-voltage (3.3 Volt). As a result of it, the power consumption should also follow the same trend. The power consumption of the MAC unit with and without adaptive technique is shown in Fig.12.



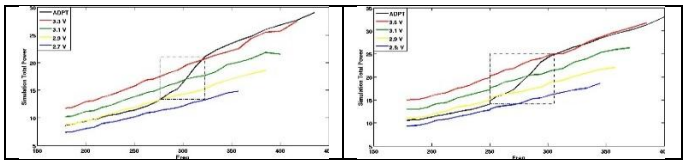


Fig. 12:- Power Comparison at different Temperature.

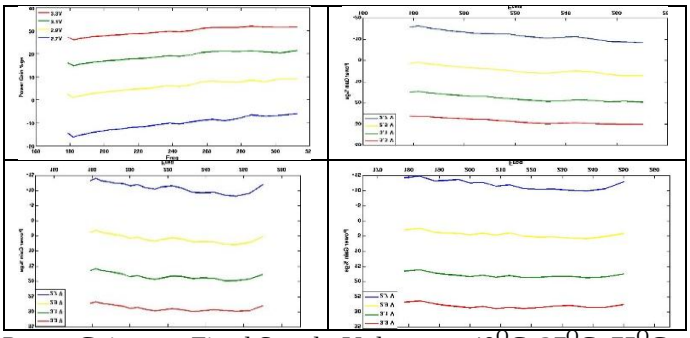


Fig. 13:- Power Gain w.r.t Fixed Supply-Voltage at -40^{O}C, 27^{O}C, 75^{O}C and 125^{O}C

It is observed from the simulation results that up to a certain frequency at each temperature, the power consumption is lower and then starts increasing with CANARY based DVS technique. As soon as the system starts getting CANARY warning, it increases the supply-voltage. As a result of it the power consumption gets increased and finally matches with it at the highest supply voltage power consumption.

Power Gain:-

It is observed in section 6.1 that the initial power consumption is maintained at lowest possible level, then it gradually increases and reaches finally up to the level of power consumed at highest voltage i.e 3.3Volt. In this section the percentage power gain w.r.t fixed supply-voltage systems, at a wide spectrum of functional frequency at different temperatures are shown in Fig. 13 with CANARY based DVS technique. It is observed from Fig. 13 that at each temperature initially the power gain is increased, up to the some respective frequency and then decreases. This behavior is observed because of the adaptive change of supply-voltage as discussed in earlier session 6.1.

Conclusions:-

In this paper, we presented an accurate methodology for predicting the required supply-voltage to optimize the power consumption of the system. The required value of a system voltage is exploited in an adaptive fault-tolerant manner in design. Different scaling-up and scaling-down mechanism is developed and verified for the effectiveness of the power saving. The detailed gain in power consumption at various temperatures and supply voltages are depicted in Table 7 without compromising the system functional bandwidth and throughput.

Table 7:- Percentage Power Gain.

Temp	Compare to Fixed Sup-Voltage 2.7V	Compare to Fixed Sup-Voltage 2.9V	Compare to Fixed Sup-Voltage 3.1V	Compare to Fixed Sup-Voltage 3.3V
-40 ^{O}C	-14% to -6.0%	1% to 9.18%	14.9% to 21.4%	26.1% to 31.6%
27 ^{O}C	-16.3% to -8.3%	0.8% to 7.0%	14.5% to 19.6%	26.3% to 30.1%
75 ^{O}C	-14.1% to -8.1%	3.1% to 7.8%	15.8% to 19.7%	26.7% to 18.4%
125 ^{O}C	-14.9% to -9.9%	2.4% to 5.1%	16.1% to 18.4%	**26.3% to 28.5%**

As per the Table 7, the maximum gain is 28.5%, which is observed over the simulation period of only 1000ns. As the system will operate for more prolonged time the gain will be more as a device will sustain for a longer time at optimum or minimum possible voltage level.

As compared to Classical worst-case margin methodology, here we did not exclude any margin while considering the system without Adaptive Technique. So, if we consider a 10% to be the impact of extra margin the overall gain of the Adaptive Technique will be 28.5+10=38.5% which will increase as the duration of usage is increased.

References:-

1. Borkar S, Karnik T, Narendra S, Tschanz J, Keshavarzi A, De V: Parameter Variations and Impact on Circuits and Microarchitecture. 40th Design Automation Conference (2003)
2. Karnik T, Borkar S, De V: Sub-90nm Technologies: Challenges and Opportunities for CAD. International Conference on Computer Aided Design (2002)
3. Unsal O S, Tschanz J W, Bowman K, De V, Vera X, Gonzalez A, Ergin O: Impact of Parameter Variations on Circuits and Microarchitecture, IEEE Micro, 26(6), (2006)
4. Das S, Sanjay P, Roberts D, Lee L S, Blaauw D, Austin T, Mudge T, Flautner K: A Self-Tuning DVS Processor Using Delay-Error Detection and Correction. Symposium on VLSI Circuits (2005)
5. Ernst D, Kim N S, Das S, Pant S, Rao R, Pham T, Ziesler C, Blaauw D, Austin T, Flautner K, Mudge T: Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation. 36th International Symposium on Microarchitecture (2003)
6. Lu S-L: Speeding up Processing with Approximation Circuits. IEEE Computer, 37(3), (2004)
7. Sato T, Arita I: Constructive Timing Violation for Improving Energy Efficiency. inBenini L, Kandemir M, Ramanujam J: Compilers and Operating Systems for Low Power. Kluwer
8. Academic Publishers (2003)
9. Sato T, Kunitake Y: A Simple Flip-Flop Circuit for Typical-Case Designs for DFM. 8th International Symposium on Quality Electronic Design (2007)
10. Shanbhag N R: Reliable and Efficient System-on-chip Design. IEEE Computer, 37(3), (2004)
11. Uht A K: Going beyond Worst-case Specs with TEAtime. IEEE Computer, 37(3), (2004)
12. Mitra S, Seifert N, Zhang M, Shi Q, Kim K S: Robust System Design with Built-In Soft- Error Resilience. IEEE Computer, 38(2), (2005)
13. Y. Kunitake, T. Sato and H. Yasuura, "A Replacement Strategy for Canary Flip-Flops" PRDC, vol. 4, 227-228 (2010).
14. The Scientist and Engineer's Guide to Digital Signal Processing By Steven W. Smith.
15. Matsui et al., 1994Parameswar et al., 1996Clark et al., 2001Liao and Roberts, 2002 Chang et al 2009.
16. P. Jebashini**,** R. Uma**,** P. Dhavachelvan **and** Hon Kah Wye"A Survey and Comparative Analysis of Multiply-Accumulate (MAC) Block for Digital Signal Processing Application on ASIC and FPGA" Science Alert, July 2015.
17. S. Das, S. Pant, R. David, S. Lee and D. Blaauw "A Self-Tuning DVS Processor Using Delay-Error Detection and Correction," JSSC, 792–804 (2006).
18. H. Fuketa, M. Hashimoto, Y. Mitsuyama and T. Onoye, "Trade-off Analysis between Timing Error Rate and Power Dissipation for Adaptive Speed Control with Timing Error Prediction," ASP-DAC, NJ, USA, 266–271 (2009)
19. H. Fuketa, M. Hashimoto, Y. Mitsuyama and T. Onoye, "Adaptive Performance Compensation With In-Situ Timing Error Predictive Sensors for Sub threshold Circuits" Transaction on VLSI Systems IEEE J., 1 - 11, (2011).