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**RESEARCH ARTICLE**

# DESIGN OF HIGH SPEED,6-BIT PIPELINE ADC WITH BUILT-IN DIGITAL ERROR CORRECTION UNIT USING SUBMICRON CMOS TECHNOLOGY.

***Manjuvani.K.M, Manasa k chigateri, Manjunath K M and Sharan basavaraj B.**
Assistant professor, Department of ECE, RYMEC, Bellary, Karnataka, India.

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***Corresponding Author***

**Manjuvani.K.M.**

## *Abstract*

The paper describes a 6bit, 1Msps Pipeline Analog to Digital Converter implemented in 0.6µm CMOS technology. The design operates at ±5V dc supply. Circuit techniques used include a precise comparator, operational amplifier which works on 1.5bits per stage and non-overlapping clock. A switched capacitor is used to sample and multiply at each stage.



## Introduction:-

Analog to Digital Converters (ADC) are one of the essential elements in mixed signal circuits and systems especially communication systems. Among different types of ADC's, Pipeline ADC's are commonly used for medium to high resolution and speed data conversions, with low power consumption. When compared with other ADC's like Flash ADC, Successive Approximation ADC and Sigma Delta ADC Pipeline ADC has advantages [1] i.e, (a) In Flash ADC the number of comparators increases by factor of 2 for every extra bit of resolution; simultaneously each comparator must be twice as accurate .In Pipeline ADC, however to a first order the complexity only increases linearly, not exponentially, with the resolution. At the sampling rates obtainable by both pipeline and flash converters, a pipeline device usually has much lower power consumption than flash. A Pipeline ADC is much susceptible to comparator metastability. Comparator metastability in flash ADC leads to sparkle code errors. (b) In a Successive Approximation Register (SAR) ADC, the bits are decided by single high speed, high accuracy comparator bit by bit, from MSB down to LSB. The SAR ADC compares the analog input with a DAC, whose output is updated by previously decided bits and successively approximates the analog input. This serial nature of SAR limits the operating speed to no more than a few MSPS, and still slower for very high resolutions (14bits to 16bits). A pipelined ADC however employs a parallel structure in which each stage works on 1 to few bits (of successive samples) concurrently. Although there is only one comparator in SAR, this comparator must be fast and as accurate as the ADC itself. In contrast, none of the comparators inside a Pipelined ADC needs this degree of speed and accuracy. SAR ADC's have high resolution but it suffers with lower speed of operation, where as Pipeline ADC's have medium speed with high resolution as SAR ADC. (c) Sigma-Delta-type converters commonly used in digital audio have a limited bandwidth of about 22 KHz, recently some high –bandwidth Sigma Delta converters reached a bandwidth of 1MHz to 2MHz with 12 to 16 bits of resolution. These specifications indicate sigma delta converters trade speed for resolution. Pipeline ADC's are used in applications like wired or wireless communication systems, digital imaging, ultrasound medical imaging, digital video broadcasting, DSL networks and HD TVs. These days Pipelined ADC's are widely used in wireless communication systems which demand high resolution and high speed data conversions [2].

In this paper, a 6bit, 1Msps Pipeline ADC with 1.5bits per stage and built-in digital error correction unit is presented. The opamp is key element of Pipeline ADC, because it is the major power hungry element and confines the overall

resolution and speed of the ADC. A cascode two stage opamp is designed to make high resolution, high speed operation possible .This paper is organized as follows, section II describes the block diagram, overall architecture and explains its main advantages and challenges. Section III describes conclusion and future enhancement.

## Pipeline adc architecture:-

### Proposed pipeline ADC:-

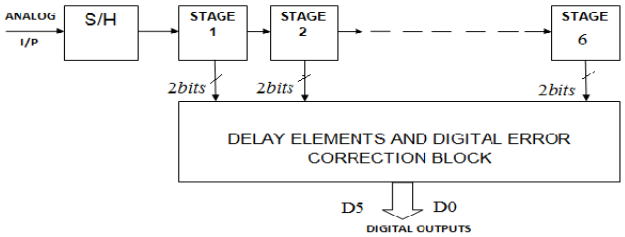



**Fig.1:-** Block diagram of the proposed pipeline ADC.

The proposed 6bit Pipelined ADC uses 1.5bits per stage architecture and consists of six 1.5bits per stages. It consists of delay elements (set of shift registers) used for bit alignment and a digital correction block (a digital adder), that produces the final 6bits. The ADC is shown in Fig.1.

Each Pipeline stage has two important tasks i.e, producing its output bits and generating the residue voltage to deliver to the next stage. The internal structure of each stage of pipeline ADC is shown in Fig 2. As a common expression the set of DAC, summer and gain block, are named Multiplying Digital to Analog Converter (MDAC).In this work, opamp based Switched capacitor (SC) architecture is used to implement the MDAC.

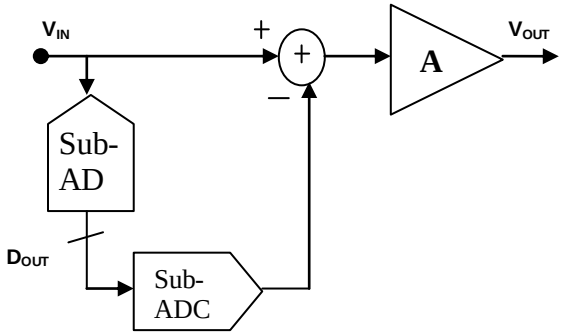



**Fig.2:-** Block diagram of each stage.

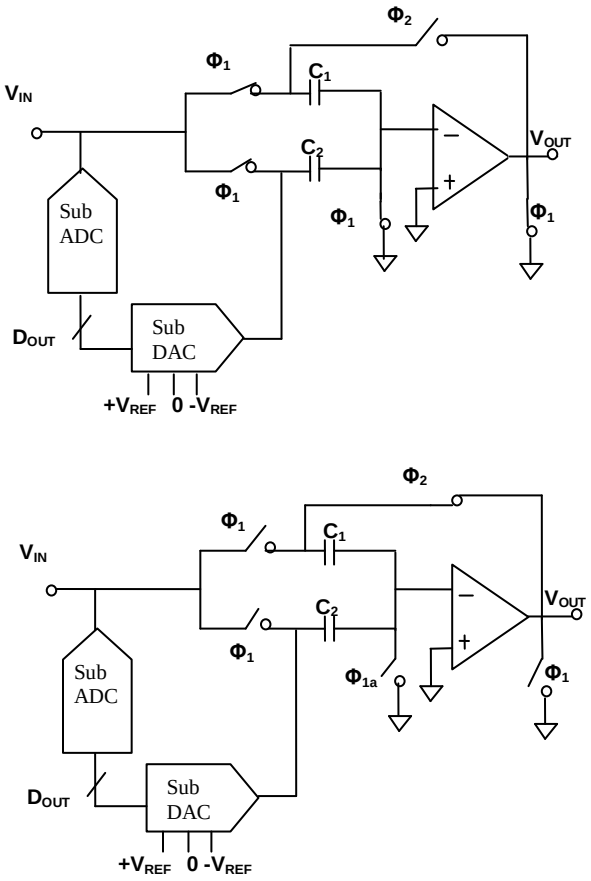
### Bit pipeline stage:-

Using redundancy in the stages is a popular method to increase the accuracy of Pipeline ADC [3], [4], [5], [6].Similarly in the proposed ADC we use 1.5bits per stage architecture to achieve better accuracy.

The 1.5bits per stage works with a two phase non overlapping clock, the sampling phase and the amplifying phase, as shown in Fig 3. Here $D_{OUT}$ represents 2bit digital output which acts as select line for mux as well as input to the Digital error correction block. During the sampling phase ($\Phi_1$ is closed) the input voltage signal is sampled by sampling capacitors $C_1$ and $C_2$ and also the input voltage is applied to the sub-ADC. Consequently, the output bits of the stage are generated at this phase. The $\Phi_{1a}$ is for ensuring that bottom plate sampling is performed [6]

In the amplification phase which is shown in Fig 3(b), ($\Phi_2$ is closed) $C_1$ is located in a feedback loop with the opamp. Based on sub-ADC's output bits, the analog MUX selects one of the inputs and the positive plate of $C_2$ connects to the output of the analog MUX.

As a result in this phase the residue of the current stage is produced and delivers to the next pipeline stage. This residue voltage ( $V_{OUT}$ ) is calculated by equation (1,2,3 )[6].
The sub ADC block consists of comparators and encoder block. It compares the input voltage with two reference voltage levels and generates output bits which commands the MUX (DAC ) to choose the proper reference voltage.




(b)

**Fig.3:-** Operation of SC 1.5bit pipelined stage (a) Sampling phase, (b) Amplifying phase.

Case(i) if $V_{IN} > +V_{REF}/4$
$V_{out} = 2V_{IN} - V_{REF}$ , and $D_{OUT} = 10$ (1)

Case (ii) if $-V_{REF}/4 < V_{IN} <+ V_{REF}/4$
$V_{OUT} = 2V_{IN}$ , and $D_{OUT} = 01$ (2)

Case (iii) if $V_{IN} < -V_{REF}/4$
$V_{OUT} = 2V_{IN} + V_{REF}$ , and $D_{OUT} = 00$ (3)

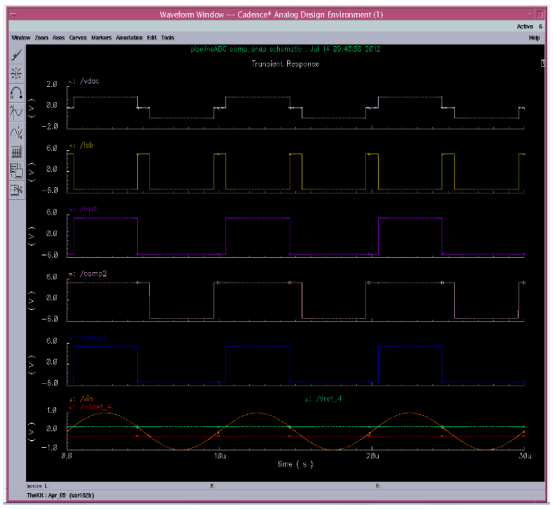


**Fig 4:-** Simulation result of sub-ADC and mux output.

The above Fig 4 shows analog mux implementation which selects $+V_{REF}$ ,0 or $-V_{REF}$ depending on analog input.

**Digital Error Correction unit:-**

For 1.5bit/stage architecture, every pipeline stage will output the digital code of 00, 01 or 10 depending on sampled input. The digital correction of this architecture is fairly simple by only an addition with 1 bit overlap methodology. Fig 5 shows how it works. For instance, the least significant bit (LSB) from stage1 overlaps with the most significant bit (MSB) of stage2 and adds together to be the ADC's output, so does every stage. Therefore, the first pipeline stage provides the MSB for the final output as the sample moves along the pipeline, the remaining stages become less significant and the last stage provides the final LSB.

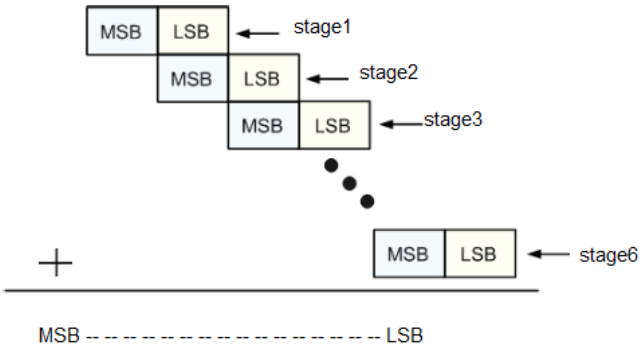



**Fig 5:-** Concept of digital error correction in a 1.5bit pipeline stage ADC

Since pipeline is a serial architecture, the digital output from all pipeline stages must be synchronized to perform the error correction. Digital outputs are synchronous with some delay blocks composed of flip flops, and are digitally corrected via full adder circuit.

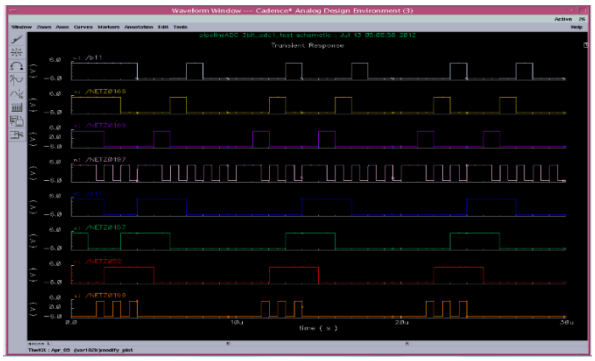



**Fig 6:-** Simulation result of delay elements block.

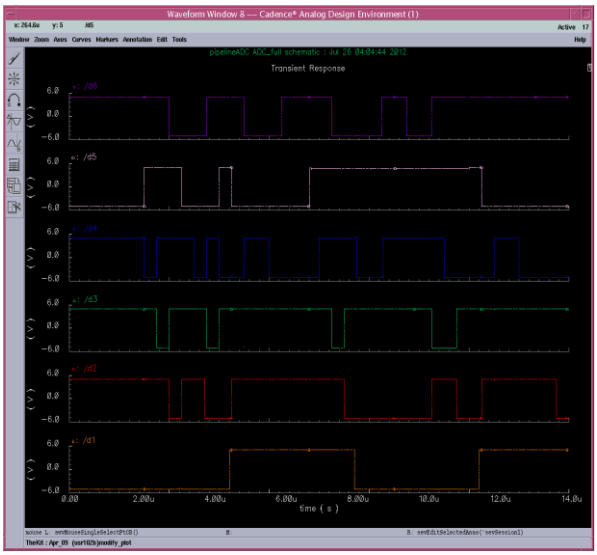



**Fig 7:-** Simulation result of 6bit digital output with analog input 990mV.

**Design Considerations:-**

The design is implemented using opamp with switched capacitor, low resolution comparator and high frequency operated switches etc. There are three main considerations on designing a 1.5bit pipeline stage (a) to achieve the desired linearity for the overall ADC; a precise gain of two is need for each stage. Since this gain is determined by the capacitors ratio $C_1/C_2$ the match between capacitors becomes important, also the match depends on technology used for fabrication. For a specific CMOS technology, as a general principle, increasing the capacitor sizes will decrease the overall sampling speed of the ADC brings up a trade-off between the linearity and sampling speed. (b) The dc gain of the opamp must be high enough to reduce the finite gain error. Neglecting the other non idealities in an N-bit pipelined ADC, it has been shown that the simplified constraint of relation (4) exists for the amplifier gain of the first stage [7], [8], [9], [10].

$$A > 2^N \qquad (4)$$

Consequently, an amplifier with a large open loop dc gain is required when designing an opamp based SC circuit to implement a pipeline stage for the medium to high resolution pipelined ADC. (c) The settling time of the opamp limits the overall ADC performance. In order to have an opamp sufficiently settled in the amplifying clock phase, the opamp must have enough bandwidth but, an opamp with a large bandwidth consumes more power. So to minimize the power consumption we should optimize the bandwidth of the opamp.

## Conclusion:-

A 6bit pipelined ADC with 1.5bits per stage architecture is presented in this paper. The sub-ADC is implemented with pair comparators which has propogation delay of 38.845nsec and logic block. The MDAC is implemented with a cascode two stage OTA which has 67db Gain and 37.4MHz GBW which is sufficient to operate for 1MHz sampling frequency and the switches are designed using Transmission gate which nullifies charge injection, and also is efficient in passing true logic 0 and true logic1 without any offsets. The designed pipeline ADC meets the specifications; the power consumption of entire design was about 530mV. Though the essential core components are implemented, the design can be extended by adding some more work, like implementing clock generator and band-gap reference circuit for generation of reference voltage to sub-ADC block. The performance summary of ADC core is given in Table I.

**Table I:-** Showing summary of ADC.

| | |
|---|---|
| Technology | 0.6μm CMOS |
| Power Supply | ±5V |
| Analog input range | ±50mV to ±1V |
| Input Frequency | 100KHz |
| Sampling Frequency | 1MHz |
| Resolution | 6-bits |
| Power consumption | 530mV |

The design can further be improved by addition of opamp sharing technique in MDAC circuit, along with calibration techniques like capacitor trimming can be done, thus reduces power consumption and non idealities of adc.

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