Journal Homepage: -www.journalijar.com
INTERNATIONAL JOURNAL OF ADVANCED RESEARCH (IJAR)
Article DOI:10.21474/IJAR01/3574
DOI URL: http://dx.doi.org/10.21474/IJAR01/3574
ISSN NO. 2320-5407

RESEARCH ARTICLE

AN EFFICIENT DESIGN OF DIGITAL DOWN CONVERTER FOR SOFTWARE DEFINED RADIO APPLICATION

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Manuscript Info

Manuscript History

Received: 03 January 2017
Final Accepted: 09 February 2017
Published: March 2017

Key words:-
SDR, DDS, DDC, DFE, IF, ADC, NCO, CORDIC, AWP, CR.

ABSTRACT

Adaptive wave pipelining is the methodology used for improving the overall performance of Software Defined Radio (SDR). This method is a functional combination of wave pipelining and hybrid technique. Wave pipelining is the methodology used for improving the performance without using the intermediate latches, at the same time it performs the same operation as pipelining. Hybrid technique is the mechanism that is used for introducing registers for achieving the timing constrain. This technique is implemented in the Direct Digital Synthesizer (DDS) which is the integral part of a Digital Down Converter (DDC) in the Digital Front End (DFE)/ Intermediate Frequency (IF) of Software Defined Radio (SDR). This paper presents the principles of wave pipelining and the method for executing the computer algorithm named Coordinate Digital Rotation Digital Computer (CORDIC) using wave pipelining. Xilinx ISE 14.75 design suite is used as the software for simulation of the proposed system.

Introduction:-

A SDR is defined as the functional system that is implemented in software and whose physical layer behavior can be changed by changing the software function. In SDR waveform signal processing is done digitally. The SDR was developed to obtain transmission link inside different bands of spectrum with a single device. SDR is a radio that solves the gap between different Link-layer protocols and provide an ideal solution for the different functional and performance problem by building a generic platform that switches the functionalities using software control. Fig. 1 shows the basic architecture of SDR.

Fig. 2 shows SDR modules in the two-axis graph Processing Intensity vs. Flexibility that determines some of spectrum signal processing associated with SDR system [1]. The upper left area indicates dedicated functions like ADC & DDC that functions with hardware. Flexibility defines the range of ease to complete the function. The lower area determines the functions like analysis and decision making which are functional parameters.

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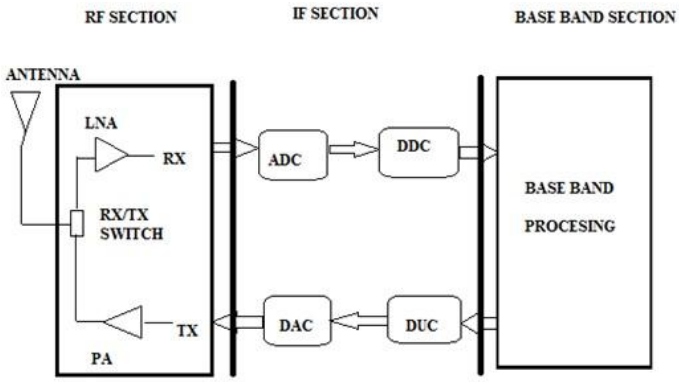

Fig. 1:- Basic architecture of SDR.

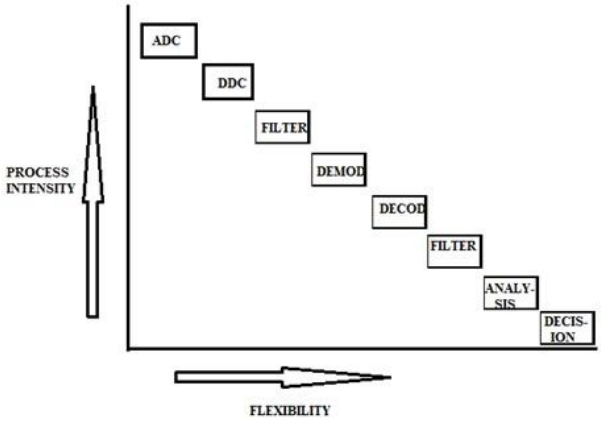

Fig. 2:- SDR modules.

Theory of ddc:-

DDC are implemented in communication processors for converting the sample frequencies. Digital down conversion occurs whenever a signal is of any particular frequency band to baseband [6]. The Fig. 3 (a) & (b) shows the functional block diagram, block diagram of DDC. DDC include frequency shifting operation with chain of mixers, decimators and filters in addition to sampling rate conversion.

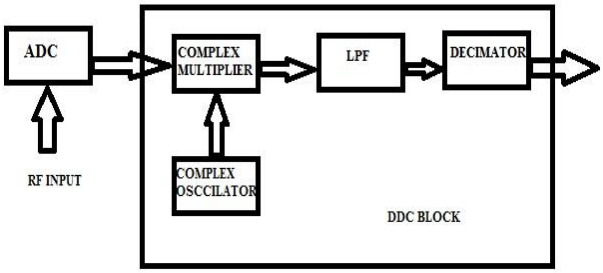

Fig. 3:- (a). Functional Block Diagram of DDC.

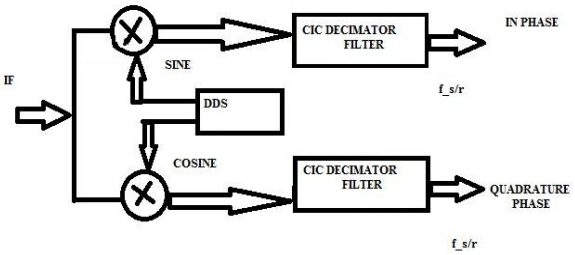

Fig. 3:- (b). Digital Down Converter Block Diagram

DDC is a complex mixer that shifts the frequency of particular range to baseband frequency. The functionality of DDC is mixing and multiplying the retrieved samples with the available digitized stream of data that produces corresponding sine and cosine phase and quadrature channels. DDC's decimate to a lower sampling frequency rate by using different stages of decimation filters. Filtering is performed to limit the bandwidth with the help of linear phase filters. The signals with low data rates are easy to be processed on a low speed functional DSP processor.

DDS/NCO:-
Direct Digital Synthesizer (DDS) is also termed Numerically Controlled Oscillator (NCO). When brought together with a DAC to create an analog output waveform, the system is called a (DDS).

NCO is digital signal generators that generate synchronous, discrete time, discrete value representation of a waveform. In NCO, digital accumulator is used to generate the address into a lookup table. Fig. 4 shows the NCO/DDS functional block diagram.

The system is common, both in hardware and in software. It allows instantaneous changes in the instantaneous frequency or phase of the generated waveform, while maintaining a continuous phase property in the output.

The NCO has 2 parts: [1] Phase Accumulator
[2] Phase To Amplitude Converter

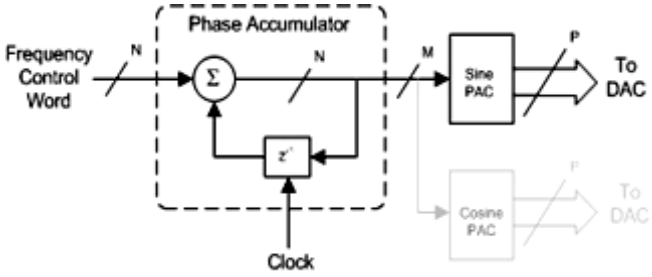

Fig. 4:- NCO/DDS functional block diagram

Theory of cordic algorithm:-

Jack. E. Volder in 1959 coined the Coordinate rotation digital computer (CORDIC). The methodology is applicable for functional execution of digital communication system. It has the characteristics of reading and analyzing the values of any functions that include trigonometric, hyperbolic, arithmetic, vector rotation, and logarithmic [3]. It computes the rotation of vectors by addition and shift operation. They are executed either in rotation mode or vectoring mode [4]. Table 1 shows the output for each mode of operation in different coordinate system. There are three different systems in which the CORDIC can be operated and they are circular coordinate system or in linear coordinate system or in hyperbolic coordinate system.

Fig. 5 shows ith stage for CORDIC from which the basic operating functions of CORDIC for ith iteration can be fetched.

$$X_{i+1} = [X_i - C_i * Y_i * 2^{-i}] * K_i$$
$$Y_{i+1} = [Y_i - C_i * X_i * 2^{-i}] * K_i$$
$$Z_{i+1} = Z_i - C_i * \arctan(2^{-i})$$

C_i Denotes direction of rotation that can have value of 1 or – 1. This is determined by the rotational direction whether positive rotation or a negative rotation. K_i Denotes scaling factor of ith iteration that can be computed at the end stage as it is determined by combination of all stages.

The K value is given theoretical as

$$K = \pi_i * K_i = .60725$$

Table 1:- Output for each mode of operation in different coordinate system

COORDINATE	**ROTATION ($Z_n \rightarrow 0$)**	**VECTORING($Y_n \rightarrow O$)**
CIRCULAR(m=1)	$X_n = \frac{1}{K_m}(X\cos Z - Y\sin Z)$ $Y_n = \frac{1}{K_m}(Y\cos Z + X\sin Z)$	$X_n = \frac{1}{K_m}\sqrt{(X^2 + Y^2)}$ $Z_n = Z + \tan^{-1}\left(\frac{Y}{X}\right)$
LINEAR(m=1)	$X_n = X$ $Y_n = Y + X * Z$	$X_n = X$ $Z_n = Z + \left(\frac{Y}{X}\right)$
HYPERBOLIC(m= 1)	$X_n = \frac{1}{K_m}(X * \cosh Z + Y * \sinh Z)$ $Y_n = \frac{1}{K_m}(Y * \cosh Z + X\sinh Z)$	$X_n = \frac{1}{K_m}\sqrt{(X^2 - Y^2)}$ $Z_n = Z + \tanh^{-1}\left(\frac{Y}{X}\right)$

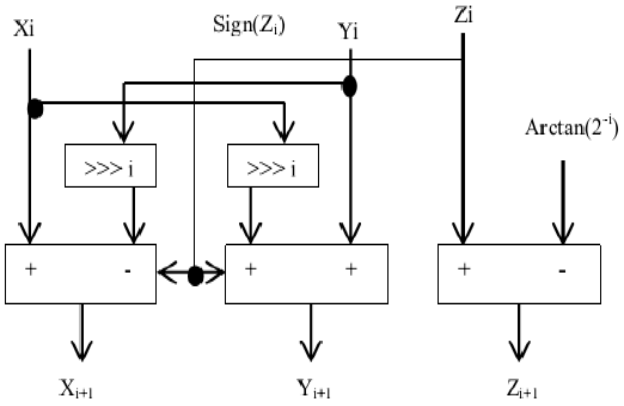

Fig. 5:- ith stage for CORDIC.

Pipeline CORDIC:-

The entire existing system is designed based on pipeline CORDIC. In the pipelined CORDIC architecture, each module is responsible for each elementary rotation occurring in the different modules selected [8] [9]. The modules are combined through immediate latches as shown in Fig. 6. Every stage of CORDIC includes addition, subtraction and shifting operation.

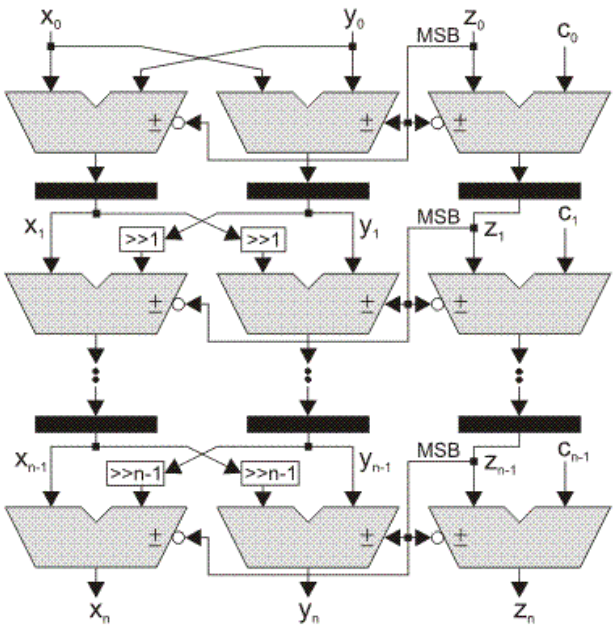

Fig. 6:- Cascading through immediate latches.

Fig. 7:-represent pipelined CORDIC. For a dedicated pipelined architecture, either IN_REGS or OUT_REGS is eliminated there by to improve latency of the design.

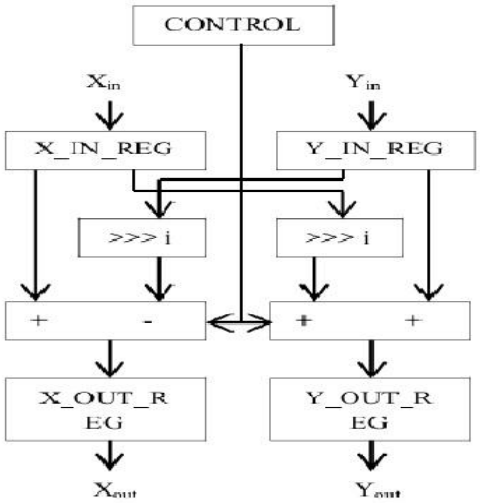

Fig. 7:- ith stage for CORDIC

Table 2 shows the pre computed values of the angle α_i needed for the i^{th} iteration that will be stored in ROM memory location.

Table 2:- Pre-computed angles.

I	$2^{-i} = \tan\alpha_i$	$\alpha_i = \arctan(2^{-i})$	α_i in radians
0	1	45^0	0.7854
1	0.5	26.565^0	0.4636
2	0.25	14.063^0	0.245
3	0.125	7.125^0	0.1244
4	0.0625	3.576^0	0.0624
5	0.03125	1.7876^0	0.0312
6	0.015625	0.8938^0	0.0156
7	0.0078125	0.4469^0	0.0078
..	……..	…..	……

Overflow is parameter that occurs whenever a rotational angle crosses from a positive right angle to negative one [5] [9]. To avoid this there is a functional overflow system control is added. This analyses the nature of operand involved in the operation. If an overflow occurs it retains its previous value.

Advantages of CORDIC Pipeline Over Other Architecture:-

1. Less area consumption
2. Low power consumption
3. Lesser delay
4. Greater throughput

On comparison with the performance

Disadvantage:-

1. Area can be reduced
2. Power consumption can be reduced
3. Reducing delay increasing the speed
4. Throughput can be reduced

Proposed system:-

The proposed system is to design further better architecture that can improve the overall performance of SDR in its applications. There by through comparative and analytical study Adaptive Wave Pipelining (AWP) is the technique that can further improve overall performance of SDR in all aspects comparative of area, speed, throughput, delay.

Adaptive wave pipelining (AWP) is the technique that is implemented in the proposed system. It is combinational logic of wave pipelining and hybrid technique. Wave pipelining is the methodology which is similar to pipelining with the difference that intermediate registers are not used for the wave pipelining execution.

Wave pipelining is an alternative pipelining technique that reduces the clock loads, area, power and latency at the same it retains the external functionality and timing of the circuit [12] [13]. Wave pipelining was coined by Cotton [8] and initially named it as maximum rate pipelining. Synchronization of signals in wave pipelining is achieved by manipulating the timing of signals due to lack of intermediate registers. Fig. 8 represents the block diagram of wave pipelining.

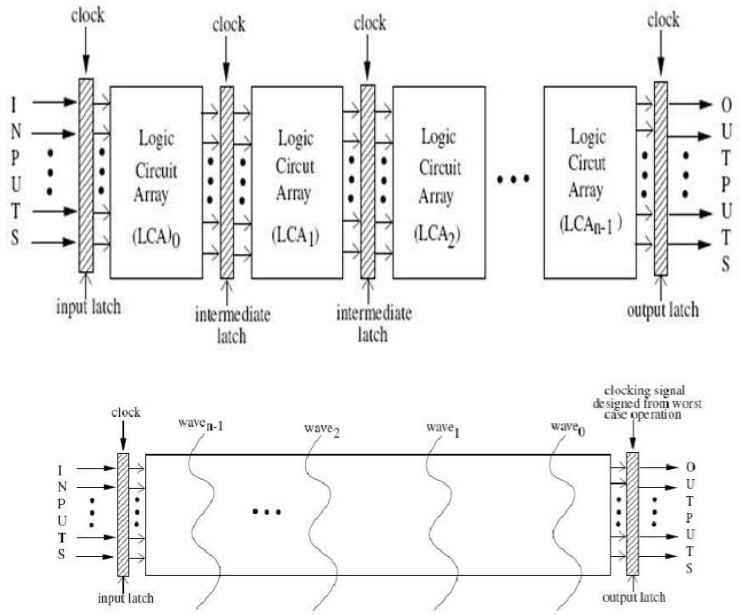

Fig.8:- Block diagram of wave pipelining.

Since there is manipulation of the signals on a periodic basis registers are introduce for the clocking function. This method of introducing the registers in wave pipelining leads to the design of proposed system AWP.

Timing Function:-

Timing requirements for a wave pipeline circuit is done by attaching the registers at the input and output at the periodic basis [14]. The clocking function is derived using certain parameters that help in deriving the timing constrain for the clocking function.

Fig. 9 (a) represents the logic of adaptive wave pipelining and (b) represents the spatial/temporal diagram of wave pipelining.

The timing function is illustrated through the following formulas:-

$$T_{max} > D_{max} + T_{set} + S_{clk}$$

$$T_{cpture} < T_{clk} + D_{min} - (T_{hold} + S_{clk})$$

$$T_{clk} > (D_{max} - D_{min}) + (T_{set} + T_{hold} + S_{clk})$$

Where:-

D_{max} – Is difference between longest path

D_{min} –Is the difference between shortest path

T_{set} – Set time

T_{clk} – Clock time

T_{hold} – Hold time

S_{clk} – Clock skew

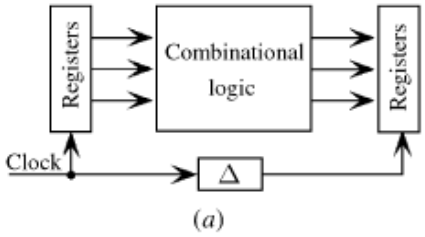

Fig. 9:- (a) Data flow through combinational logic.

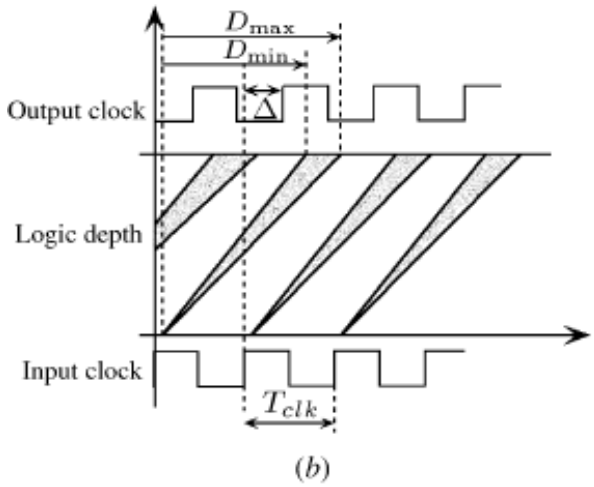

Fig. 9:- (b). Temporal/Spatial representation of wave pipelining.

Fig. 10 shows the functional flow diagram, of AWP. In AWP the entire wave pipelining process is executed by introducing the clocking function for registers. These intermediate registers re used for timing constrain.

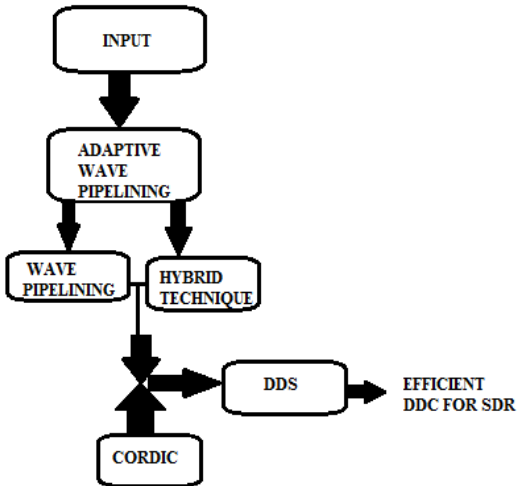

Fig.10:- Flow diagram of AWP

Advantages of Proposed System:-

1. Reduction in area
2. Reduction in power consumption
3. Increase in speed
4. Increase in throughput

Outputs and case study:-

Table 3:- Theoretical comparison of existing and proposed.

FACTORS	CORDIC PIPELINE	ADAPTIPE WAVE PIPELINING WITH CORDIC
SPEED	LESS	MORE
POWER CONSUMPTION	LESS	MORE
MEMORY UTILISATION	LESS	MORE
THROUGHPUT	LESS	MORE

Table 3 shows the theoretical comparison of the existing and proposed system using CORDIC through the literature survey.

Outputs obtained for the CORDIC with AWP using Xilinx synthesis.

KIT USED: - Artix 7
DEVICE:-XC7A100T
PACKAGE: - FTG256
SPEED: - -3

Fig. 11:- And Fig. 12. Represent the output wave for AWP for the specified inputs. They are analyzed through the case studies.

CASE STUDY 1:-
Clk: - 50 duty cycles force constant 1
Enb: - 1
Xi: - 2
Yi: - 3
Zi: - 4

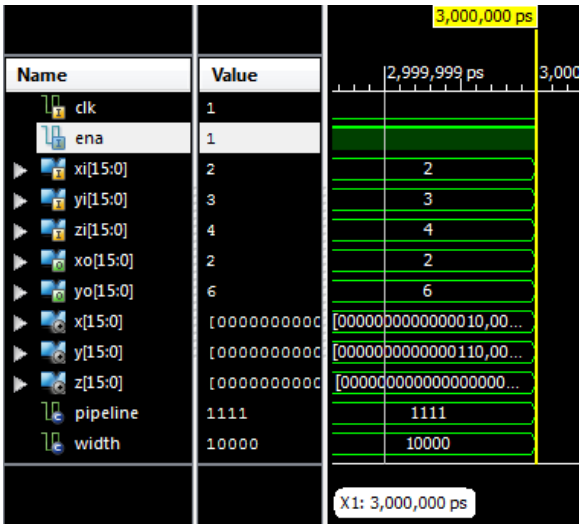

Fig. 11:- Output for AWP

Xo: - 2
Yo: - 6

CASE STUDY 2:-
Clk: - 50 duty cycles force constant 1
Enb: - 1
Xi: - 3
Yi: - 4
Zi: - 5

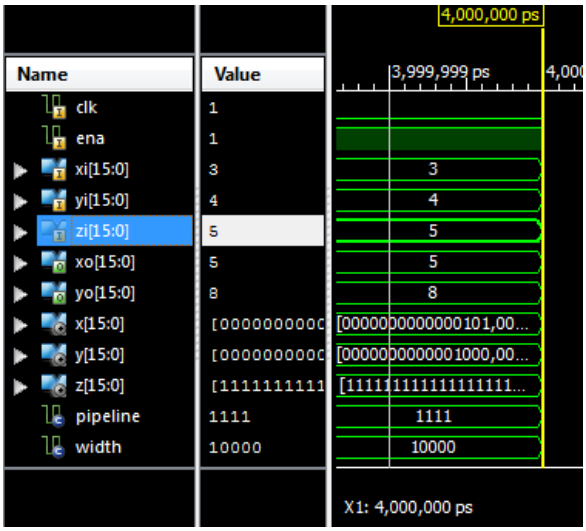

Fig. 14:- Output for AWP

Xo: - 5
Yo: - 8

Inference from the above wave forms fetched is that, whenever each time the value for inputs is forced in the ISim simulator there is corresponding change in the outputs of the wave. The number of register values is clearly available from the output window for further clarification synthesis reports are taken and compared.

Fig. 14. And Fig. 15. Is the utilization summary report that determines the number of registers and LUT's used along with which the delay and maximum frequency, is specified from the synthesis report. These utilization summary of both CORDIC pipeline and AWP are used for comparison.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1000	126800	0%
Number of Slice LUTs	1129	63400	1%
Number of fully used LUT-FF pairs	968	1161	83%
Number of bonded IOBs	74	170	43%
Number of BUFG/BUFGCTRLs	1	32	3%

Minimum period: 2.398ns (Maximum Frequency: 416.963MHz)

Fig. 14:- Utilization summary for CORDIC pipeline.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	680	126800	0%
Number of Slice LUTs	723	63400	1%
Number of fully used LUT-FF pairs	652	751	86%
Number of bonded IOBs	50	170	29%
Number of BUFG/BUFGCTRLs	1	32	3%

Minimum period: 2.036ns (Maximum Frequency: 491.087MHz)

Fig.15:- Utilization summary for AWP

Comparison and analytical study:-

The entire proposed system stated as AWP, is executed using the Xilinx ISE 14.75 and the outputs are fetched. The outputs are compared with the help of utilization summary and synthesis reports.

Graph representations are made for comparison and displaying the comparative area, delay and frequency (throughput). Table 4 shows the practical comparison of the both systems using the physical values fetched after running the codes in Xilinx ISE 14.75 design suite. Fig. 16,17,18,19 are the graph representation done from the synthesis report and utilization summary.

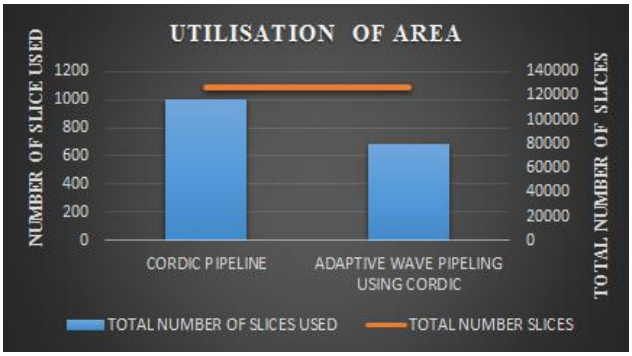

Fig. 16:- Graph representation of area utilization

Inference: From the above graph it is clear to knowledge that the number of slices used by AWP is lesser than the number of slices used by CORDIC pipeline. Hence the area occupied by AWP is less compared to other method.

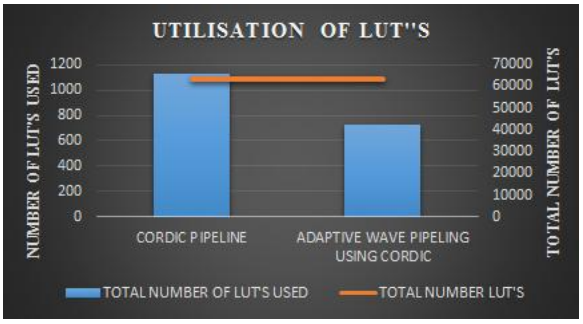

Fig. 17:- Graph representation of utilization of lut's

Inference: the above graph denoted the number of LUT's used by the two different processes. From the graph it is clear that the number of LUT's used by AWP is lesser than the comparative method.

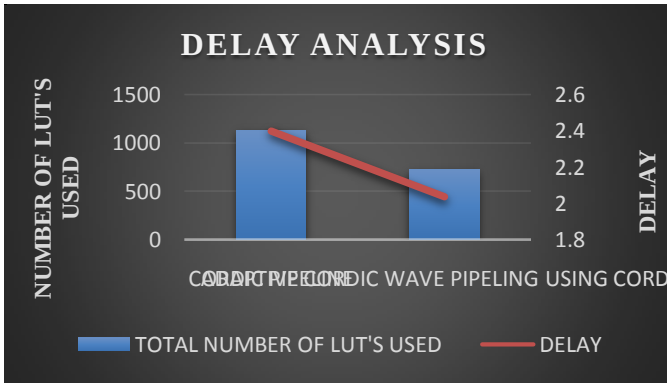

Fig. 18:- Delay analysis

Inference: the above graph is plotted between number of slice LUT's used vs delay. From the previous graph representation it is clear that CORDIC pipeline uses more LUT's than AWP. Hence the delay acquired for CORDIC pipeline is more than the proposed system that is AWP.

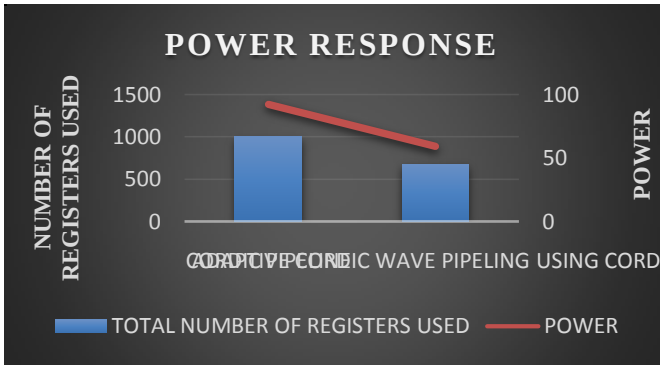

Fig. 19:- Power response.

Inference: the above graph is plotted between number of registers used vs power. Since the number of registers used is less in AWP the power consumed in this method is less. This is been analyzed by plotting the graph

Table 4:- Physical value comparison.

FACTORS	CORDIC PIPELINE	ADAPTIVE WAVE PIPELINING WITH CORDIC
NUMBER OF SLICE REGISTERS USED	1000/126800 UTILISATION-0%	680/126800 UTILISATION-0%
NUMBER OF SLICE LUT'S USED	1129/63400 UTILISATION-1%	723/63400 UTILISATION-1%
FREQUENCY	416.98Mhz	491.087Mhz
DELAY	2.398ns	2.036ns
POWER	1129×.082= 92.578W	723×.082= 59.286W

Conclusion:-

The entire proposed system is designed and executed using Xilinx. The function is designed in such a manner the end users can modify them according their requirements and application. Since FPGA is chosen as target technology the design has resulted in consumption of low area, power with increased speed and throughput.

The entire project work is focused on designing of efficient DDS to improve the efficiency of DDC and improve the overall performance of SDR. In future the entire DDC structure can be designed with the developed AWP technique and better efficient SDR structure can be evolved.

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