8 TO 3 PRIORITY ENCODERS

Manuscript Info

Manuscript History
Received: xxxxxxxxxxxxxxx
Final Accepted: xxxxxxxxxxx
Published: xxxxxxxxxxxxxxx
Key words:-

FSM, HDL, Verilog, IEEE, IC, FPGA

Abstract

The Hardware Description Language (HDL) is a specialized computer language used to describe the structure and behavior of digital circuits and systems. HDLs are essential in the design and development of integrated circuits (ICs) and field-programmable gate arrays (FPGAs). Verilog is a hardware description language (HDL) used to model and design digital circuits. It's widely used in the semiconductor industry for designing and verifying digital systems, especially in the context of Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs) They allow designers to model, simulate, and synthesize hardware designs, effectively creating a blueprint for the physical hardware. In this paper we presented 8 to 3 Priority Encoders with and without priority which was implemented using Verilog.

Introduction:-

Hardware Description Language (HDL) allows designers to model, simulate, and synthesize hardware designs, effectively creating a blueprint for the physical hardware. HDLs are used to create models of digital circuits, allowing designers to simulate their behavior before physical fabrication. HDL code can be automatically converted into physical implementation (e.g., an IC) using specialized software tools, a process called synthesis. HDLs support various levels of abstraction, from high-level behavioral descriptions to low-level gate-level representations. Popular HDLs include VHDL and Verilog, both of which are IEEE standards.

Verilog enables designers to describe the connections and behavior of digital circuits, allowing for a structured and systematic approach to hardware design.

It provides a way to create test benches that simulate the behavior of the designed circuit, ensuring its correctness before physical implementation. Verilog code can be translated into actual hardware implementations using synthesis tools, which convert the code into logic gates and their connections.

An encoder is a device or circuit that converts information from one format to another. In digital electronics, it's a logic circuit that takes multiple input lines and outputs a unique binary code, often representing the active input. In other contexts, an encoder can refer to a device that converts mechanical motion into an electrical signal (like in position sensing) or a process that compresses data (like in video encoding).

An encoder has 2^n input lines and n-output lines. At a time, only one of the 2^n input lines is activated. The coded output of the encoder depends upon the activated input line. There are several types of encoders available such as "octal to binary encoder", "decimal to BCD encoder", "keyboard encoders", etc.

RTL schematic:-

Register transfer level (RTL) is an abstraction for defining the digital portions of a design. It is the principle abstraction used for defining electronic systems today and often serves as the golden model in the design and verification flow.

Technology schematic:-

Technology schematics are architecture-specific designs that use technology-specific/ target FPGA specific components like LUTs, carry logic, I/O buffers, and other technology-specific components.

Device Utilization Summary:-

A device utilization summary, in the context of Verilog HDL designs, refers to a report generated by synthesis and implementation tools (e.g., Xilinx Vivado, Intel Quartus Prime) after processing a Verilog design for a target FPGA or ASIC. This summary provides a detailed breakdown of how the logic described in the Verilog code translates into physical resources available on the chosen device.

Key elements typically found in a device utilization summary include Logic Utilization, Memory Utilization, DSP Slice Utilization, I/O Pin Utilization, and Clock Resources. The device utilization summary is crucial for Resource Management, Design Feasibility, Performance Analysis, Cost Estimation.

Timing Summary:-

In Verilog, timing summaries provide a concise overview of the timing behavior of a digital design, often generated during synthesis or static timing analysis (STA). They detail how signals propagate through the circuit, highlighting potential timing violations like setup and hold time issues. Essentially, they summarize the timing characteristics of paths within the design, ensuring it meets specified clock frequencies and operational constraints.

Priority Encoder:-

A priority encoder is a combinational logic circuit that encodes multiple input lines into a smaller number of output lines, but with a priority function. It assigns a priority level to each input, and when multiple inputs are active, the output reflects only the highest priority input. This is different from a regular binary encoder, which may produce an undefined output when multiple inputs are active.

In digital electronics, a combinational logic circuit which produces outputs in response to only one input among all those that may be activated at the same time is called a priority encoder. For this, it uses a priority system, and hence it is named so.

8 to 3 Priority Encoder without priority:-

A priority encoder 8 to 3 converts eight binary inputs into a 3-bit binary output, prioritizing the highest-order active input. If multiple inputs are active, the output represents the highest-priority input.

Block Diagram of 8 to 3 Encoder without priority:-

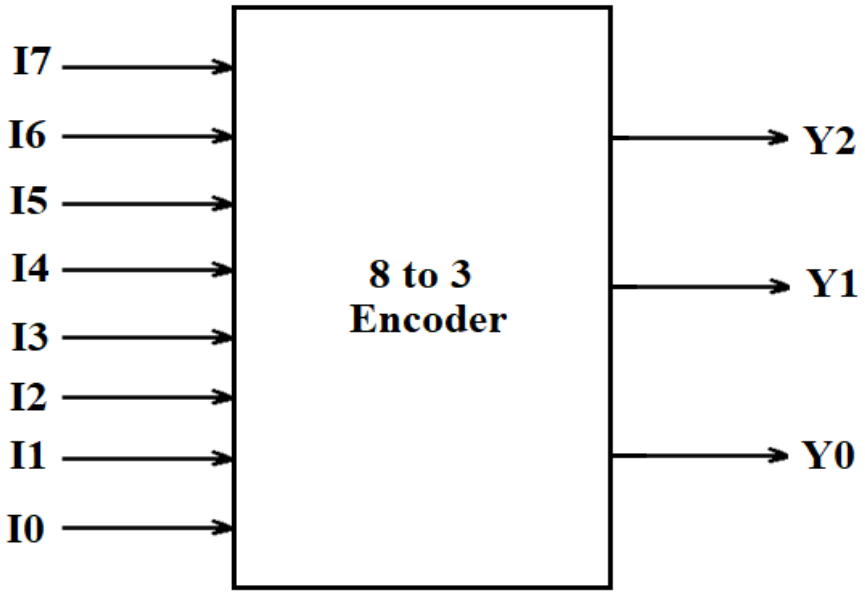


Fig: 8 to 3 Encoder without priority

The Block Diagram of 8 to 3 Encoder without priority consists of 8 inputs from $I_7 - I_o$ and outputs from $Y_2 - Y_o$.

Working of 8 to 3 Encoder without priority:-

The working of 8 to 3 Encoder without priority is as follows,

When the input I_o is active high($I_o = 1$) and all other inputs are active low($I_1I_2I_3I_4I_5I_6I_7 = 0000000$) then the output ($Y_2Y_1Y_0$) becomes 000.

When the input I_1 is active high($I_1 = 1$) and all other inputs are active low($I_0I_2I_3I_4I_5I_6I_7 = 0000000$) then the output ($Y_2Y_1Y_0$) becomes 001.

When the input I_2 is active high($I_2 = 1$) and all other inputs are active low($I_0I_1I_3I_4I_5I_6I_7 = 0000000$) then the output ($Y_2Y_1Y_0$) becomes 010.

When the input I_3 is active high($I_3 = 1$) and all other inputs are active low($I_0I_1I_2I_4I_5I_6I_7 = 0000000$) then the output ($Y_2Y_1Y_0$) becomes 011.

When the input I_4 is active high($I_4 = 1$) and all other inputs are active low($I_0I_1I_2I_3I_5I_6I_7 = 0000000$) then the output ($Y_2Y_1Y_0$) becomes 100.

When the input I_5 is active high($I_5 = 1$) and all other inputs are active low($I_0I_1I_2I_3I_4I_6I_7 = 0000000$) then the output ($Y_2Y_1Y_0$) becomes 101.

When the input I_6 is active high($I_6 = 1$) and all other inputs are active low($I_0I_1I_2I_3I_4I_5I_7 = 0000000$) then the output ($Y_2Y_1Y_0$) becomes 110,

Similarly, when the input I_7 is active high($I_7 = 1$) and all other inputs are active low($I_0I_1I_2I_3I_4I_5I_6 = 0000000$) then the output ($Y_2Y_1Y_0$) becomes 111.

Truth Table : 8 to 3 Encoder without priority:-

I7	I6	I5	I4	I3	I2	I1	I0	Y2	Y1	Y0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

Logic Diagram of 8 to 3 Encoder without priority:-

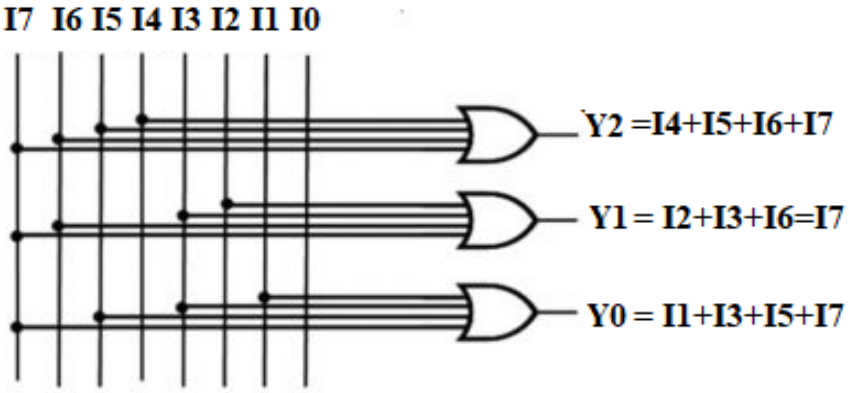
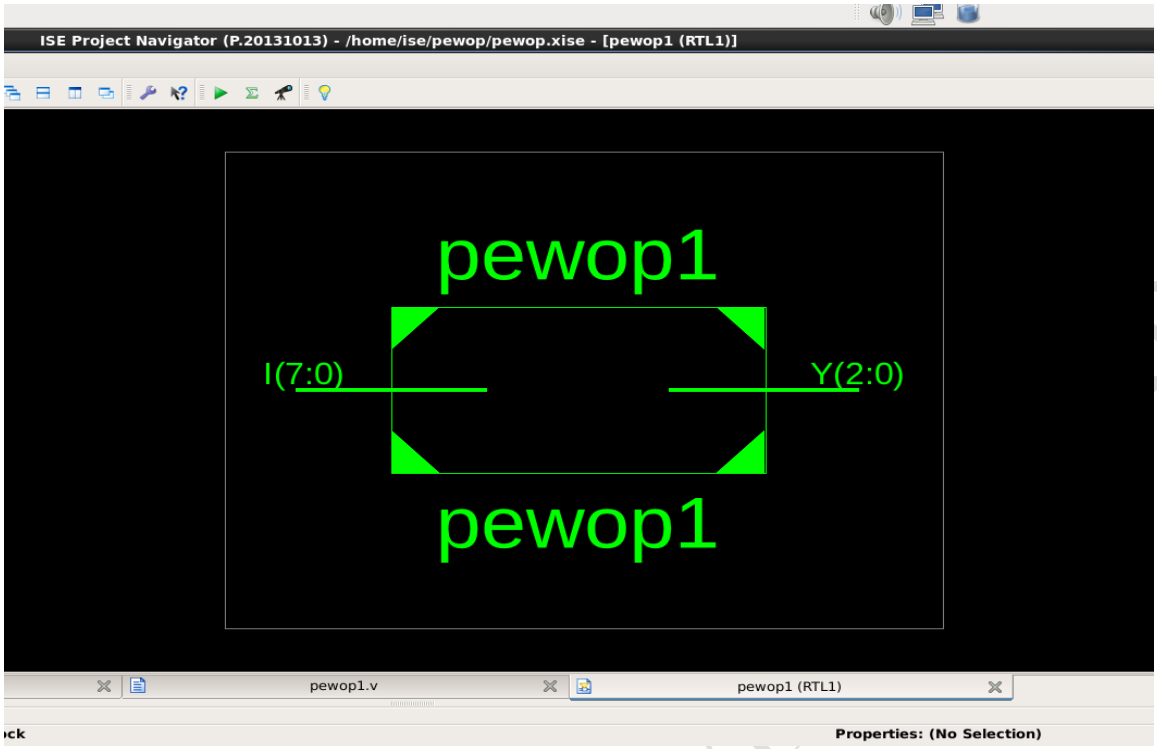


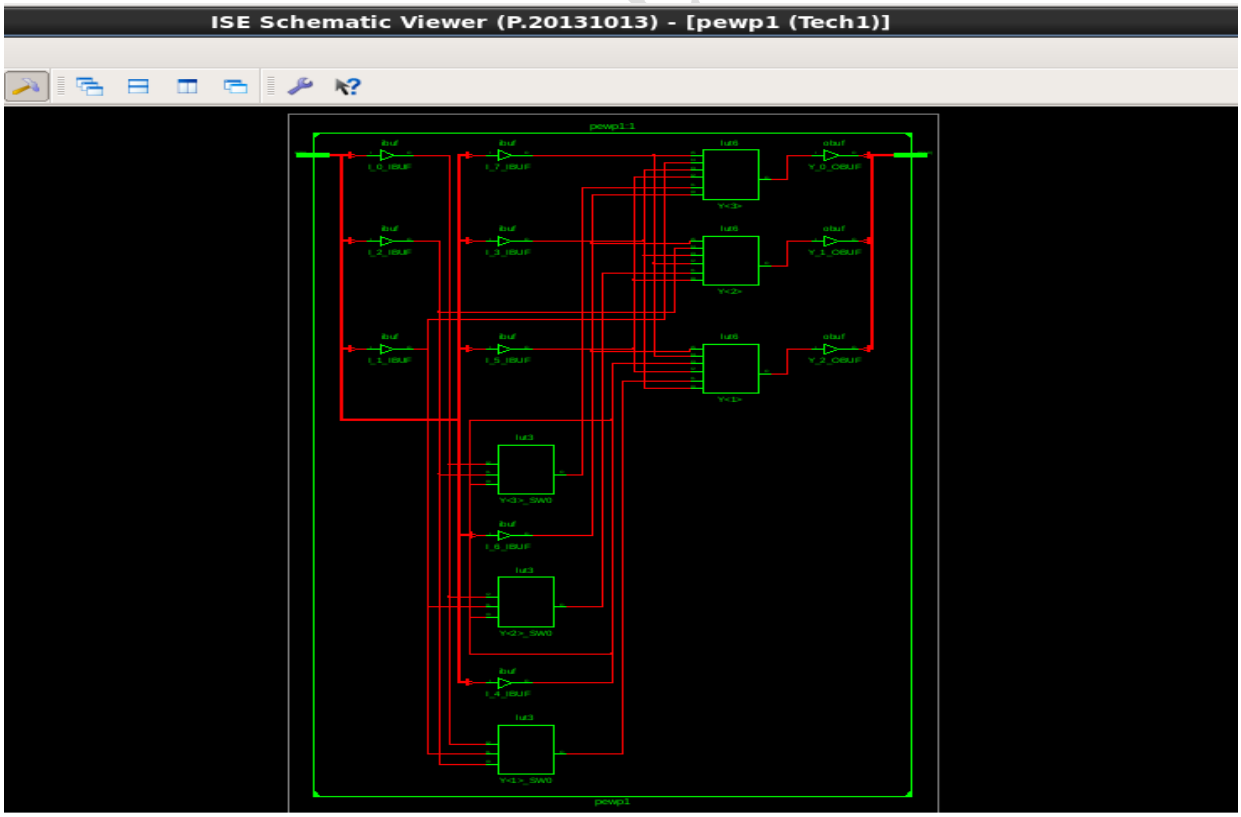
Fig: Logic Diagram of 8 to 3 Encoder without priority

RTL schematic:- 8 to 3 Encoder without priority



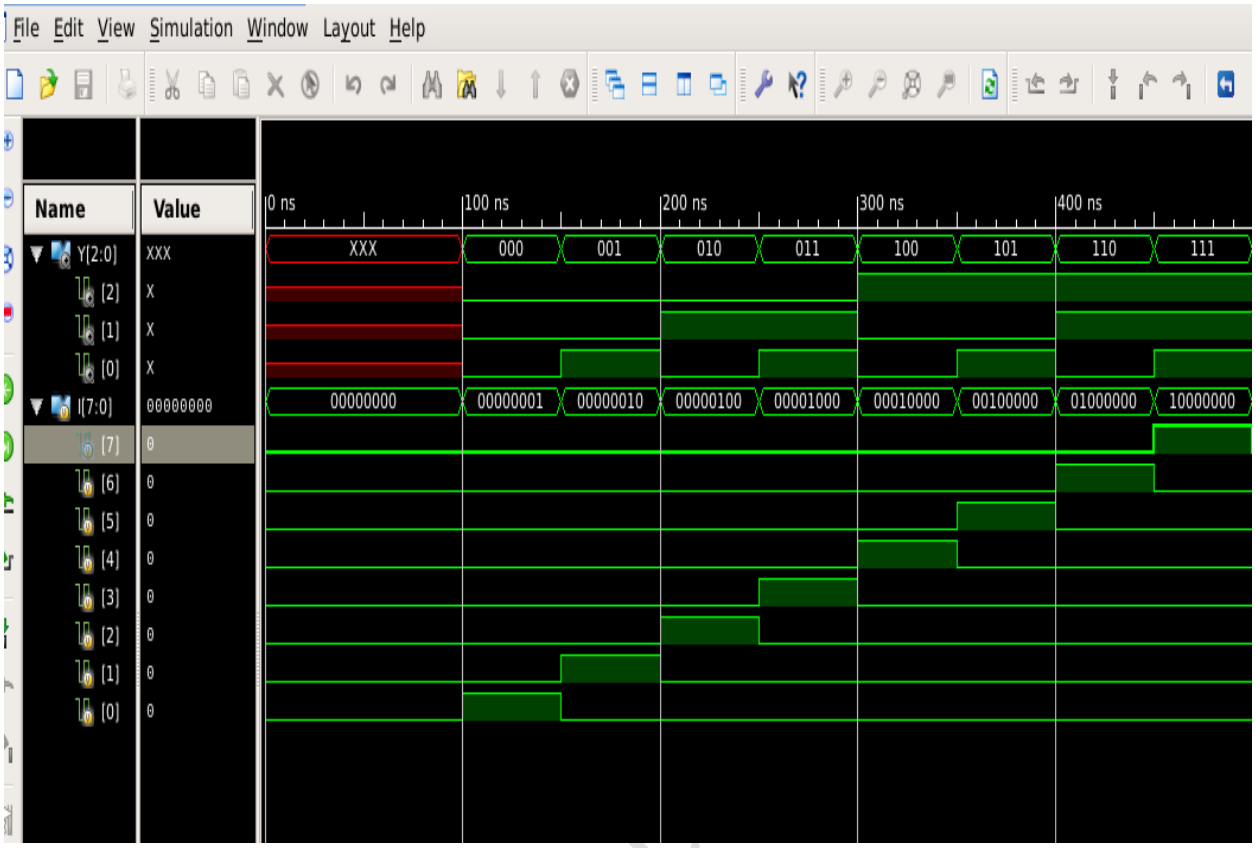
82

83 **Technology schematic:- 8 to 3 Encoder without priority**



84

85 **Output Waveform: - 8 to 3 Encoder without priority**



Timing Summary:- 8 to 3 Encoder withput priority

Speed Grade: -3

Minimum period	No path found
Minimum input arrival time before clock	No path found
Maximum output required time after clock	No path found
Maximum combinational path delay	1.679ns

Device utilization summary:- 8 to 3 Encoder withput priority

Selected Device: 7a100tcsg324-3

Slice Logic Utilization:	
Number of Slice LUTs:	6 out of 63400 0%
Number used as Logic:	6 out of 63400 0%
Slice Logic Distribution:	
Number of LUT Flip Flop pairs used	6
Number with an unused Flip Flop	6 out of 6 100%
Number with an unused LUT	0 out of 6 0%
Number of fully used LUT-FF pairs	0 out of 6 0%
Number of unique control sets	0
IO Utilization:	
Number of IOs	11
Number of bonded IOBs	11 out of 210 5%

Primitive and Black Box Usage:- 8 to 3 Encoder withput priority

#BELS	6
#LUT3	3
#LUT6	3
# IO Buffers	11
# IBUF	8

8 to 3 Priority Encoder with priority:-

A priority encoder 8 to 3 converts eight binary inputs into a 3-bit binary output, prioritizing the highest-order active input. If multiple inputs are active, the output represents the highest-priority input.

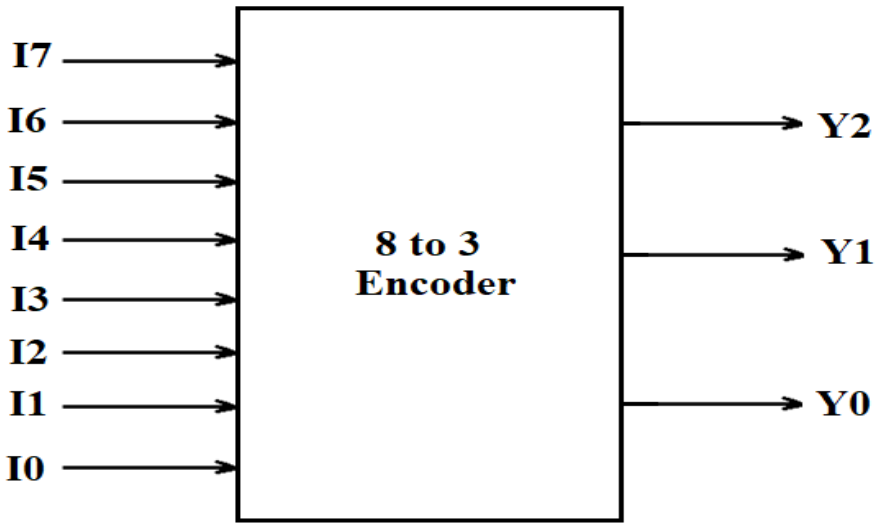


Fig: 8 to 3 Encoder with priority

Working of 8 to 3 Encoder with priority:-

The working of 8 to 3 Encoder with priority is as follows,

When the enble input is active low(en = 0):

When all the other inputs are active low($I_oI\ I_1I_2I_3I_4I_5I_6I_7$ = 00000000) then the output ($Y_2Y_1Y_0$) becomes ZZZ (High impedance state).

When the enble input is active high(en = 1):

When all the other inputs are active low($I_oI\ I_1I_2I_3I_4I_5I_6I_7$ = 00000000) then the output ($Y_2Y_1Y_0$) becomes XXX.

When the input I_o is active high(I_o = 1) and all other inputs are active low($I_1I_2I_3I_4I_5I_6I_7$ = 0000000) then the output ($Y_2Y_1Y_0$) becomes 000.

When the input I_1 is active high(I_1 = 1) and all other inputs are active low($I_0I_2I_3I_4I_5I_6I_7$ = X000000) then the output ($Y_2Y_1Y_0$) becomes 001.

When the input I_2 is active high(I_2 = 1) and all other inputs are active low($I_0I_1I_3I_4I_5I_6I_7$ = 0X00000) then the output ($Y_2Y_1Y_0$) becomes 010.

When the input I_3 is active high(I_3 = 1) and all other inputs are active low($I_0I_1I_2I_4I_5I_6I_7$ = 00X0000) then the output ($Y_2Y_1Y_0$) becomes 011.

When the input I_4 is active high(I_4 = 1) and all other inputs are active low($I_0I_1I_2I_3I_5I_6I_7$ = 000X000) then the output ($Y_2Y_1Y_0$) becomes 100.

When the input I_5 is active high(I_5 = 1) and all other inputs are active low($I_0I_1I_2I_3I_4I_6I_7$ = 0000X00) then the output ($Y_2Y_1Y_0$) becomes 101.

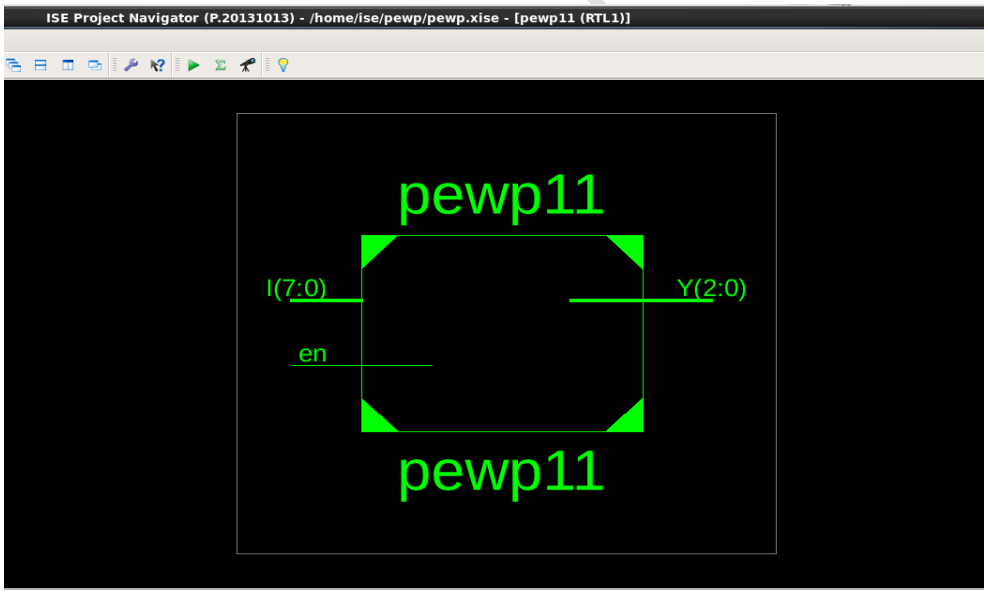
When the input I_6 is active high(I_6 = 1) and all other inputs are active low($I_0I_1I_2I_3I_4I_5I_7$ = 00000X0) then the output ($Y_2Y_1Y_0$) becomes 110,

Similarly, when the input I_7 is active high(I_7 = 1) and all other inputs are active low($I_0I_1I_2I_3I_4I_5I_6$ = 000000X) then the output ($Y_2Y_1Y_0$) becomes 111.

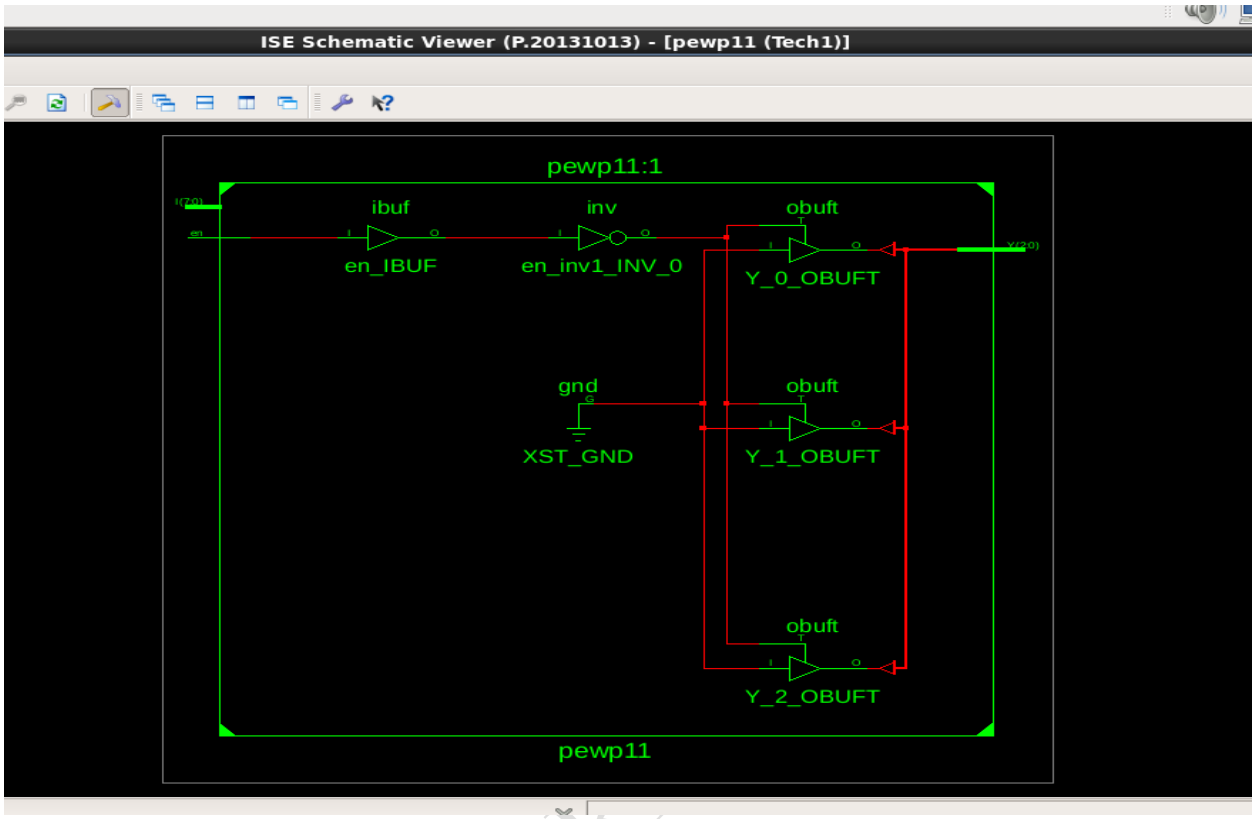
Truth Table :- 8 to 3 Encoder with priority

en	I7	I6	I5	I4	I3	I2	I1	I0	Y2	Y1	Y0
0	0	0	0	0	0	0	0	0	Z	Z	Z
1	0	0	0	0	0	0	0	0	X	X	X
1	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	1	X	0	0	1
1	0	0	0	0	0	1	X	X	0	1	0
1	0	0	0	0	1	X	X	X	0	1	1
1	0	0	0	1	X	X	X	X	1	0	0
1	0	0	1	X	X	X	X	X	1	0	1
1	0	1	X	X	X	X	X	X	1	1	0
1	1	X	X	X	X	X	X	X	1	1	1

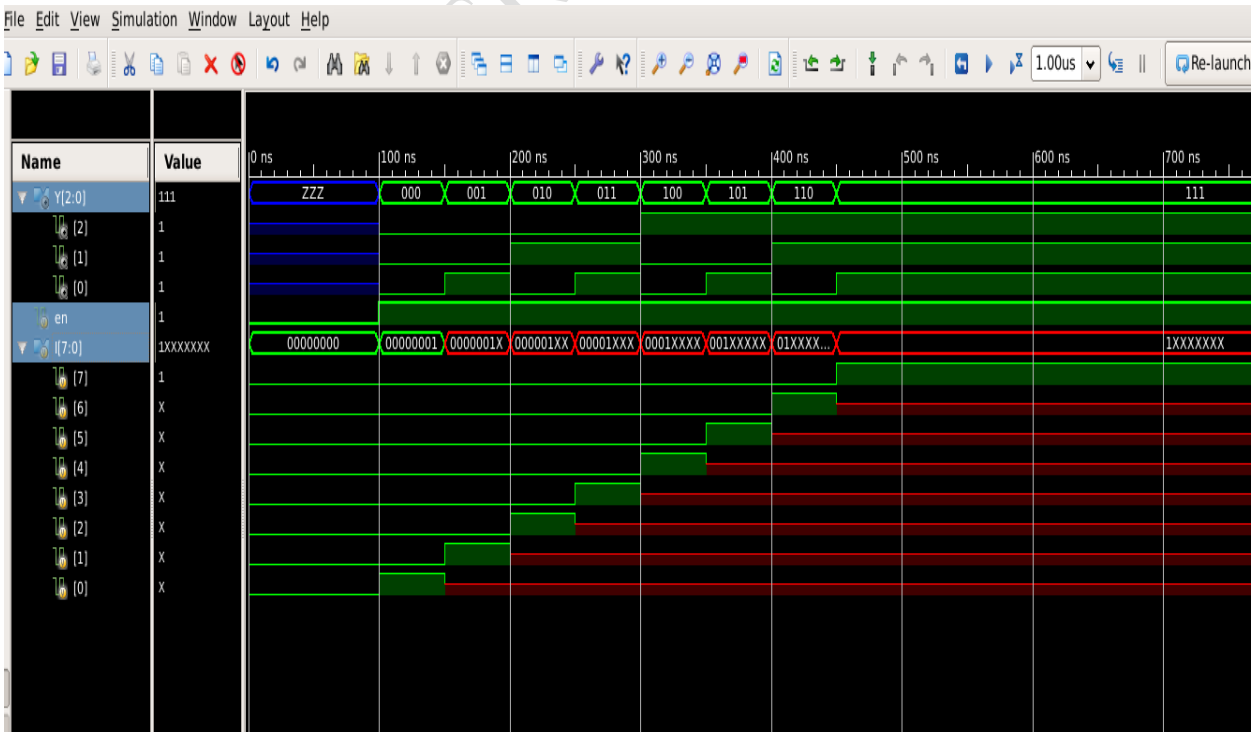
RTL schematic: - 8 to 3 Encoder with priority



Technology schematic: - 8 to 3 Encoder with priority



Output Waveform: - 8 to 3 Encoder with priority



Timing Summary: - 8 to 3 Encoder with priority

Speed Grade: -3

Minimum period	No path found
Minimum input arrival time before clock	No path found
Maximum output required time after clock	No path found
Maximum combinational path delay	0.682ns

Device utilization summary:- 8 to 3 Encoder with priority

Selected Device: 7a100tcsg324-3

Slice Logic Utilization:	
Number of Slice LUTs:	1 out of 63400 0%
Number used as Logic:	1 out of 63400 0%
Slice Logic Distribution:	
Number of LUT Flip Flop pairs used	1
Number with an unused Flip Flop	1 out of 1 100%
Number with an unused LUT	0 out of 1 0%
Number of fully used LUT-FF pairs	0 out of 1 0%
Number of unique control sets	0
IO Utilization:	
Number of IOs	12
Number of bonded IOBs	4 out of 210 1%

Primitive and Black Box Usage:- 8 to 3 Encoder with priority

#BELS	2
#GND	1
#INV	1
# IO Buffers	4
# IBUF	1
# OBUFT	3

Conclusion:-

In this paper priority encoders (8 to 3) with and without priorities was implemented and simulated and synthesized using Verilog. RTL and Technology schematics were obtained. Device Utilization Summary, Timing Summary and Primitive and Black Box Usage were summarized.

References:

[1] J. G. Delgado-Frias, J. Nyathi, "A high-performance encoder with priority lookahead," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 47, no. 9, pp. 1390–1292, 2000.

[2] A. Morgenshtein, A. Fish, and I. A. Wagner, "Gate-Diffusion Input (GDI): A Power Efficient Method for Digital Combinatorial Circuits ", *IEEE Trans. VLSI Systems*, Vol. 10, No. 5, pp- 566 to 581, Oct. 2002.

[3] S. A. Hafeez and S. Harb, "A VLSI high performance priority Encoder using standard CMOS library ", *IEEE transactions on Circuits and System II*, Vol. 53, pp- 597 to 601, No. 8, August 2006.

[4] Vishal Khandelwal and Ankur Srivastava, "Leakage Control Through Fine-Grained Placement and Sizing of Sleep Transistors ", *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS*, Vol. 26, No. 7, JULY 2007.

[5] H. F. Dadgour and K. Banerjee "A novel variation-tolerant keeper architecture for high-performance low-power wide fan-in dynamic OR gates", *IEEE Trans. Very Large Intrgr. (VLSI) Syst.*, vol. 18, no. 11, pp. 1567–1577 2010.

[6] S. W. Huang, and Y. J. Chang, "A full parallel priority encoder design used in comparator," in *Proc. of the 53rd IEEE International Midwest Symposium on Circuits and Systems*, Seattle, USA, pp. 877–880, 2010.

[7] N. Mehta and B. Amrutur, "Dynamic supply and threshold voltage scaling for CMOS digital circuits using in-situ power monitor ", *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, Vol. 20, No. 5, pp- 892 to 901, May 2012.

[8] Amritesh Ojha, Rajesh Mehra, "low Power Layout design of Priority encoder using 65nm technology ", *International Journal of Engineering Trends and Technology (IJETT)* -Volume 23 Number 9 - May 2015.

[9] Ojha, Amritesh & Mehra, Dr. Rajesh. (2015). Low Power Layout Design of Priority Encoder Using 65nm Technology. *International Journal of Engineering Trends and Technology*. 23. 450–453. 10.14445/22315381/IJETT-V23P285.

[10] L. Dileshwar Rao, S. Dixit, K. Pachkor, and M. Aarthy, "FinFET based adiabatic logic design for low power applications," *2017 International conference on Microelectronic Devices, Circuits and Systems (ICMDCS)*, Vellore, India, 2017, pp. 1–6, doi: 10.1109/ICMDCS.2017.8211535.

[11] E. Norige, A. X. Liu, E. Torng, "A ternary unification framework for optimizing TCAM-based packet classification systems," *IEEE/ACM Transactions on Networking*, vol. 26, no. 2, pp. 657–670, 2018.

[12] C. -L. Hsieh, N. Weng and W. Wei, "Scalable Many-Field Packet Classification for Traffic Steering in SDN Switches," *IEEE Transactions on Network and Service Management*, vol. 16, no. 1, pp. 348–361, 2019.

[13] R. R. Vallabhuni, A. Karthik, C. V. Sai Kumar, B. Varun, P. Veerendra, and S. Nayak, "Comparative Analysis of8-Bit Manchester Carry Chain Adder Using FinFET at 18nm Technology," *2020 3rd International Conference on Intelligent Sustainable Systems (ICISS)*, Tho othukudi, India, 2020, pp. 1579–1583, doi: 10.1109/ICISS49785.2020.9316061.

[14] R. R. Vallabhuni, D. V. L. Sravya, M. S. Shalini, and G. U. Maheshwararao, "Design of Comparator using 18nm FinFET Technology for Analog to Digital Converters," *2020 7th International Conference on Smart Structures and Systems (ICSSS)*, Chennai, India, 2020, pp. 1–6, doi: 10.1109/ICSSS49621.2020.9202164.

[15] M. Irfan, Z. Ullah, M.H. Chowdhury and R.C. Cheung, "RPE-TCAM: Reconfigurable power-efficient ternary content-addressable memory on FPGAs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 8, pp. 1925–1929, 2020.

[16] S. Asadrooz, M. Nassiri, M. Abbasi, and H. Abdoli, "A Traffic-Aware Packet Classification Method to Reduce Memory Accesses," *Iranian Journal of Electrical and Computer Engineering*, vol. 18, no. 3, pp. 185–196, 2021.

[17] J. Yang, H. Lee, J.H. Jeong, T.h. Kim, S.H. Lee, T. Song, A Practical Implementation of the Ternary Logic Using Memristors and MOSFETs, in: 2021 IEEE 51st International Symposium on Multiple-Valued Logic, ISMVL, 2021, pp. 183–188.

[18] A. Goenka, S. Mitra, N. Das, Design of Balanced Ternary Encoder and Decoder, in: 2022 6th International Conference on Computing Methodologies and Communication, ICCMC, 2022, pp. 482–490.

[19] V.S.M. Srinivasavarma, S. Pydi Sk. N. Mahammad, "Hardware-based multi-match packet classification in NIDS: an overview and novel extensions for improving the energy efficiency of TCAM -based classifiers," *The Journal of Supercomputing*, vol. 78, no. 11, pp. 13086–13121, 2022.

[20] M. Dhayalakumar, Sk. N. Mahammad, "TeRa: Ternary and Range based packet classification engine," *Integration*, vol. 96, pages. 102153, 2024.