

# 8 TO 3 PRIORITY ENCODERS

*by* Jana Publication & Research

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## 8 TO 3 PRIORITY ENCODERS

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#### Key words:-

**FSM, HDL, Verilog, IEEE, IC, FPGA**

The Hardware Description Language (HDL) is a specialized computer language used to describe the structure and behavior of digital circuits and systems. HDLs are essential in the design and development of integrated circuits (ICs) and

### Abstract

field-programmable gate arrays (FPGAs). Verilog is a hardware description language (HDL) used to model and design digital circuits. It's widely used in the semiconductor industry for designing and verifying digital systems, especially in the context of Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs). They allow designers to model, simulate, and synthesize hardware designs, effectively creating a blueprint for the physical hardware. In this paper we presented 8 to 3 Priority Encoders with and without priority which was implemented using Verilog.

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### Introduction:-

Hardware Description Language (HDL) allows designers to model, simulate, and synthesize hardware designs, effectively creating a blueprint for the physical hardware. HDLs are used to create models of digital circuits, allowing designers to simulate their behavior before physical fabrication. HDL code can be automatically converted into physical implementation (e.g., an IC) using specialized software tools, a process called synthesis. HDLs support various levels of abstraction, from high-level behavioral descriptions to low-level gate-level representations. Popular HDLs include VHDL and Verilog, both of which are IEEE standards.

Verilog enables designers to describe the connections and behavior of digital circuits, allowing for a structured and systematic approach to hardware design.

It provides a way to create test benches that simulate the behavior of the designed circuit, ensuring its correctness before physical implementation. Verilog code can be translated into actual hardware implementations using synthesis tools, which convert the code into logic gates and their connections.

An encoder is a device or circuit that converts information from one format to another. In digital electronics, it's a logic circuit that takes multiple input lines and outputs a unique binary code, often representing the active input. In other contexts, an encoder can refer to a device that converts mechanical motion into an electrical signal (like in position sensing) or a process that compresses data (like in video encoding).

An encoder has  $2^n$  input lines and n-output lines. At a time, only one of the  $2^n$  input lines is activated. The coded output of the encoder depends upon the activated input line. There are several types of encoders available such as "octal to binary encoder", "decimal to BCD encoder", "keyboard encoders", etc.

### RTL schematic:-

<sup>7</sup> Register transfer level (RTL) is an abstraction for defining the digital portions of a design. It is the principle abstraction used for defining electronic systems today and often serves as the golden model in the design and verification flow.

### Technology schematic:-

Technology schematics are architecture-specific designs that use technology-specific/ target FPGA specific components like LUTs, carry logic, I/O buffers, and other technology-specific components.

### Device Utilization Summary:-

<sup>17</sup> A device utilization summary, in the context of Verilog HDL designs, refers to a report generated by synthesis and implementation tools (e.g., Xilinx Vivado, Intel Quartus Prime) after processing a Verilog design for a target FPGA or ASIC. This summary provides a detailed breakdown of how the logic described in the Verilog code translates into physical resources available on the chosen device.

Key elements typically found in a device utilization summary include Logic Utilization, Memory Utilization, DSP Slice Utilization, I/O Pin Utilization, and Clock Resources. The device utilization summary is crucial for Resource Management, Design Feasibility, Performance Analysis, Cost Estimation.

### Timing Summary:-

In Verilog, timing summaries provide a concise overview of the timing behavior of a digital design, often generated during synthesis or static timing analysis (STA). They detail how signals propagate through the circuit, highlighting potential timing violations like setup and hold time issues. Essentially, they summarize the timing characteristics of paths within the design, ensuring it meets specified clock frequencies and operational constraints.

### <sup>10</sup> Priority Encoder:-

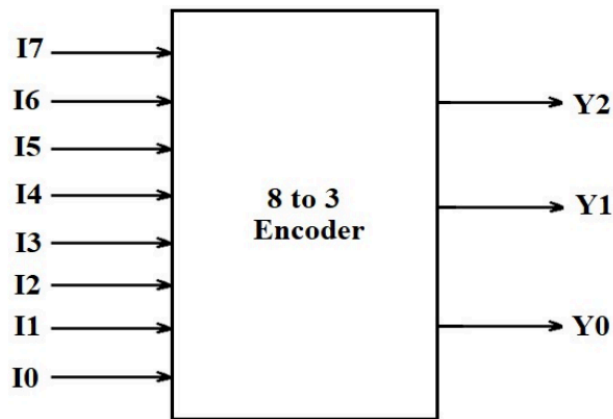
A priority encoder is a combinational logic circuit that encodes multiple input lines into a smaller number of output lines, but with <sup>5</sup> priority function. It assigns a priority level to each input, and when multiple inputs are active, the output reflects only the highest priority input. This is different from a regular binary encoder, which may produce an undefined output when multiple inputs are active.

<sup>2</sup> In digital electronics, a combinational logic circuit which produces outputs in response to only one input among all those that may be activated at the same time is called a priority encoder. For this, it uses a priority system, and hence it is named so.

### <sup>5</sup> 8 to 3 Priority Encoder without priority:-

A priority <sup>12</sup> encoder 8 to 3 converts eight binary inputs into a 3-bit binary output, prioritizing the highest-order active input. If multiple inputs are active, the output represents the highest-priority input.

### <sup>5</sup> Block Diagram of 8 to 3 Encoder without priority:-



**Fig: 8 to 3 Encoder without priority**

The Block Diagram of 8 to 3 Encoder without priority consists of 8 inputs from  $I_7 - I_0$  and outputs from  $Y_2 - Y_0$ .

#### Working of 8 to 3 Encoder without priority:-

The working of 8 to 3 Encoder without priority is as follows,

1 When the input  $I_0$  is active high ( $I_0 = 1$ ) and all other inputs are active low ( $I_1 I_2 I_3 I_4 I_5 I_6 I_7 = 0000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 000.

1 When the input  $I_1$  is active high ( $I_1 = 1$ ) and all other inputs are active low ( $I_0 I_2 I_3 I_4 I_5 I_6 I_7 = 0000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 001.

1 When the input  $I_2$  is active high ( $I_2 = 1$ ) and all other inputs are active low ( $I_0 I_1 I_3 I_4 I_5 I_6 I_7 = 0000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 010.

1 When the input  $I_3$  is active high ( $I_3 = 1$ ) and all other inputs are active low ( $I_0 I_1 I_2 I_4 I_5 I_6 I_7 = 0000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 011.

1 When the input  $I_4$  is active high ( $I_4 = 1$ ) and all other inputs are active low ( $I_0 I_1 I_2 I_3 I_5 I_6 I_7 = 0000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 100.

1 When the input  $I_5$  is active high ( $I_5 = 1$ ) and all other inputs are active low ( $I_0 I_1 I_2 I_3 I_4 I_6 I_7 = 0000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 101.

1 When the input  $I_6$  is active high ( $I_6 = 1$ ) and all other inputs are active low ( $I_0 I_1 I_2 I_3 I_4 I_5 I_7 = 0000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 110.

Similarly, when the input  $I_7$  is active high ( $I_7 = 1$ ) and all other inputs are active low ( $I_0 I_1 I_2 I_3 I_4 I_5 I_6 = 0000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 111.

Truth Table : **8 to 3 Encoder** without priority:-

I7	I6	I5	I4	I3	I2	I1	I0	Y2	Y1	Y0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

Logic Diagram of **8 to 3 Encoder** without priority:-

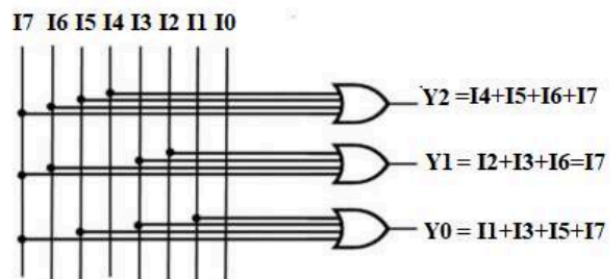
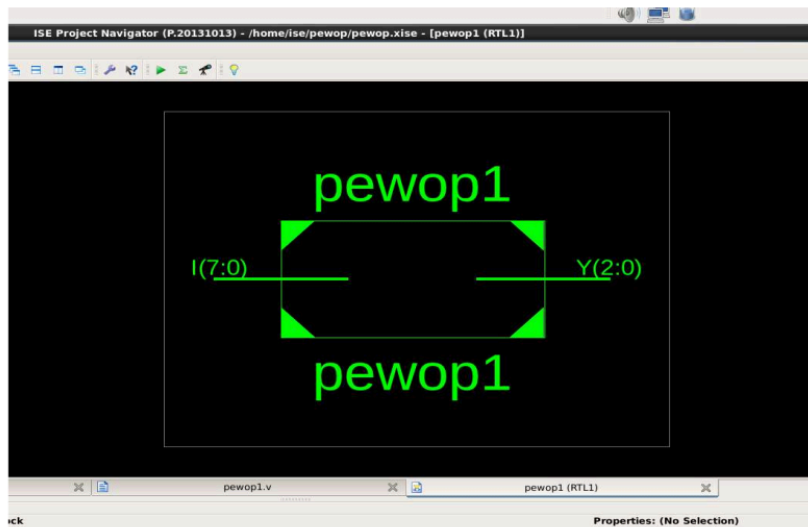
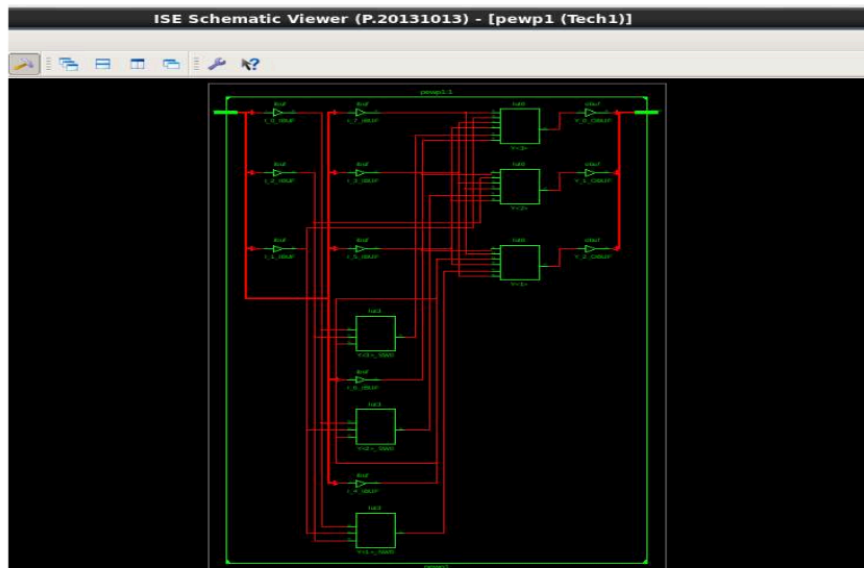


Fig: Logic Diagram of 8 to 3 Encoder without priority

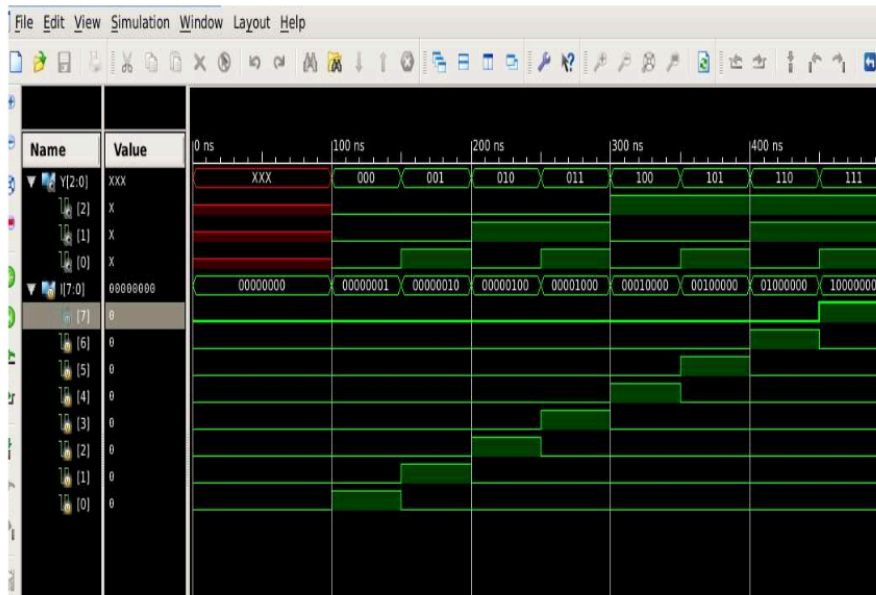
RTL schematic:- **8 to 3 Encoder** without priority



Technology schematic:- 8 to 3 Encoder without priority



Output Waveform: - 8 to 3 Encoder without priority



#### Timing Summary:- 8 to 3 Encoder withput priority

8  
Speed Grade: -3

Minimum period	No path found
Minimum input arrival time before clock	No path found
Maximum output required time after clock	No path found
Maximum combinational path delay	1.679ns

#### Device utilization summary:- 8 to 3 Encoder withput priority

3

Selected Device: 7a100tcsg324-3

<b>Slice Logic Utilization:</b>	
Number of Slice LUTs:	6 out of 63400 0%
Number used as Logic:	6 out of 63400 0%
<b>Slice Logic Distribution:</b>	
Number of LUT Flip Flop pairs used	6
Number with an unused Flip Flop	6 out of 6 100%
Number with an unused LUT	0 out of 6 0%
Number of fully used LUT-FF pairs	0 out of 6 0%
Number of unique control sets	0
<b>IO Utilization:</b>	
Number of IOs	11
Number of bonded IOBs	11 out of 210 5%

**Primitive and Black Box Usage:- 8 to 3 Encoder without priority**

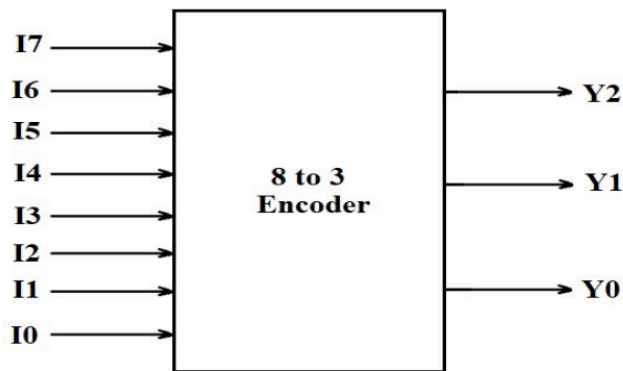
#BELS	6
#LUT3	3
#LUT6	3
# IO Buffers	11
# IBUF	8

5

**8 to 3 Priority Encoder with priority:-**

A priority encoder 8 to 3 converts eight binary inputs into a 3-bit binary output, prioritizing the highest-order active input. If multiple inputs are active, the output represents the highest-priority input.





**Fig: 8 to 3 Encoder with priority**

### Working of 8 to 3 Encoder with priority:-

The working of 8 to 3 Encoder with priority is as follows,

When the enable input is active low ( $en = 0$ ):

When all the other inputs are active low ( $I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7 = 00000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes ZZZ (High impedance state).

When the enable input is active high ( $en = 1$ ):

When all the other inputs are active low ( $I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7 = 00000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes XXX.

When the input  $I_0$  is active high ( $I_0 = 1$ ) and all other inputs are active low ( $I_1 I_2 I_3 I_4 I_5 I_6 I_7 = 00000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 000.

When the input  $I_1$  is active high ( $I_1 = 1$ ) and all other inputs are active low ( $I_0 I_2 I_3 I_4 I_5 I_6 I_7 = X0000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 001.

When the input  $I_2$  is active high ( $I_2 = 1$ ) and all other inputs are active low ( $I_0 I_1 I_3 I_4 I_5 I_6 I_7 = 0X000000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 010.

When the input  $I_3$  is active high ( $I_3 = 1$ ) and all other inputs are active low ( $I_0 I_1 I_2 I_4 I_5 I_6 I_7 = 00X00000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 011.

When the input  $I_4$  is active high ( $I_4 = 1$ ) and all other inputs are active low ( $I_0 I_1 I_2 I_3 I_5 I_6 I_7 = 000X0000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 100.

When the input  $I_5$  is active high ( $I_5 = 1$ ) and all other inputs are active low ( $I_0 I_1 I_2 I_3 I_4 I_6 I_7 = 0000X000$ ) then the output ( $Y_2 Y_1 Y_0$ ) becomes 101.

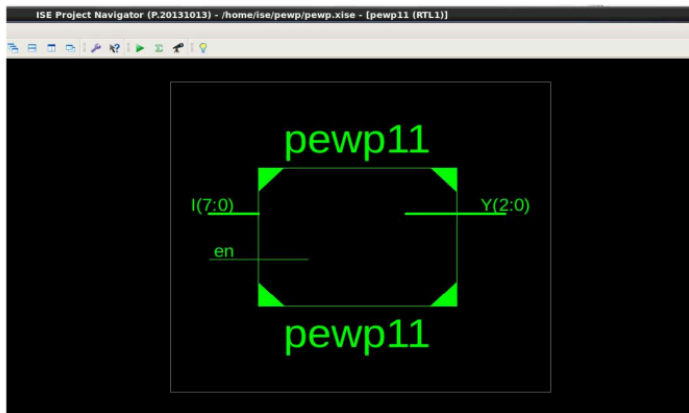
When the input  $I_6$  is active high ( $I_6 = 1$ ) and all other inputs are active low ( $I_0I_1I_2I_3I_4I_5I_7 = 00000X0$ ) then the output ( $Y_2Y_1Y_0$ ) becomes 110,

Similarly, when the input  $I_7$  is active high ( $I_7 = 1$ ) and all other inputs are active low ( $I_0I_1I_2I_3I_4I_5I_6 = 000000X$ ) then the output ( $Y_2Y_1Y_0$ ) becomes 111.

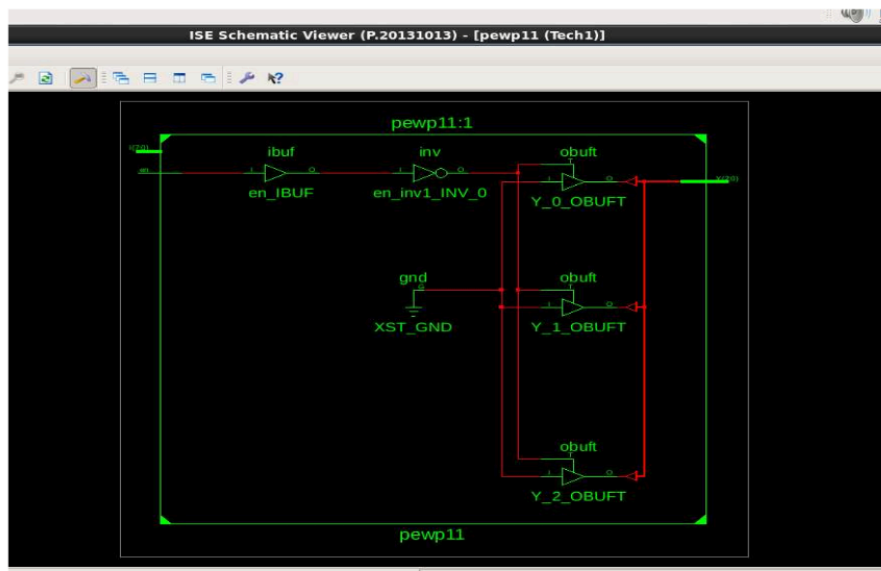
#### Truth Table :- 8 to 3 Encoder with priority

en	I7	I6	I5	I4	I3	I2	I1	I0	Y2	Y1	Y0
0	0	0	0	0	0	0	0	0	Z	Z	Z
1	0	0	0	0	0	0	0	0	X	X	X
1	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	1	X	0	0	1
1	0	0	0	0	0	1	X	X	0	1	0
1	0	0	0	0	1	X	X	X	0	1	1
1	0	0	0	1	X	X	X	X	1	0	0
1	0	0	1	X	X	X	X	X	1	0	1
1	0	1	X	X	X	X	X	X	1	1	0
1	1	X	X	X	X	X	X	X	1	1	1

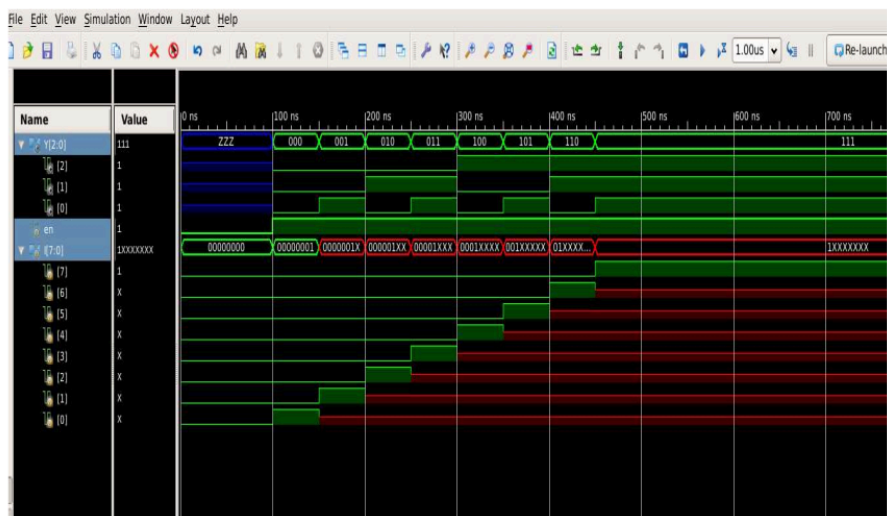
#### RTL schematic: - 8 to 3 Encoder with priority



**Technology schematic: - 8 to 3 Encoder with priority**



**Output Waveform: - 8 to 3 Encoder with priority**



**Timing Summary: - 8 to 3 Encoder with priority**

**9**  
Speed Grade: -3

Minimum period	No path found
Minimum input arrival time before clock	No path found
Maximum output required time after clock	No path found
Maximum combinational path delay	0.682ns

**Device utilization summary:- 8 to 3 Encoder with priority**

**4**  
Selected Device: 7a100tcsg324-3

<b>Slice Logic Utilization:</b>	
Number of Slice LUTs:	1 out of 63400 0%
Number used as Logic:	1 out of 63400 0%
<b>Slice Logic Distribution:</b>	
Number of LUT Flip Flop pairs used	1
Number with an unused Flip Flop	1 out of 1 100%
Number with an unused LUT	0 out of 1 0%
Number of fully used LUT-FF pairs	0 out of 1 0%
Number of unique control sets	0
<b>IO Utilization:</b>	
Number of IOs	12
Number of bonded IOBs	4 out of 210 1%

### Primitive and Black Box Usage:- 8 to 3 Encoder with priority

<sup>16</sup> #BELS	2
#GND	1
#INV	1
#IO Buffers	4
#IBUF	1
#OBUFT	3

### Conclusion:-

In this paper priority encoders (8 to 3) with and without priorities was implemented and simulated and synthesized using Verilog. RTL and Technology schematics were obtained. Device Utilization Summary, Timing Summary and Primitive and Black Box Usage were summarized.

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