ISSN: 2320-5407

International Journal of Advanced Research

Publisher's Name: Jana Publication and Research LLP

www.journalijar.com

REVIEWER'S REPORT

Manuscript No.: **IJAR-53090** Date: 02-08-2025

Title: 8 TO 3 PRIORITY ENCODERS

Recommendation:
Accept as it is .....
Accept after minor revision.....
Accept after major revision .....
Do not accept (*Reasons below*) .....

Rating	Excel.	Good	Fair	Poor
Originality			✓	
Techn. Quality			✓	
Clarity		✓		
Significance			✓	

Reviewer Name: Mr Bilal Mir

Reviewer's Comment for Publication.

Abstract Evaluation:
The abstract introduces the central focus of the study, which is the implementation of 8-to-3 priority encoders with and without priority using Verilog. It provides a brief but relevant overview of Hardware Description Language (HDL) and its importance in digital circuit design, particularly for integrated circuits (ICs) and field-programmable gate arrays (FPGAs). The explanation of Verilog's role in modeling, designing, simulating, and synthesizing hardware is clearly stated, with an emphasis on its application in industry for FPGA and ASIC development. The abstract situates the paper within the context of digital system design and gives a succinct description of the work undertaken.

Keywords Assessment:
The keywords—*FSM, HDL, Verilog, IEEE, IC, FPGA*—are relevant to the topic, accurately representing the paper's scope and technical domain. They are suitable for academic indexing and research retrieval.

Introduction Evaluation:
The introduction expands on the role of HDL in digital hardware design, simulation, and synthesis. It explains the abstraction levels supported by HDLs and highlights their utility in verifying circuit behavior before fabrication. The description of Verilog is clear and concise, outlining its structured approach to hardware design and its ability to model both connections and behavior. The mention of test benches underscores the importance of functional verification in the design process. The introduction also points out the synthesis process, linking Verilog code to its eventual hardware realization in the form of logic gates and their interconnections.

Overall Assessment:
The paper demonstrates a well-defined technical focus on digital circuit implementation using Verilog. Both the abstract and introduction effectively contextualize the study within the field of hardware design

ISSN: 2320-5407
International Journal of Advanced Research
Publisher's Name: Jana Publication and Research LLP
www.journalijar.com

REVIEWER'S REPORT

and digital electronics. The content maintains technical accuracy, logical structure, and an appropriate academic tone for an engineering and technology research audience.