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RESEARCH ARTICLE

TSPC Based State Look Ahead Counter

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Abstract

The speed of the circuit is one of the important performance factors, which determines the overall efficiency of the circuit. The selection of best counter topology is essential since counters are the basic building blocks of memory select management, code generators, shifters, frequency dividers and various arithmetic operations. TSPC based state look ahead counter is the best counter architecture when considering area, power consumption, speed, skew and operating frequency. This counter topology has two paths: - State look ahead path and Counting path. Both these path uses True single Phase (TSPC) D Flip-flop which is the main attraction of the entire Counter Architecture .This structure uses only three blocks in a repeated fashion so the design time of the counter is reduced compared to conventional synchronous counter. The proposed counter is designed in 180nm CMOS technology and simulated using Cadence Virtuoso software.

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Introduction

Counters are the basic building block of memory select management, code generators, frequency dividers and various arithmetic operations, so it is essential to build an efficient counter architecture. There are various factors which affects the overall performance of the counter. Speed, area, power consumption and operating frequency are the performance factors which help to find the best counter topologies.

The proposed TSPC based state look ahead counter consist of two paths: - Counting path and State look ahead path. The main attraction of this counter topology is that, it uses True Single Phase (TSPC) D Flip Flop in all Paths which adds advantages of low transistor count and skew tolerant structure. As it name indicate TSPC DFF is a Flip-flop which uses only clock signal and it doesn`t uses the inverted Clock signal. So the skew problem commonly found in many flip-flop structures can be avoided. Even though there are many varieties of D Flip-flop topologies are available another attracting feature of this TSPC DFF is low transistor count .Because of these merits the entire counter architecture has high speed, reduced area ,less design time ,skew tolerant and low power consumption.

8 Bit Counter Topology

The counter architecture consist of two paths state look ahead path and counting path. Counting path is responsible for counting the next higher order bits and state look ahead path prepares the counting path`s next counter state prior to the clock edge such that the clock edge triggers all the modules simultaneously. So both state look ahead path and counting path works together for entire counter working. Figure 1 represents the 8 bit counter topology .The counter architecture

consist of three blocks – Block 1, Block 2 and Block 3s where s=1, 2, 3. These blocks can be arranged in a repeated fashion in order to build the entire counter topology. Thus the design time of this counter reduced rather than a conventional synchronous counter. In the case of conventional synchronous counter when the counter width increases the design time as well as complexity increases, but no such problem exists in this proposed counter.

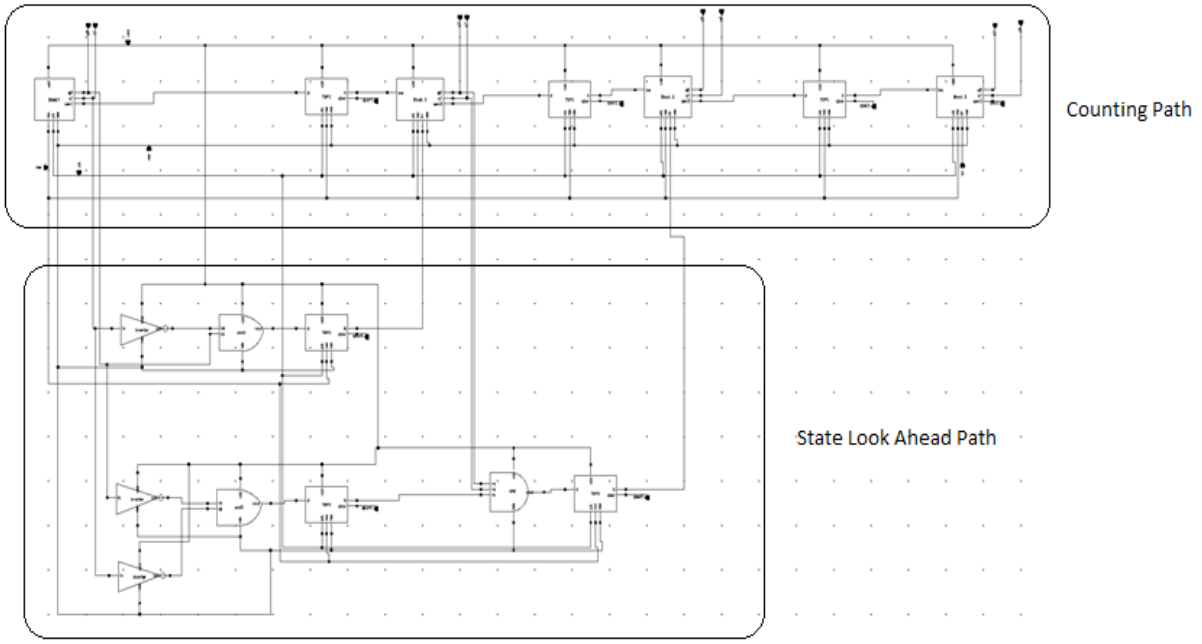

Figure 1: 8 Bit TSPC Based State Look Ahead Counter

The individual circuit diagram of Block 1, Block 2 and Block 3S are shown in figure 2 and 3. The Block 2 is True Single phase clock D Flip-flop, which is a common unit used in Block 1 and Block 3S.

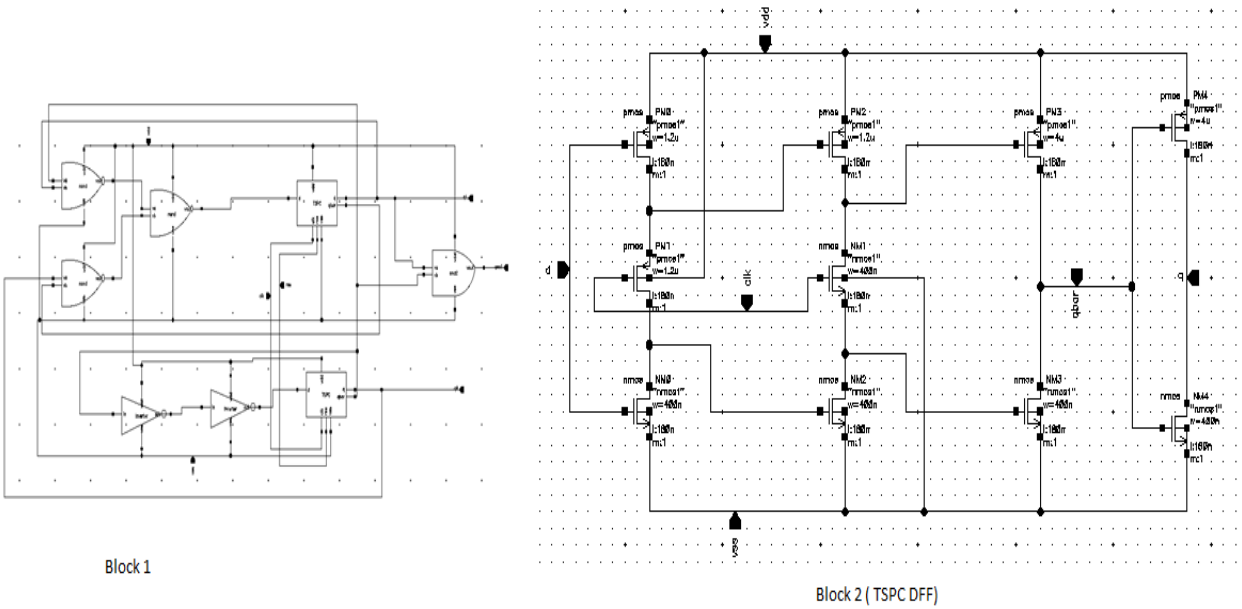

Figure 2: Circuit Diagram of Block 1 and Block 2

Block 1 is a standard parallel synchronous binary two bit counter, which is responsible for lower order counting bits. This block is also used to enable the Block 3S by incorporating with the state look ahead path.The state diagram of Block 1 is shown in figure 4 , After reset whenever the positive clock edge comes it changes the state. Block 2 is a positive edge triggered TSPC DFF. The block 2 in counting path act as a pipeline between block 1 and block 31 and subsequent block 3s.

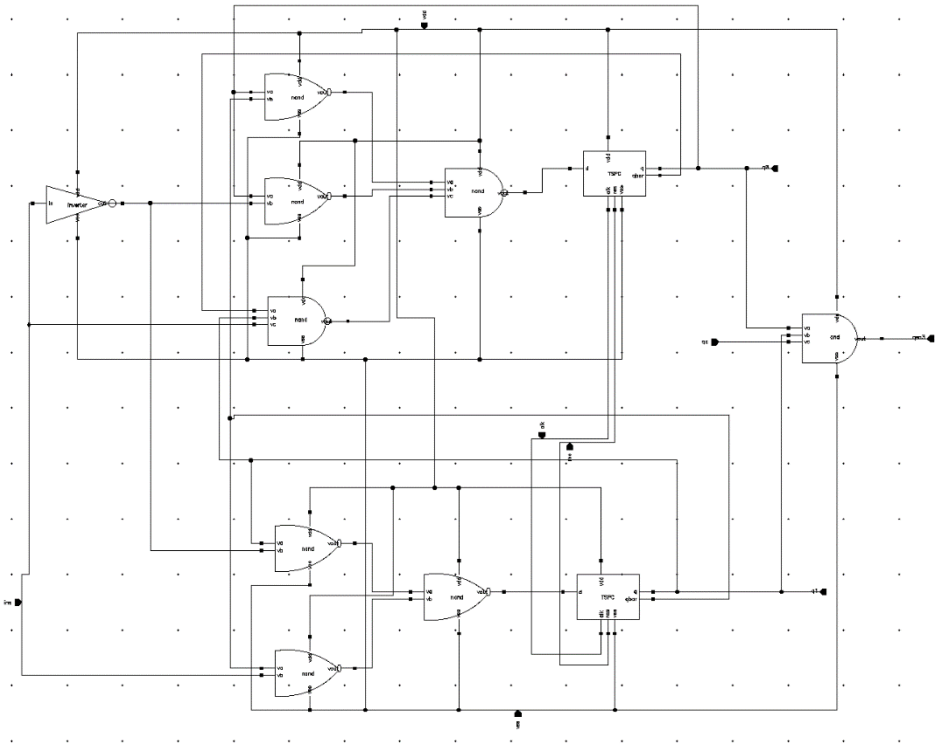

Figure 3: Circuit Diagram of Block 3S

Block 3S is a parallel synchronous binary 2 bit counter but it has an enable called INS. According to the INS it changes the state. After the reset with respect to the positive clock edge and INS the counter state changes which is shown in figure 4.

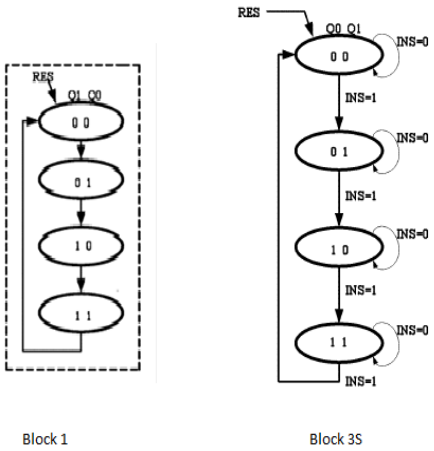

Figure 4: State Diagram

Results and Comparison

The proposed counter is designed in Cadence Virtuoso Software, in 180nm technology. The simulation waveform of 8 bit TSPC based state look ahead counter is shown in figure 5. After reset according to the positive edge of clock signal the counter changes the output, "q0q1q2q3q4q5q6q7" represents the counting bits of the proposed counter.

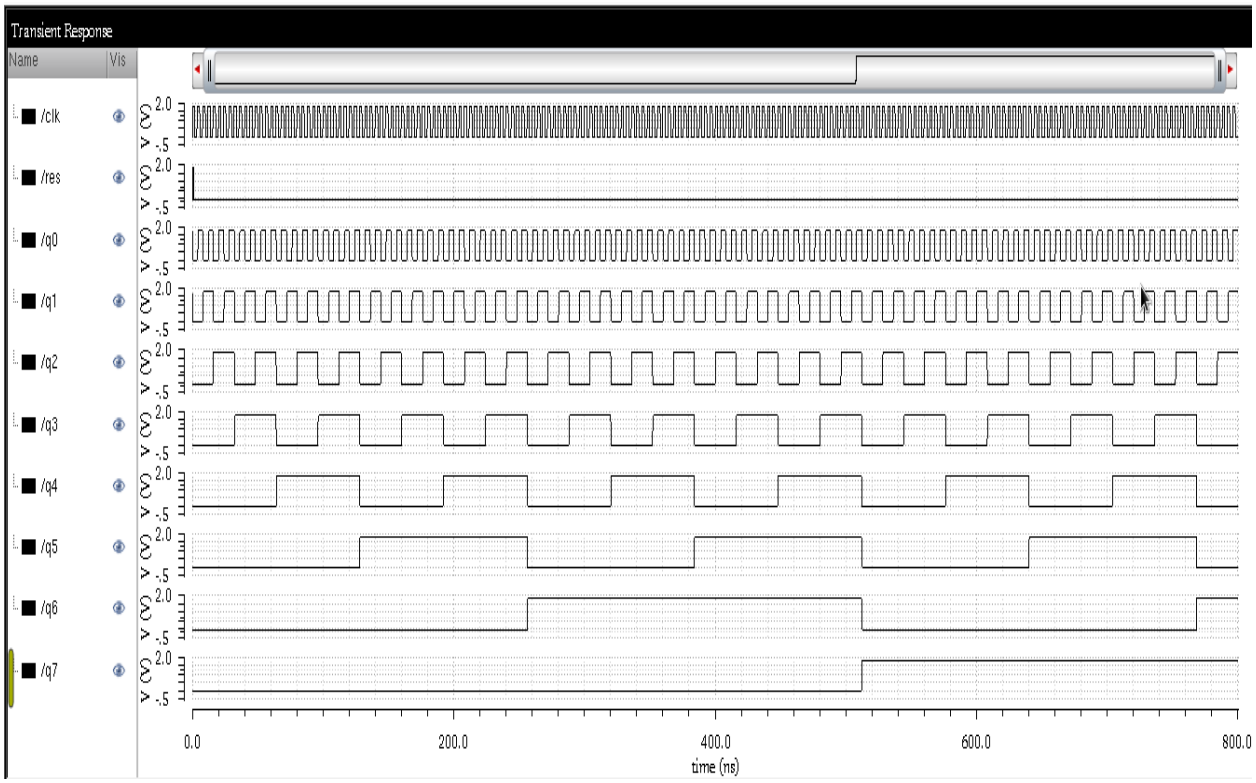

Figure 5: Simulation waveform 8 bit TSPC State Look Ahead Counter

The comparison of conventional counter, state look ahead counter and TSPC based state look ahead counter is performed, in order to find out the best counter architecture. To perform comparison, various parameters such as delay, power, transistor count, power delay product and operating frequency are measured.

The comparison result is shown in figure 6. From the comparison results, it can be reach the conclusion that TSPC based state look ahead counter is a best counter architecture among the three counter architectures. It can be seen that power delay product is very low for the proposed counter architecture, even though the delay of the proposed counter is greater than state look ahead counter. The transistor count of the new counter is also very less so the area of the design gets reduced in a significant amount. So TSPC based state look ahead counter is the best counter topology in all aspects.

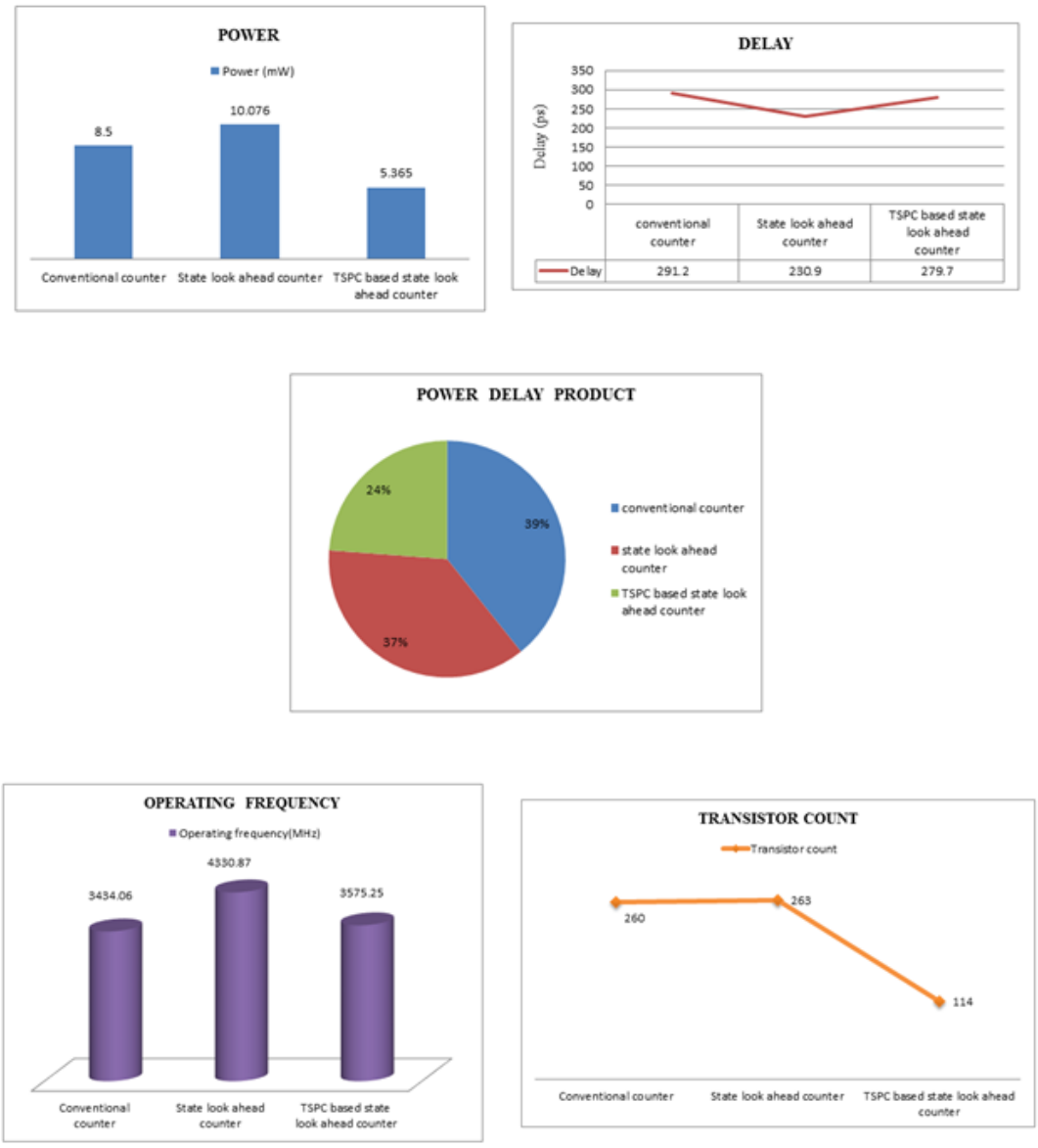

Figure 6: Comparison of performance parameters

Conclusion

The proposed TSPC based state look ahead counter is a simple counter structure which uses digital CMOS gate logic components. This architecture consists of three predefined blocks, block 1, block 2 and block 3S which are arranged in a repeated manner in order to realize the entire counter topology. So the counter design time get reduced compared with conventional counters. Also the main attraction of this topology is the use of TSPC based D Flip Flop. The True single phase clock (TSPC) DFF used, in the counter's architecture provides several merits than existing state look ahead counter: - The number of transistor count and power delay product get reduced, Due to use of single clock signal for DFF operations, the clock skew problem also avoided.

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