ISSN NO. 2320-5407

Journal homepage: http://www.journalijar.com

INTERNATIONAL JOURNAL OF ADVANCED RESEARCH

RESEARCH ARTICLE

A Current Copier Latch Circuit as Current-mode Information Storage

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Manuscript Info

Manuscript History:

Received: 14 October 2015
Final Accepted: 26 November 2015
Published Online: December 2015

Key words:

Current-mode circuits;
Analog signal processing;
Information storage

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Abstract

A new current copier latch circuit is proposed. The circuit employs positive feedback for improved performance and robustness to voltage variations at storage node. Circuit configuration allows faster response at switching times compared to previous designs with reduced dependence on input current level.

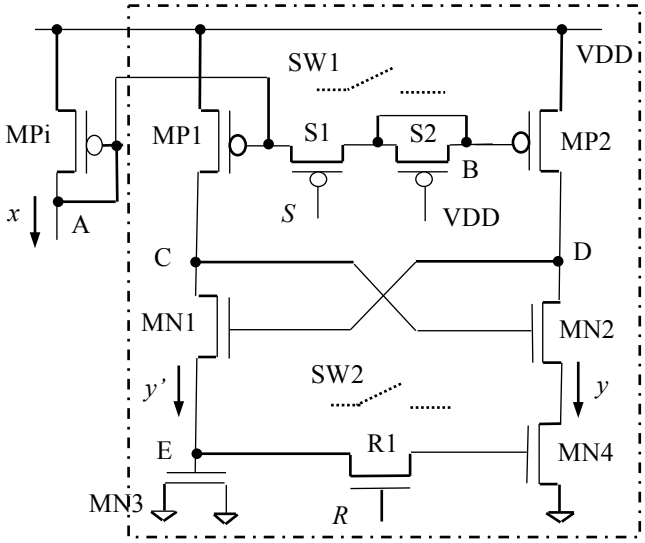
Introduction

Latching is an important and fundamental operation in varying applications such as filtering, analogue-to-digital conversion. Iterative weight-update with each sample input in training neural networks, [1]-[3], and system modeling in control, [4]-[5], are some of the examples of latching and can be implemented as analog structures. Voltage-mode latch designs based on current-mode logic (CML) in [6]-[7] latch a voltage input by switching a bias current between differential-pair and positive-feedback circuits, the latter consisting of two cross-coupled transistors to increase the speed of operation. On the other hand, current-mode design allows for simpler circuit realizations even implementing discretized hybrid design, e.g. multi-valued higher-radix circuitries, [8]-[10]. However, current-mode latch as storage is an involved design issue. Latching a current-mode input for high-speed, low-voltage operation is generally realized by using current copier or dynamic current-mirror structure with switched-current (SI) method, [11]. In this realization, the input current is sampled and copied (stored/held) in the form of voltage at a capacitive node switched by a synchronization signal, e.g. clock. However, use of current mostly involves a feedback for maintaining the stored voltage at the respective node and restoring it into the original input current value. For example, current copier circuit in [12] employs a multi-phase clock scheme and a negative feedback circuitry with amplification. The circuit in [13] employs a Wilson current mirror where the input current is converted into a feedback voltage at one phase of the clock. At the reverse phase, the stored voltage forces a path for copied version of the input current. Another SI design in [14] relies on switching a transistor between states at a capacitive node and a current source in respective clock phases. In most designs above, the output current needs to be provided at alternative path while holding the input current during the same clock phase. Moreover, the issues concerning the performance dependence on input current, charge injection, and clock feed-through should be considered. A current copier cell description to alleviate these problems is given by [15] with two separate clock signals along with their respective shifted and inverted forms.

In this study, we propose a new, simple-architecture current-mode latch circuit based on copying input current. The circuit exploits positive feedback for fast capture of the input current. The scheme allows the voltage at storage node to be robustly maintained, hence compensating the effect of such distortions as charge injection and clock feed-through. The configuration also reduces the dependency of dynamic performance on input level.

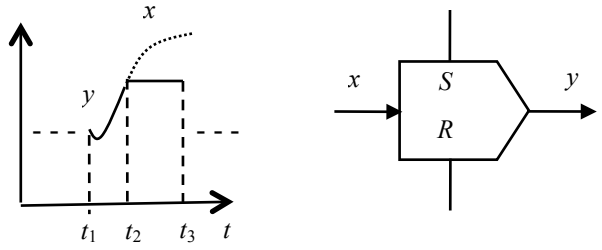
Description of the Proposed Circuit

New current-mode latch circuit is shown in Fig. 1 where cross-coupled transistors MN1 and MN2 form the positive-feedback circuit. Switch SW1 consists of transistors S1 and S2. Transistor S2 acts as a capacitance for reducing charge injection and feed-through when S1 is turned on/off.



Transistor	MP1 - 2	MN1 - 2	MN3 - 4	R1 - S1 - S2
W' / L'	3 / 2 – 18 / 3	3 / 12 – 12 / 3	8 / 3	18 / 3 – 3 / 2 – 3 / 2

(a)



(b)

Fig. 1. (a) New current-mode latch (in dashed box) and transistor aspect ratios (in table) with (W', L') = (W_{true} , L_{true}) / 0.12μm; (b) its expected transient response *y* in solid for input *x* in dashed lines(left)and block representation with switching signals S and R (right).

Let us, initially, assume that node E and drain of MN4 are short-circuited to ground and SW1 and SW2 are closed at $t = t_1$, each represented by negligible on-state channel resistances of switch transistors S1 and R1,

respectively. Then, MP1 and MP2 start to conduct, which builds up the gate voltages of MN1 and MN2 as their respective loads. In case $(W/L)_{MN1} < (W/L)_{MN2}$, an input current variation δx causes voltage variations δv_C and δv_D at nodes C and D, respectively. Because of differing channel resistances of MN1 and MN2, it will be seen that $\delta v_C > \delta v_D$. Reduced drain voltage of MN2 increases the drain voltage of MN1 that re-reduces the drain voltage of MN2 and so on. Overall voltage variations will push the voltage at node C toward VDD, which also charges associated total capacitance seen at this node. As a result, MP1 ceases providing a current, i.e. $y' = 0$. Because MP1 is forced to cut-off, it can be sized arbitrarily small. On the other hand, during this build-up phase, total capacitance seen at the gate of MP2, node B, is charged to a voltage level determined by input current, x. The stored voltage at node B keeps MP2 in conduction with saturation after SW1 opens at $t = t_2$ as a current source providing $y(t_2)$for $t > t_2$. Increased voltage at the drain of MN1 forces MN2 into linear-mode with a smaller channel resistance.

In case transistors MN3 and MN4 are included as shown in Fig. 1 and SW1 and SW2 are closed at $t = t_1$ the voltage at node E will resort to a value during build-up with $y' \neq 0$. As a result, MN4 enters linear mode. Therefore, the drain voltage of MN4 will follow the voltage at node D. When SW2 opens, MN4 is driven into cut-off through source-to-gate capacitance of R1 rapidly due to reduced excessive charge at its gate that is shared with MN3 just before SW2 has opened. Therefore, assuming $(W / L)_{MPi} = (W / L)_{MP2}$, input-output relationship of the circuit is as follows:

$$y(t) = \begin{cases} x(t) & t_1 < t \le t_2 \text{ with SW1 \& SW2 closed} \\ x(t_2) & t_1 < t \le t_2 \text{ with SW1 open \& SW2 closed} \\ 0 & \text{for all } t \text{ with SW2 open} \end{cases} \quad (1)$$

In the proposed design, charging and discharging behavior, particularly at node B determines the speed of the operation. When S is low, i.e. logic 0, at $t = t_1$, transistor S1 is assumed to operate in linear mode with negligible channel resistance. In this case, the capacitance at node B will charge with a time-constant roughly given by $\tau_B \approx C_B / g_{mi}$ where g_{mi} is small-signal transconductance of MPi while C_B is the total capacitance seen at node B. Although both C_B and g_{mi} are dependent on size and biasing as well as technological parameters used, the circuit configuration adopted here reduces these dependencies: For example, transconductance parameter g_{mi} can be expressed in terms of variations in input current x, δx, and voltage at node B, hence D, δv_B and δv_D, respectively, as

$$g_{mi} = \delta y / \delta v_B \approx |K_v| \, \delta x / \delta v_D \quad (2)$$

In (2), $|K_v|$is the voltage gain between nodes D and B. Given K_v and δx, it is seen that as δv_D is kept smaller, τ_B becomes smaller. As explained previously, by using MN3 and cross-coupled transistors MN1 and MN2 with $(W / L)_{MN1} < (W / L)_{MN2}$, the voltage at node C is forced toward VDD and is kept almost constant. Due to minimized voltage variation at node C, δv_D is also minimized. The circuit configuration allows choosing MP1 arbitrarily small. Thus, the contribution to τ_B via MP1 can also be kept at a minimum. In the circuit, the size of S2 is chosen to optimize the transient response while reducing feed-through and charge injection.

Simulation with Proposed Circuit

Proposed latch circuit and predecessors in [12]-[15] were designed and simulated for comparison using TSMC 0.25μm HSPICE (level - 49) parameters in full post-layout extraction with 1.8V supply voltage. In designs where R input is not available, the respective design was modified by adding an extra PMOS transistor of W / L = 2.06μm / 0.36μm on output current path to be switched by input R for resetting. A digital clock (CLK) signal of 100 MHz and reset signal of 25 MHz were applied to S and R inputs, respectively, as shown in Fig. 2. In all designs, body-biased effects were included and transistors were sized for optimum transient performance. For design in [12], CLK signal and its non-overlapped inverted version (I_CLK) with slight modification to pulse-width were used. In realization of the latch corresponding to [15], CLK and I_CLK were ANDed with their respective 1/2 period shifted versions and these four clock signals were applied to the circuit. HSPICE transient simulation results for the proposed circuit are illustrated in Fig. 2 with indicated waveforms of input current x andpreviously describedswitching S and R inputs.

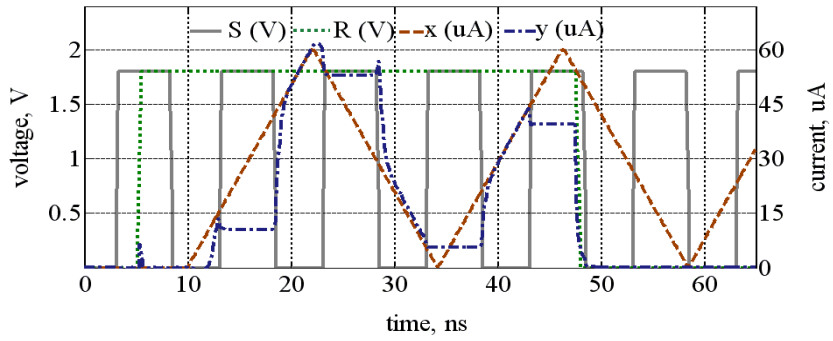


Fig. 2. Transient simulation results of proposed latch circuit.

The circuits were investigated in terms of the following dynamic performance measures: *Settling-time* (τ_s) was defined as the time duration, when $R = 1$, for y to reach the range $x \pm \Delta$ after S has risen to/fallen down to 0.5VDDor while $S = 0$. *Resetting-time* (τ_r) was defined as the time duration for y to decay to the lowest value, i.e. below Δ after R has fallen down to 0.5VDD. The parameter Δ is utilized to account for total effect of charge redistribution, design discrepancies etc. after a state transition in S and R and it is taken 1.5μA. Following table presents some important design characteristics with performance measures in average for the designs investigated.

Design	# of Trans.	Avg. τ_s - τ_r	Avg. Power Diss. (mW)	Layout Area, $(\mu m)^2$
New	9	1.4 - 1.6	0.23	8.3
[12]	15	2.3 - 2.6	0.30	13.3
[13]	8	1.7 - 2.0	0.21	8.2
[14]	8	1.9 - 1.9	0.26	7.9
[15]	18	2.4 - 2.7	0.33	15.1

Table I. Performance and design characteristics of proposed, (New), and previous current copier latch circuits.

Conclusions

A new current-mode latch circuit described. Major characteristics of the new circuit are fast operation, reduced sensitivity of circuit performance to input variation and secondary effects such as charge injection. Its improved performance and simplicity are expected to allow it to be utilized in more complicated designs such as flip-flops.

Acknowledgement

This work was supported by The Scientific and Technical Research Council of Turkey (TUBITAK) under the project no: 107E059.

References

[1] R. Kozma, C. Horvath, G. Hosszu, and F. Kovacs, "A low-power current-mode correlation detector with analog data storage," Proc. IEEE TENCON, vol. 2, pp. 442-445, 2004.

[2] T. Temel, and B. Karlik, "An improved odor recognition system using learning vector quantization with a new discriminant analysis," Neural Network World, vol. 17, no. 4, pp. 287-294, 2007.

[3] T. Temel, "A New Generalized Learning Vector Quantization Classifier Algorithm with Sliding-mode Optimized Training," Int. Journal of Advanced Research, vol. 3, no. 7, pp. 678-683, 2015.

[4] T. Temel, and H. Ashrafiuon, "Sliding-mode control approach for faster tracking," IET Electronics Letters, vol. 48, no. 15, pp. 916-917, 2012.

[5] T. Temel, and H. Ashrafiuon, "Sliding-mode speed controller for tracking of underactuated surface vessels with extended Kalman filter," IET Electronics Letters, vol. 51, no. 6, pp. 467-469, 2015.

[6] R. Huang, J. S. Wang, and C. L. Wey,"A fully differential current copier for performance improvement," Wiley Int. Journal Circuit Theory and Applications,vol. 28, no. 2, pp. 101-108, 2008.

[7] P. Heydari, and R. Mohavavelu,"Design of ultrahigh-speed low-voltage CMOS CML buffers and latches," IEEE Trans. Very Large Scale Integration (VLSI) Systems, vol. 12, no. 10, pp. 1081-1092, 2004.

[8] T. Temel, "Current-mode CMOS Design of Multi-valued Logic Circuits," PhD Thesis, Bogazici University, Department of Electrical and Electronics Engineering, 2002.

[9] T. Temel, A. Morgul, and N. Aydin, "A Novel Signed Higher-Radix Full-Adder Algorithm and Implementation with Current-Mode Multi-Valued Logic Circuits," Proc. IEEE Euromicro Systems Symposium on Digital System Design(DSD 2004), pp. 80-87, 2004.

[10] T. Temel, "High-performance current-mode multi-input loser-take-all minimum circuit," IET Electronics Letters, vol. 44, no. 12, pp. 718-719, 2008.

[11] S. Daubert, J. Vallancourt, and Y. P. Tsividis, "Current-copier cells," IEE Electronics Letters, vol. 24, no. 25, pp. 1560-1562, 1988.

[12] G. Wegmann, and E. A. Vittoz,"Very accurate dynamic current mirrors,"IEE Electronics Letters,vol. 25, no. 10, pp. 644-646, 1989.

[13] C. Wang, M. O. Ahmad,M.N.S. Swamy,and A. Azelmad, "Low-switching-noise current copier," Proc. IEEE Canadian Electrical and Computer Engineering Conf. (CCECE 2000),vol. 2, pp. 7-10, March 2000.

[14] R. Wilcock, P. Wilson, and B. Al-Hashimi,"A novel switched-current phase locked loop,"Proc. IEEE Int. Symp. on Circuits and Systems, pp. 2815-2818, May 2005.

[15] J. Nakamura, B. Pain, T. Nomoto, T. Nakamura, and E. R. Fossum,"On-focal signal processing for current-mode active pixel sensors," IEEE Trans. Electron Devices,vol. 44, no. 10, pp. 1747-1758, 1997.