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RESEARCH ARTICLE

Design Automation and Verification of Step-Down DC-DC Converter for IC Based Boards

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Abstract

Quickly dropping power supply voltages and tight voltage regulation prerequisites for ICs difficulties power supply fashioners. A novel interleaved releasing (ID) methodology is introduced to diminish the ripple in step down switched capacitor (SC) dc–dc converters. Simulation and experimental of a four-stage SC dc–dc converter demonstrate that the ID methodology can diminish the ripple by a factor of three. The proposed approach additionally enhances the converter productivity by 7%. The ID strategy gives adaptability in the optimization and design of SC based DC-DC converters.

INTRODUCTION

Power supply voltages for integrated circuits (ICs) are being reduced steadily in an effort to increase integration densities and reduce power dissipation. According to the 2002 "International Technology Roadmap for Semiconductors" [1], by 2016, the supply voltage for high performance ICs will drop to only 0.4 V. Along with the plummeting supply voltages, the currents drained by ICs are going to be much higher due to increasing power requirements. This trend presents power supply designers with many tough challenges, such as supply efficiency, regulation, ripple, response time, size/weight, cost, power bus architecture, etc. [2], [3].

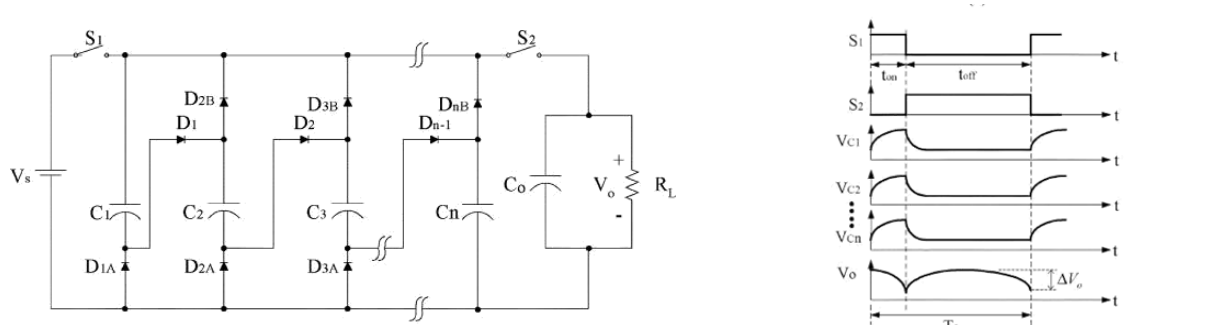
In applications such as computers, a higher voltage (e.g., 12 V) is more suitable for efficient power delivery, because of reduced resistive losses in the copper traces on printed circuit boards. The voltage delivered on-board needs to be converted into required supply voltages through voltage regulator modules (VRMs) [4]. Therefore, for future low-voltage applications, step-down (buck) dc–dc converters are becoming important. In conventional switch-mode power supplies (SMPSs), due to the use of magnetic components (inductors and transformers), it is difficult to achieve high power-density and low cost designs. In recent years, switched-capacitor (SC) dc–dc converters (also known as charge pumps) have gained increased attention [5]–[8]. There have already been many commercial products in use [9], [10]. The increasing popularity of SC dc–dc converters is mainly due to their unique features: they consist of only switches and capacitors, and energy transfer is achieved by controlling the charging and discharging process of the capacitors. Because no magnetic components are needed, SC dc–dc converters are amenable to single chip integration.

Thus far, output ripple issues in SC dc–dc converters have received only limited attention. In SMPSs, the percentage output voltage ripple is usually specified to be less than 1% [11]. The value of the output filter capacitance can be simply increased to meet the ripple specification, but this method may not meet low cost and high-power-density design requirements. Interleaving techniques have already been used in low-voltage high-current SMPSs to improve the power level [12]–[14], as shown in Fig. 1.The converter cells are physically paralleled and operated at the same switching frequency, but are phase-shifted by 2 with respect to one another. By interleaving paralleled converter cells, the input/output ripple can be reduced by a factor of 1 or better. The cost of this interleaving technique is increased component count and complicated control. The interleaving technique has also found use in SC dc–dc converters to reduce output ripple [7], [10].In Section II of this paper, conventional step-down SC dc–dc converters are first

reviewed, after which a new approach to reducing the output ripple is proposed, taking full advantage of the structure of step-down SC dc–dc converters. Steady-state analysis of the proposed converter is presented in Section III. Simulation results are provided in Section IV to demonstrate the effectiveness of the proposed approach. Experimental results are presented in Section V.

Proposed Interleaved Discharging Approach

A. *Conventional Step-Down SC DC–DC Converter*



(a) (b)

Fig. 2. Conventional n-stage step-down SC dc–dc converter. (a) Circuit. (b) Timing diagram and waveforms.

Fig. 2(a) shows the schematic of a conventional n-stage step-down SC dc–dc converter. Its timing diagram and some theoretical waveforms are shown in Fig. 2(b). In each switching cycle, the circuit goes through two different switching states. During T_{on}(S_1 closed; S_2open), capacitors C_1-C_n(called pump capacitors) are charged in series through S_1, and D_1 to D_n-$_1$The output capacitor C_0 supplies the load during this interval. During t_{off} (S_1open;S_2 closed), the pump capacitors are connected in parallel through diodes D_{1A}-$D_{n-1A}$and D_{2B} _D_{nB}, so that they can be discharged simultaneously to the load through S_2. The output voltage is ideally

$$V_o = \frac{V_s}{n} \dots\dots\dots\dots\dots\dots\dots\dots (1)$$

B. *Proposed Step-Down SC DC–DC Converter with Interleaved Discharging*

The proposed n-stage step-down SC dc–dc converter is shown in Fig. 3(a). Diodes D_{1A}-D_{n-1A} and $_{DnB\ in}$ Fig. 2(a) are replaced by power switches S_{1A}_ S_{n-1A} and S_{nB}. Fig. 3(b) shows the timing diagram and waveforms for the proposed SC dc–dc converter. The charging interval (during t_{on}) is the same as that of a conventional step-down SC dc–dc converter, i.e., capacitors C_1-C_n are still charged in series through S_1, and D_1 to D_{n-1}. However, unlike in a conventional step-down SC dc–dc converter where the pump capacitors are discharged simultaneously, in the proposed n-stage step-down SC dc–dc Converter the pump capacitors are discharged one by one, which is here termed interleaved discharging (ID). The ID method is realized by introducing a phase shift of $\frac{2\pi}{n}$ to each pump capacitor during the discharging interval (T_{off}). By investigating the voltage waveforms V_{c1}-V_{cn} in Fig. 3(b), it can be seen that while C_1 is being discharged (only S_{1A} and S_2 are on), the other capacitors remain charged, i.e., their voltages don't change. The similar process is repeated for the remaining capacitors until the end of T_{off}. Compared to Fig. 2(b), the output voltage V_O in Fig. 3(b) has higher frequency, with the same capacitors. Because the output voltage ripple is inversely proportional to the ripple frequency, the output ripple can be reduced. Fig. 3(c) and (d) show the circuit configuration during different switching states. Discharging intervals 2-n (not shown) are similar to Fig. 3(d), except include a phase shift of$\frac{2\pi}{n}$.The proposed ID method is different from the conventional interleaving technique previously shown in Fig. 1. This new ID method takes full advantage of the special structure of the step-down SC dc–dc converters, and it does not need any extra converter cells to be connected in parallel. The ID method does need some extra driving signals for the switches, but simple circuits such as flip-flops can be used.It should be pointed out that the power switches in Fig. 3(a) that replace the original diodes in Fig. 2(a) would not present difficulties since it is possible to integrate power switches on chip in low-power applications. In order to obtain high efficiency in low-voltage low-power applications, all of the diodes should be replaced by power switches. Also, floating diodes are difficult to realize in complementary metal-oxide semiconductor (CMOS) technology. For medium-power

conventional SC dc–dc converters, replacing the diodes with power switches can still improve the efficiency. Therefore, the above-mentioned conceptual topologies can be improved in practice. Fig. 4 shows the topology of a practical n-stage step-down SC dc–dc converter. Note that C_1 is the combination of the output capacitor C_o in Fig. 3(a)] and a pump capacitor, and thus one capacitor and one MOSFET (and its driving circuit) are saved When switches S_1,S_{2A} –S_{nA} are on, the capacitors are charged in series, and the input power supply also provides part of the load current. When S_i and S_{iB} are closed, pump capacitor C_1 will be discharged, where i= 2….,n, Both the conventional and pro-posed n-stage step-down SC dc–dc converters can be realized based on the topology shown in Fig. 4, according to the control algorithms just mentioned in subsections A and B. Thus, the topology shown in Fig. 4 will be assumed in the remainder of this paper.

Steady State Analysis

In this section, a steady-state analysis of Fig. 4 is presented, in order to provide insight on how the ID method reduces the output ripple. For simplicity of the analysis, parasitic parameters, such as MOSFET on-resistances and capacitor equivalent series resistances, are neglected.

A. Analysis of the Conventional n-Stage SC DC–DC Converter

For a conventional n-stage SC dc–dc converter based on the practical topology shown in Fig. 4, the waveform of its output voltage may be approximated in Fig. 5(a).V_1 And V_2 are the maximum and minimum output voltages respectively. T is the switching period

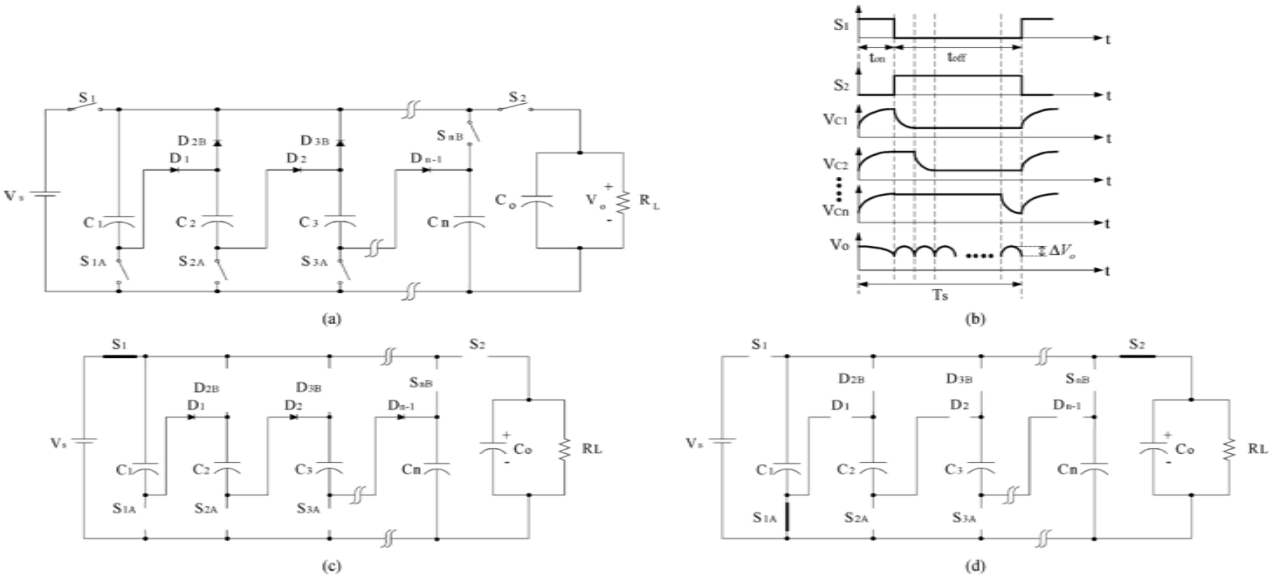


Fig. 3Proposed step-down SC dc–dc converter with ID. (a) Circuit. (b) Timing diagram and waveforms. (c) Charging interval. (d) Discharging interval.

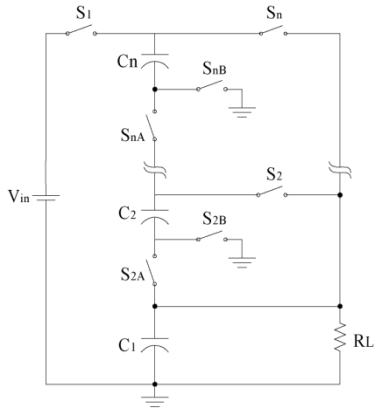


Fig. 4.Practical n-stage step-down SC dc–dc converter

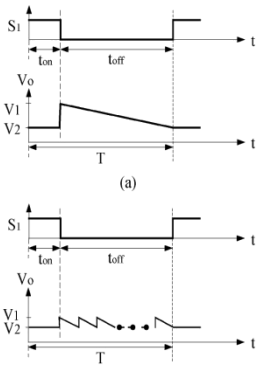


Fig. 5. Output voltage waveforms of the conventional and proposed step-down SC dc–dc converters based on the topology shown in Fig. 3. (a) Conventional Method (b) ID method.

The circuits has (n-1) capacitors, where c_i= c where i-2 …n, at the beginning of t_{off} by charge conservation we have

$$(n-1)c\frac{(v_{in}-v_2)}{(n-1)}-v_1=c_1(v_1-v_2)\ldots\ldots(2)$$

Let k=c/c_1, then

$$V_2=\frac{[1+(n-1)k]v_1-kv_{in}}{1-k}\ldots\ldots\ldots(3)$$

During t_{off}, the voltage v_0 changes from v_1 to v_2.

$$V2=V1e^{-\frac{(1-d)t}{\tau}}\cdots\cdots\cdots(4)$$

$$D=\frac{t_{on}}{t},T=R_L[C_1+C(n-1)]\cdots\cdots\cdots(5)$$

From Equation (3) & (4) we get

$$V_1=\frac{K\,V_{in}}{1+(n-1)k-(1-k)e^{-\frac{(1-d)T}{\tau}}}\cdots\cdots\cdots(6)$$

The output voltage ripple is V_R=V_1-V_2 therefore

$$V_R=\frac{k\,v_{in}e^{-\frac{(1-d)T}{\tau}}}{1+(n-1)k-(1-k)e^{-\frac{(1-d)T}{\tau}}}\cdots\cdots\cdots(7)$$

Approximating $e^{-\frac{(1-d)T}{\tau}}$ valve with [1-(1-d) T/τ]

$$V_R\approx\frac{k\,v_{in}\frac{(1-d)T}{\tau}}{1+(n-1)k-(1-k)e^{-\frac{(1-d)T}{\tau}}}\cdots\cdots\cdots(8)$$

Substituting (5) into (8), and using the switching frequency$f=(1/T)$, we obtain

$$V_R=\frac{v_{in}\,(1-d)}{nR_LC_1f+nR_L(n-1)Cf+(1-k)(1-d)/k}\cdots\cdots\cdots(9)$$

The average output voltage can be expressed as

$$V_{av}=V_2d+\frac{V_{1+V_2}}{2}(1+d)\cdots\cdots\cdots(10)$$

The converter efficiency is

$$\eta=\frac{V_{av}^2/R_L}{V_{in}I_{in}}\cdots\cdots\cdots(11)$$

$$I_{in}=\frac{V_2}{R_L}d\cdots\cdots\cdots(12)$$

B. Analysis of the ID-Based n-Stage SC DC–DC Converter

For an ID-based n-stage SC dc–dc converter based on the practical topology shown in Fig. 4, the waveform of its output voltage is approximated in Fig. 5(b), with V_1 and V_2 representing the maximum and minimum output voltages, respectively. The steady-state analysis is similar. At the beginning of T_{off}, by charge conservation, we have

$$C\left(\frac{V_{in}-V_2}{n-1}-V_1\right)=C_1(V_1-V_2)\cdots\cdots\cdots(13)$$

Note that only one pump capacitor is discharged each time, i.e., the left hand side of (13) should not be multiplied by (n-1) as in (2).

The discharging time for each pump capacitor is$\frac{t_{off}}{(n-1)}$. During this interval, the output voltage V_o changes from V_1 toV_2.

$$V_2=V_1e^{-\frac{(1-d)T}{(n-1)\tau'}}\cdots\cdots\cdots(14)$$

Where$\tau'=R_L(C_1-C)$.

The output ripple is obtained from (13) and (14)

$$VR = V1 - V2$$

$$V_R = \frac{kV_{in}\left(1 - e^{-\frac{(1-d)T}{(n-1)\tau'}}\right)}{(n-1)(1+k) - (n-1-k)e^{-\frac{(1-d)T}{(n-1)\tau'}}} \cdots\cdots\cdots (16)$$

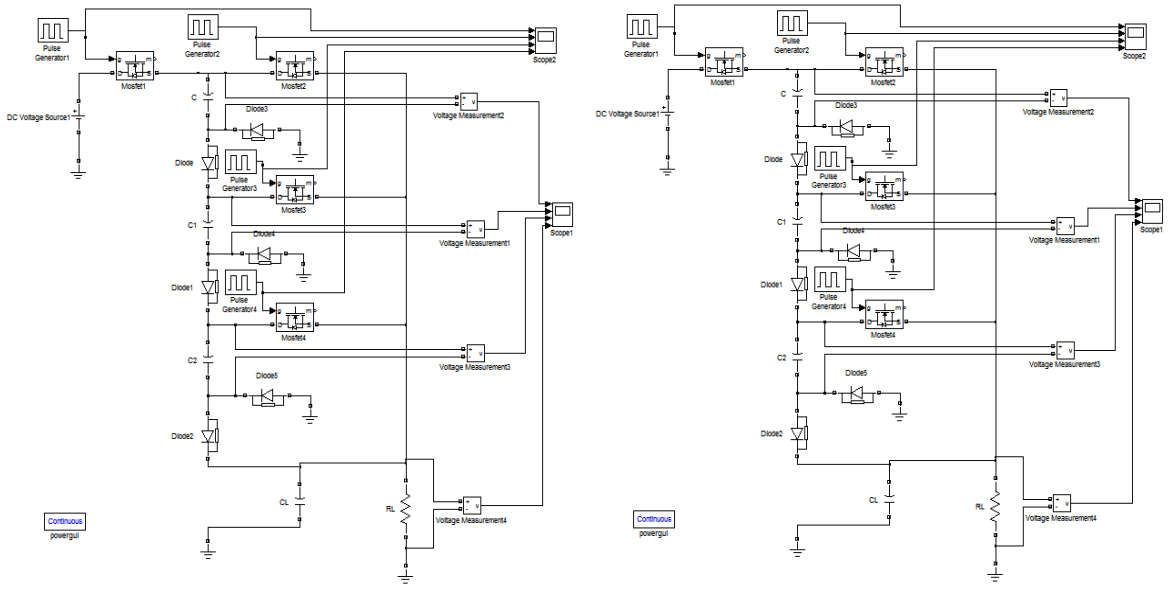
After approximation, we obtain

$$V_R = \frac{V_{in}(1-d)}{nR_L(n-1)C_1 f + nR_{L\,(n-1)Cf} + (n-1-K)(1-d)/k} \cdots\cdots\cdots (17)$$

The expressions of the average output voltage and converter efficiency are the same as (10) and (11), respectively. It can be observed that the first term in the denominator of (17) is (n-1) times of that of (9). Therefore, it is now clear that the ID method reduces the output ripple mainly by effectively increasing the product of C_{1f} by (n-1) times. For instance, if n=4, d=0.25, C=10 μF, C_1=200 μF, V_{in} =5V, the calculated output ripple for the conventional and proposed converters are 25.3 and 9.2 mV, respectively. Their efficiencies are both about 89%. However, in Section V we will see that the ID method actually improves the efficiency, if the parasitic parameters are also considered.

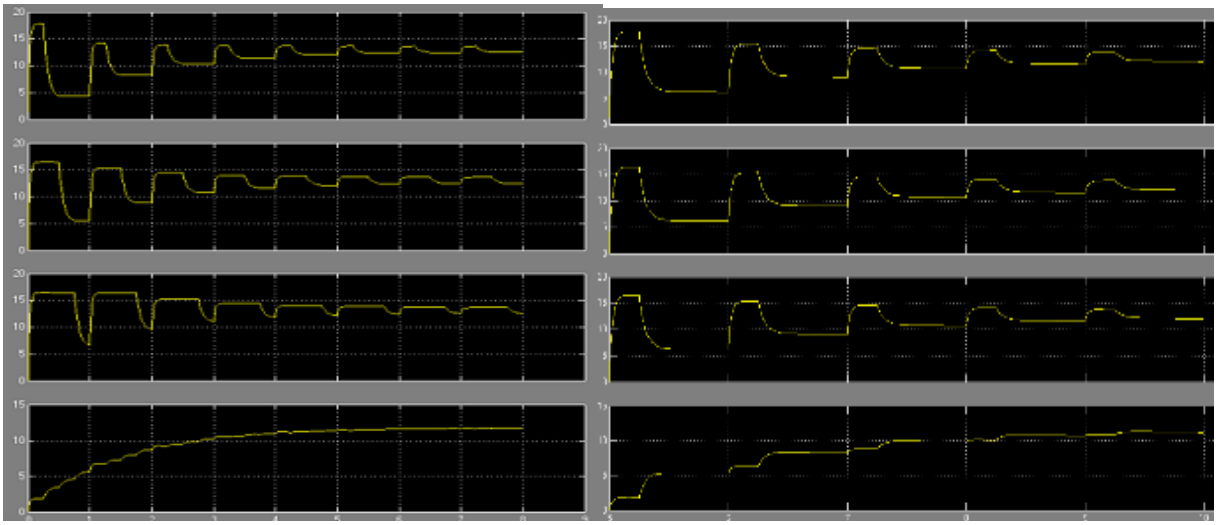
Verification of Simulation

In [6], a 48 W, 55 V/12 V switched-capacitor dc–dc converter was proposed, as shown in Fig. 6. This is the commonly used step-down SC topology. In this section, the proposed ID method is applied to this converter, which was chosen so that the detailed results provided in [6] may be referenced for comparison. Fig. 7 illustrates the MATLAB simulation waveforms without using the ID method. Fig. 8 shows the MATLAB simulation waveforms using the proposed ID method. Note that in Fig. 7(a) the voltage waveforms of C_2 to C_4 be in phase, which is the feature of conventional step-down SC dc–dc converters. In Fig. 7(b), a phase shift exists in the voltage waveforms of C_2 to C_4. After using the proposed ID method, the output ripple [Fig. 7(b)] is much smaller than that of a conventional step-down SC dc–dc converter, as shown in Fig. 7(a). The simulation results of both cases are tabulated in Table. 1. The results show that the proposed ID method can reduce the output ripple by a factor of three.



(a) (b)

Fig. 6. (a) MATLAB simulation circuit without ID method (b) with ID method.



(a) (b)

Fig. 7. (a) MATLAB simulation results without ID method (b) with ID method.

	Average output voltage (V)	Average input current (I)	Efficiency (%)	Output ripple (mV)
Without ID	11.98	1.0015	82.3	94
With ID	11.94	1.008	85.7	24

Table. 1 Simulated Performance Comparisons of A Step-Down SC DC–DC converter With And Without The Proposed Id Approach.

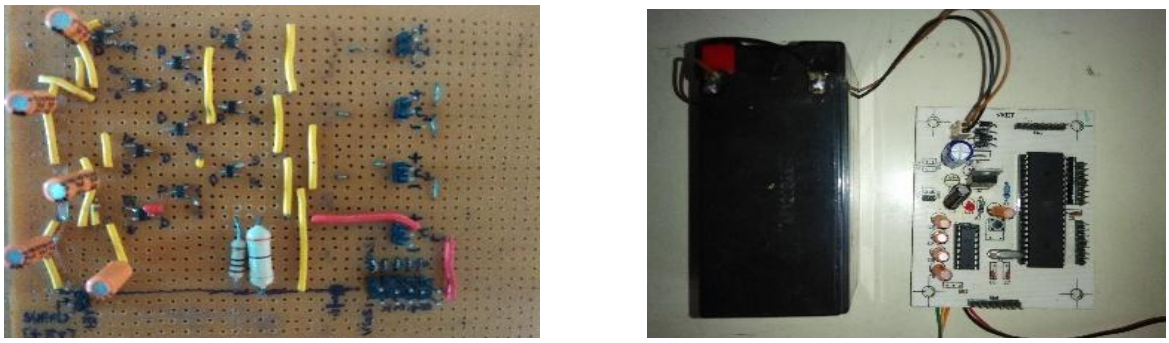
Experimental Results

A 5-V/1.1-V, 150-mA four-stage step-down SC dc–dc converter was built with discrete devices. The 5-V/1.1-V specs were chosen due to the common application in the low-voltage IC industry. Fig. 9 shows the converter topology. It can be observed that this topology is the same as that shown in Fig. 6, except that all of the diodes are replaced by MOSFETs. Since the proposed ID method only modifies the control algorithm, control circuits of a conventional SC dc–dc converter and an ID-based version were built on the same circuit board, utilizing the same power stage. A DIP switch was used to select whether the conventional or ID method is going to control the power stage. This arrangement makes possible a fair and accurate comparison between the two control methods.

In Fig. 8(a), to hardware of a proposed SC dc–dc converter, two anti-phase (i.e., 180o phase shift) pulse width modulation (PWM) signals are required: one for and the other for V_{gs1} and V_{gsa} and the other for V_{gs2}- V_{gs4}. To realize the ID method, four-phase PWM signals (90 phase shift between every two phases) are needed. A simple PLC based hardware circuitasshowninFig.8 (b) was designed to generate the required four-phase PWM signals. In Fig. 8(b), four PWM signals are used for V_{gs1},V_{gsa}, V_{gs2},V_{gs3}, and V_{gs4}. All of the N-channel MOSFETs in Fig. 8(a) are FDN327N. For simpler gate drive circuitry a N-channel series inductance (ESL). The MOSFET driver circuit used is PIC18F4331 micro controller.

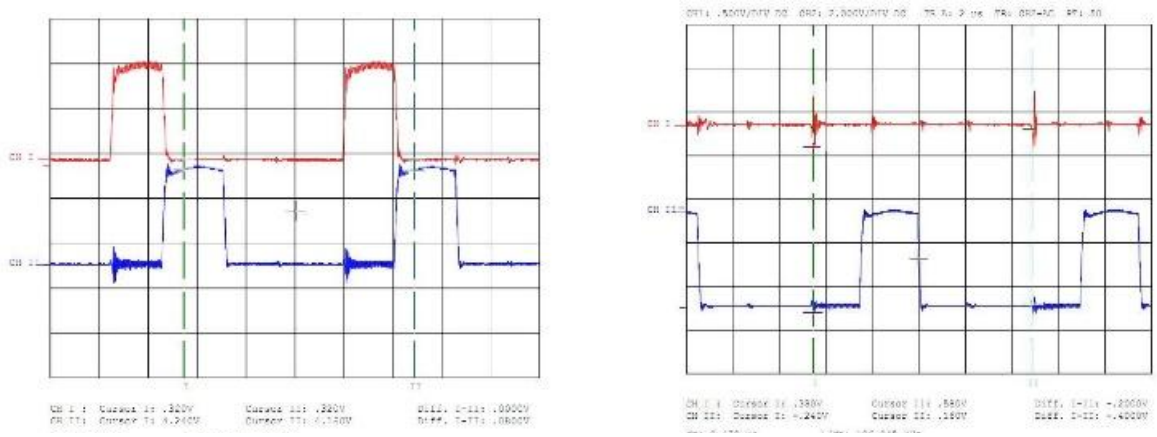
The experimental waveforms for the conventional and ID method converters are shown in Figs. 9(a) and (b), respectively. Note that Phase D of the ID method is not shown in Fig. 9(b), due to channel limitations of the oscilloscope. The effect of the ID approach is apparent: the output voltage ripple is reduced from 31.3 mV with the conventional method to 9.4 mV with the proposed ID approach. Employing a 7.2- resistive load, the measured efficiency of the conventional and ID approaches are 80% and 87%, respectively. The improvement in efficiency of the ID approach is mainly due to the shortened discharging period of the pump capacitors (only one third of the conventional approach), which means less MOSFET conduction loss and trace resistive loss. The experimental results

also showed that the parasitic inductances in the circuit can lead to spikes during the switching instants. Increasing the rising and fall time of the PWM signals can help reduce the spikes, but this also decreases the converter efficiency.In [15], a monolithic IC circuit similar to Fig. 8(a) was implemented, using the AMI0.5 m CMOS process through MOSIS. The die photo of the fabricated circuit is shown in Fig. 13. The total die size is 7.5 mm. Fig. 14 compares the output MOSFET can be used, but the converter efficiency may be lowered due to the larger on-resistance. Multilayer ceramic capacitors (MLCC) are used due to their small size, light weight, and low ESR and equivalent. Ripple in the conventional and ID based SC converters under different load currents. For the ID approach, an investigation was conducted to determine if discharging the pump capacitors one by one would sacrifice the transient response performance of the converter. A proportional–integral (PI) network was used to compensate the error amplifier. The transient responses when step changes are applied to the reference voltage V_{ref}. When V_{ref} changes from 1.1 V to 0.9 V, both the conventional and ID approaches have an overshoot of only 6 mV and a 1% settling time of 16μs. Thus the transient response performance of the converter is not sacrificed.



(a) (b)

Fig 8. Photos of hardware for (a) proposed circuit (b) PWM signal generation circuit



(a) (b)

Fig 9. Snaps of results from CRO (a) across circuit capacitors C_1 and C_2 (b)) across circuit capacitors C_1 and load capacitor C_L.

Conclusion

In this paper, an ID approach was proposed to reduce the output ripple in switched-capacitor-based step-down dc–dc converters. The proposed ID approach takes full advantage of the structure of step-down SC dc–dc converters. The steady-state performance of the proposed step-down SC dc–dc converter was analyzed, using the charge conservation method. Simulation and experimental results of a four-stage SC dc–dc converter show that the ID approach can reduce the output ripple by a factor of three. The proposed ID approach also improves the converter efficiency by 7%. A single-chip ID-based SC dc–dc converter was also successfully implemented. Further investigation opportunities exist for high current applications [16].

The proposed ID approach not only provides the possibility to reduce the output ripple, but also provides some flexibility in optimizing the design of step-down SC dc–dc converters. For example, if higher output ripple is tolerable, with the ID approach, the capacitance value of the output filter can be reduced for lower cost and higher power density. In addition, the switching frequency can be reduced for higher efficiency due to reduced switching losses.

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