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RESEARCH ARTICLE

FPGA IMPLEMENTATION OF DIRECT SEQUENCE SPREAD SPECTRUM TRANSMITTER WITH PSEUDO CHAOTIC GENERATOR.

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Abstract

Chaos based pseudo noise sequences for spread spectrum communications ranks amongst the most promising applications of chaos to communication. In arriving at these new sequences the theory of chaos has been used. The correlation properties of these chaotic sequences are analogous to white noise. In this paper we describe FPGA implementation of a spread spectrum transmitter using pseudo-chaotic sequences (PCS) for spreading the input digital data. The lengths of chaotic sequences are not restricted like LFSR sequences. The generated pseudo-chaotic sequences are investigated for autocorrelation, cross- correlation and balance properties.

Introduction:-

In order to spread the bandwidth of the transmitting signals, binary pseudo noise (PN) sequence has been used in spread spectrum communication system [4]. The autocorrelation and cross correlation functions of the spreading sequences are of most great importance in spread spectrum system. This paper suggests a completely different type of spreading sequence for use in direct sequence spread spectrum system. These sequences are generated using discrete chaotic maps. The sequences so generated, even though completely deterministic have characteristics similar to random noise. Furthermore length of sequences is for all practical purposes unlimited.

In a truly random sequence the bit pattern never repeats. A pseudo random binary sequence is semi random sequence the significance is that it appears random within the sequence length, satisfying the needs of randomness but the entire sequence repeats uncertainly. To a careless observer, the sequence appears totally random, however a user who is aware of the way the sequence is generated then he should know all properties of sequences. The figure.1 gives the overview of PN sequences.

The PN sequences have several interesting properties, which are exploited in variety of applications [3]. Because of their good autocorrelation two similar PN sequences can easily be phase synchronized, even when one of them is corrupted by noise.

Balance Property:-
In each period of maximum length sequence, the number of 1's is always one more than the number of 0's.

Run property:-
Among the runs of 1's and 0's in each period of sequence one half the runs of each kind are of length, one fourth are of length two, one eight are of length three and so on as long as these fractions represented meaningful number of runs [5].

Correlation property:-
Correlation is a measure of similarities between two sequences. When the two sequence compared are different it is the cross correlation and when they are same it is the autocorrelation.

$$R(m)_{xv} = \sum_{k=0}^{L-1} \quad x(k)y(k+m)$$

Where, R (m) = total number of `1`s / total number of bits.
The highlight of this paper is the PCS generator which generates a pseudo-chaotic PN sequence with good cross-correlation and auto correlation properties is well suited for direct sequence spread spectrum system [6]. Because of long periodicity it provides high security and is capable of handling more users.

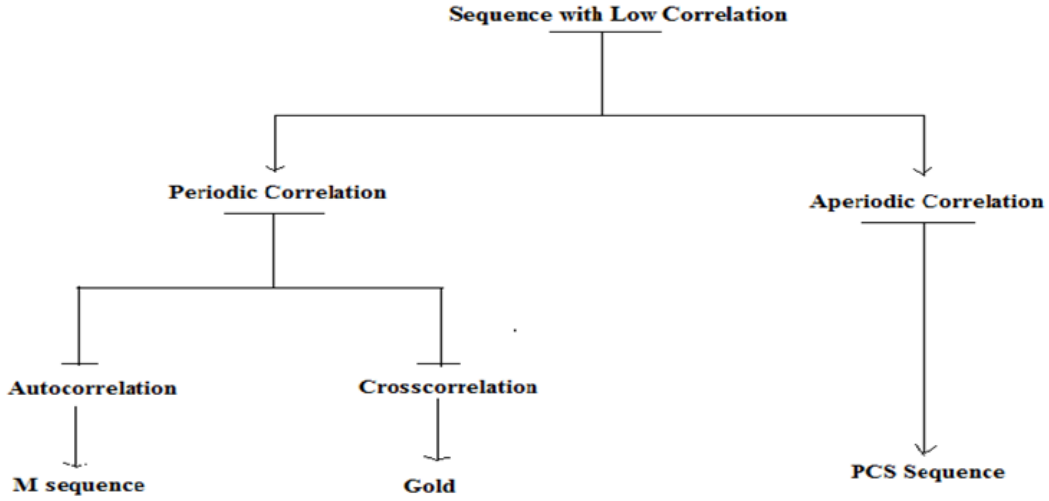


Fig.1. Overview of PN sequences.

Generation of PN Sequences:-

Generation of m-sequence (LFSR):-
Following figure.2 shows the basic block diagram of LFSR based on shift registers. The feedback from different shift registers which influence the input is called taps [2].This feedback arrangement can be expressed in finite field arithmetic polynomial mod 2. The period of sequence is $2^n - 1$ where n is number of shift registers.

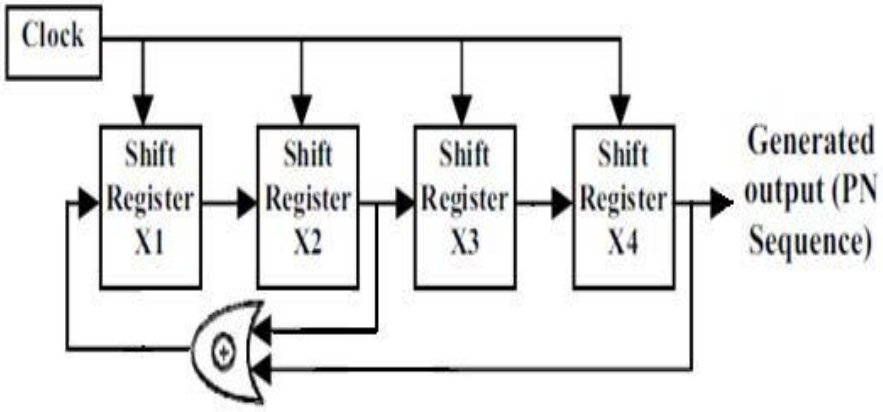


Fig.2. Block diagram of LFSR.

The 8 bit LFSR with maximum length feedback polynomial $X^8 + X^6 + X^5 + X^4 + 1$ that generates $2^8 - 1 = 255$ random outputs.
Figure.3 shows circuit of 8bit LFSR with maximum length feedback polynomial. The simulation waveform of this is

shown in figure.8.

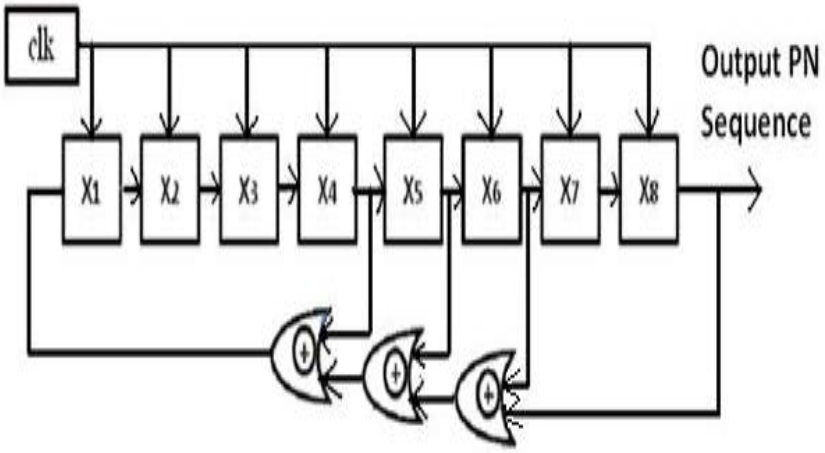


Fig.3. Eight bit LFSR Circuit.

The flowchart of M sequence (LFSR) generation is gives in figure.4.

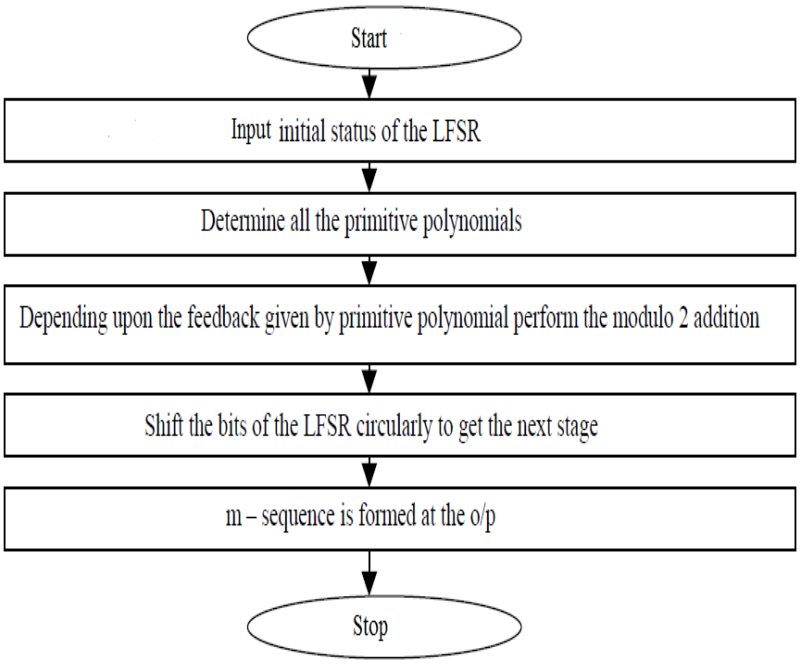


Fig 4: Flowchart of M sequence generator.

Generation of PCS sequence (NLFSR):-

The highlight of this paper is to generate PCS sequence with good cross correlation and auto-correlation properties that is well suited for DS-SS system.

It consists of a cascade of four basic cells with two eight bit programmable register each. The output of last cell i.e. each bit of last cell output are XORed together to obtain PCS and also this bit is feedback to the system to maintain nonlinearity. By increasing cells and size of register we can increase the number of users and period of sequence. Since the number of implementation possibilities are very high due to initial condition programmability [1].

The figure.5 gives the details of the generation of PCS sequence with four cells are connected in series.

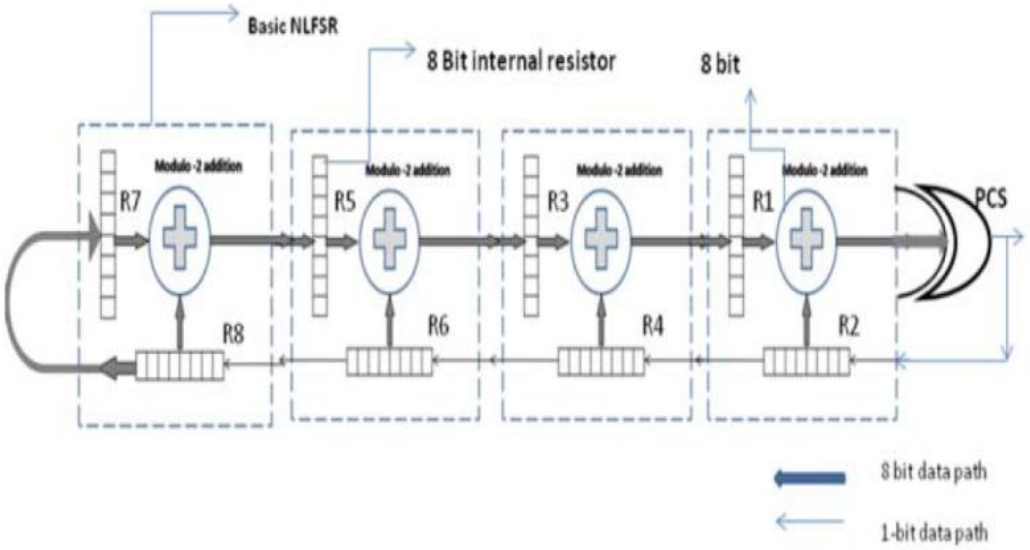
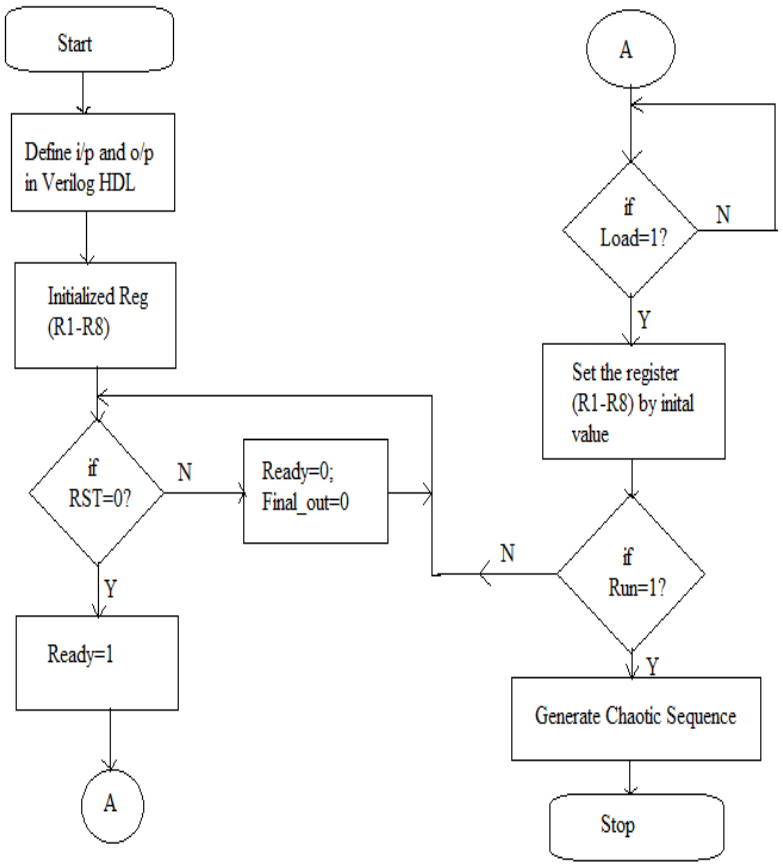


Fig.5. Pseudo chaotic sequence generator.

The flowchart of PCS generation is shows in figure.6. Verilog HDL programming language is used for the PCS generation. The simulation waveform of PCS is shown in Figure 9.

Fig.6. Flowchart of PCS generator.



FPGA Implementation of DS-SS Transmitter with PCS Generator:-

In this paper we replaced the conventional M-sequence (LFSR) with PCS (NLFSR) for DS-SS transmitter system. The block diagram of the implemented DS-SS system with transmitter is shown in figure.7

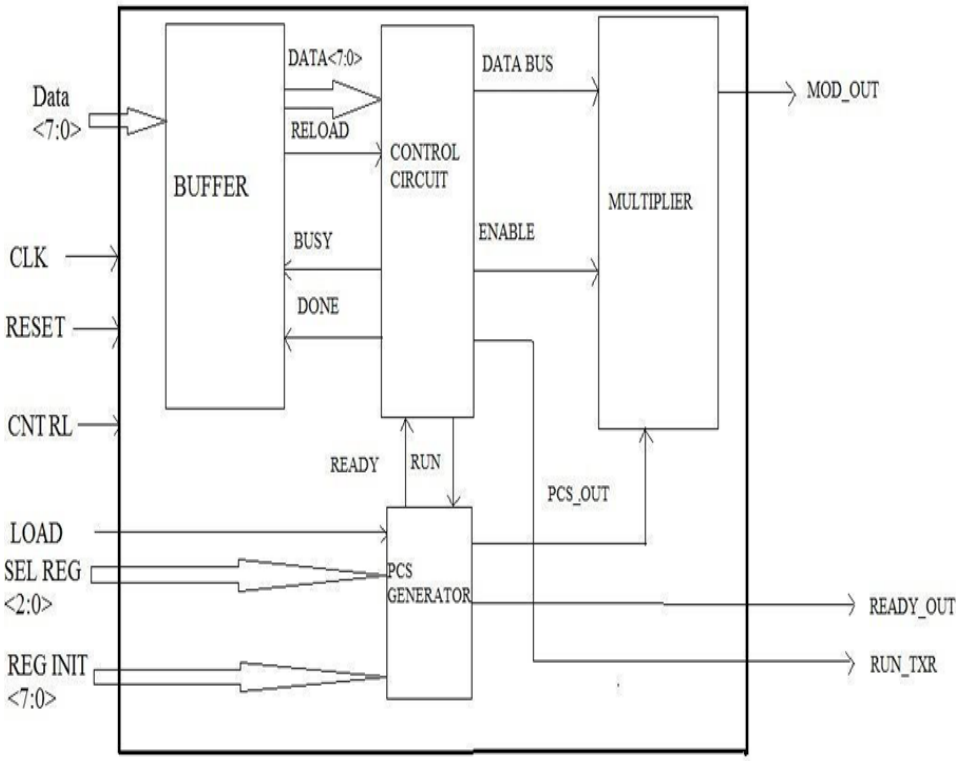


Fig.7. Block Diagram of DSSS transmitter.

In this we spread the data bits using PCS sequence which are generated using PCS generator as mentioned in section 2. To generate PCS we need to follow below process [1].

1. We need to initialized the 8 bit registers of PCS, to load this registers set load=1and to select particular register use sel reg pin.
2. After initialization the ready=1, which gives indication to control circuit that it can start its operation. As soon as ready=1, the busy=0.
3. In that condition message source sends a signal in the form of reload to control circuit to indicate that it is ready to send data. It sends data parallel and stored temporary in buffer of control circuit.
4. After receiving 8 bit data, control circuit enables the PCS by setting run=1 and also enables multiplier by setting enable=1 and send busy=1 to buffer.
5. The PCS generator starts generating 32 bits of PCS sequence. The control circuit then transfer one bit at a time serially to multiplier where it multiplied by 32 bits of generated PCS sequence resulting in a 32 bit of Spread sequence and the same is transmitted. This process is repeats 8 times; hence the PCS generator generates a total of 256 bits to spread all 8 bit data.
6. After transmitting all the 256 bits i.e. 8-bits of data, the control circuits makes signal done=1 and busy=0.

Simulation results:-

a. The output of 8 bit LFSR is shown in figure.8, by using 8 bits we get 255 random outputs.

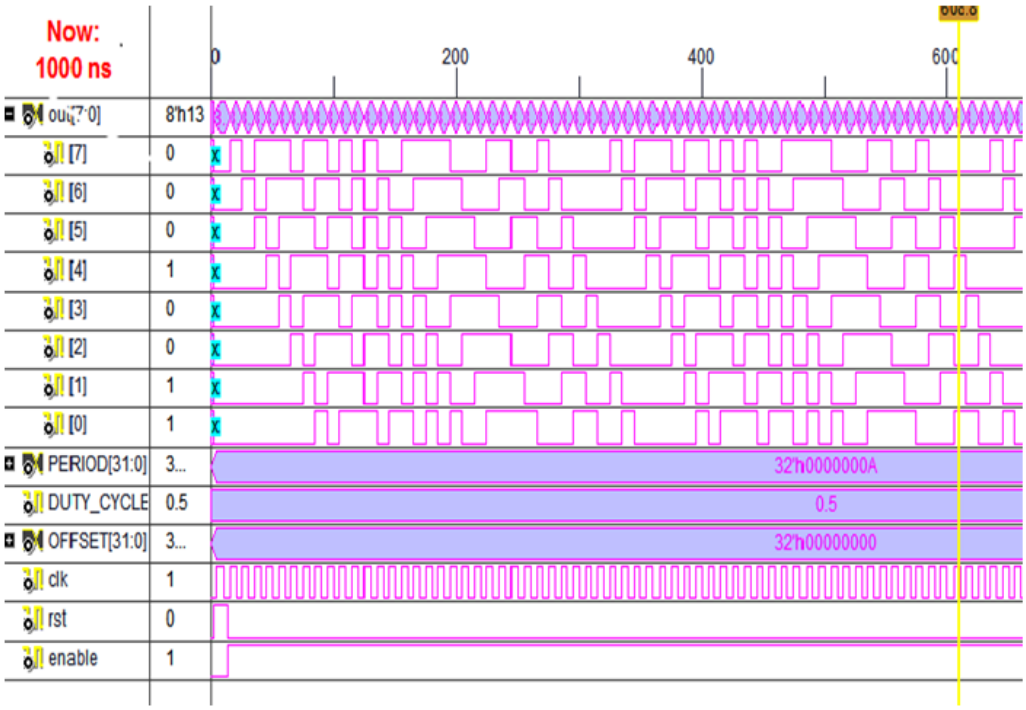


Fig.8. Simulated waveform of 8-bit LFSR

b. The output of PCS (NLFSR) is shown in figure.9. The simulated waveform shows that when load=1 and run=1 it gives 32 bit PCS output. The ready pin set high when output is generated otherwise it will be low.

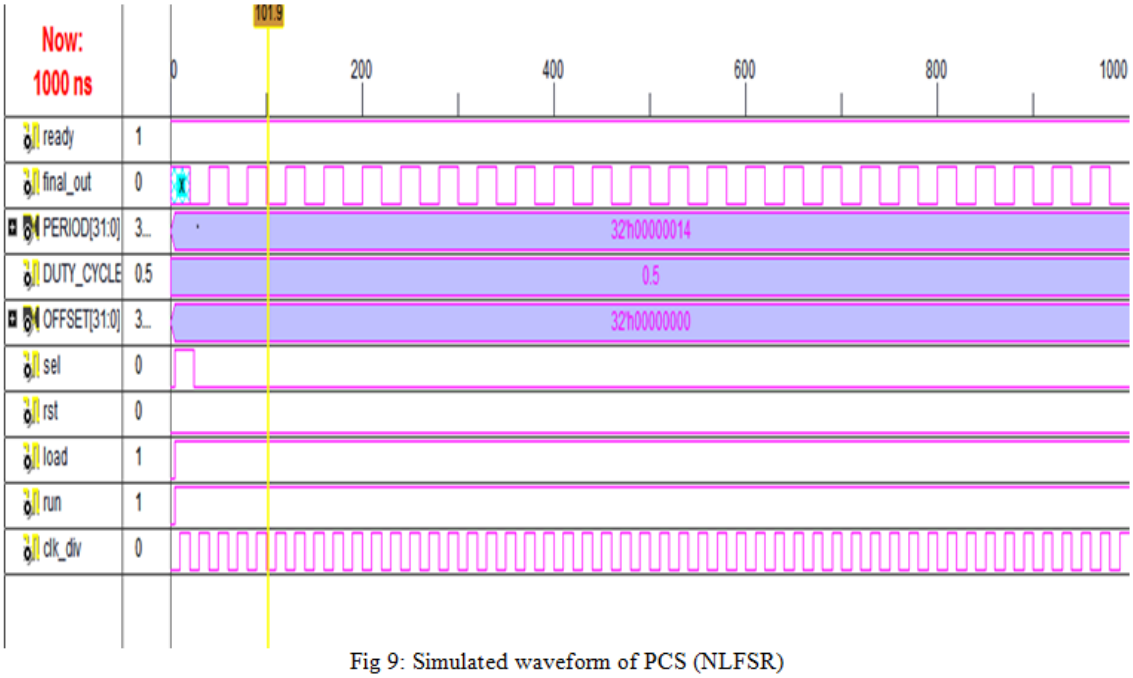


Fig 9: Simulated waveform of PCS (NLFSR)

c. The timing simulation is gives in table1. This gives the status of registers, flip-flops and LUT used, also gives the timing analysis of m sequence and PCS sequence.

Sr No.	Performance	8-bit LFSR	PCS (NLFSR)
1	Shift registers	8	11
2	XORs	1	5
3	Flip flops	8	3
4	LUT	1	2
5	GCLK	1	1
6	Delay	4 η sec	2 η sec

Table.1. Timing Simulation of M and PCS Sequences

Conclusions:-

A method of generating chaotic sequences suitable for use in a DS/SS system was described. The purpose of the use of chaotic sequences is to take advantage of their noise like features. They possess low auto and cross-correlations with spectral density similar to wideband noise.

Moreover, they out-perform PN systems in low probability of intercept Therefore, the task of interception and detection for an adversary becomes much harder when chaotic sequences are used instead of binary PN sequences in DS-SS systems.

The ease of generation of chaotic sequences is astonishing compared to the complexity of their random-like appearance.

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