ISSN NO. 2320-5407

Journal homepage: http://www.journalijar.com

INTERNATIONAL JOURNAL OF ADVANCED RESEARCH

RESEARCH ARTICLE

Noise Tolerable Dynamic CMOS Circuit With Current Mirror Keeper Transistor.

Rupa Behre[1], Rahul Mishra[2].

1. Student, Department of ECE, Lakshmi Narain College Of Technology, Bhopal,India.
2. Assistant professor,Department of EIE, Lakshmi Narain College Of Technology, Bhopal , India.

Manuscript Info

Manuscript History:

Received: 17 January 2016
Final Accepted: 29 February 2016
Published Online: March 2016

Key words: Dynamic CMOS logic, Keeper transistor, Domino logic, and current mirror circuit

Corresponding Author

Rupa Behre.

Abstract

Dynamic CMOS circuits are less immune to noise as compare to static CMOS circuits in digital VLSI design. The use of dynamic CMOS circuits reduces the number of transistors, which in turn reduces the number of interconnects, cross talk between interconnect and power dissipation. So noise is the major concern of dynamic CMOS design. The noise susceptible design through simulation and analysis shows that noise resistance of dynamic CMOS logic circuits can be improved as compare to static CMOS logic circuits with the same performance of dynamic circuits the inhibitor's concentration and decreased with rise of temperature.

Introduction:-

Dynamic CMOS circuits is mostly use because of less number of transistors require to implement any logic function. But dynamic CMOS is less susceptible to noise. For the noise due to leakage current suppress in CMOS logic circuits, the variable and multi threshold CMOS circuits are use. The noise is generated due to voltage fluctuation at power and ground rail (also called as power and ground bouncing noise) during the active and sleep mode transition is of major concern. This noise propagates to the neighboring circuits through shared supply rails and internal nodes of circuits. Keeper transistor design using current mirror, stack transistor technique is presented in this paper for internal node charge sharing noise and sleep transistor technique is use to suppress power/ ground bouncing noise. The switching delay time, power consumption and CMOS layout area are characterized under an equal noise constraint. The effect of process variations on the noise, switching time, and power consumption of dynamic CMOS circuits is also evaluated.

Noise in Dynamic CMOS Circuit:-

Low area and high speed is the major achievement of high performance computing application of dynamic CMOS circuit design. The speed of dynamic CMOS circuit is increase due to lower capacitance and low contention during switching as compare to static CMOS circuit using only NMOS transistor. Dynamic circuit operates in precharge and evaluation phase. In precharge phase, the output dynamic node is precharge to supply logic and at evaluation phase the output dynamic node is evaluated. Depends on the inputs bits, the output dynamic node will either stay at logic high or discharge to logic-low.

The noise in CMOS circuit is the deviation in supply voltage is the major problem to concern. Impact of noise on system performance is less but the power dissipation in noise tolerable circuits as the power dissipation dominates the overall power consumption in design systems. Dynamic CMOS circuit is the best choice for high performance design due to there advantage of parametric optimization. The charge sharing between the internal nodes of dynamic logic during evaluation phase creates the voltage deviation at internal nodes which cause the noise. This noise can not be recovered and leads to false output transitions [2].

In this dynamic CMOS circuit design, several nodes are essential to seize their binary bits as a charge stored on a capacitor. These nodes are not coupled to their 'drivers' permanently. The 'driver' places the logic value on them, and is then disconnected from the node. Due to leakage etc., the logic value cannot be held indefinitely. Dynamic circuits therefore require a minimum clock frequency to operate correctly. Use of dynamic circuits can reduce circuit complexity and power consumption substantially. When the clock is low, pMOS is on and the bottom nMOS is off. The output is 'pre-charged' to 1 unconditionally [2].

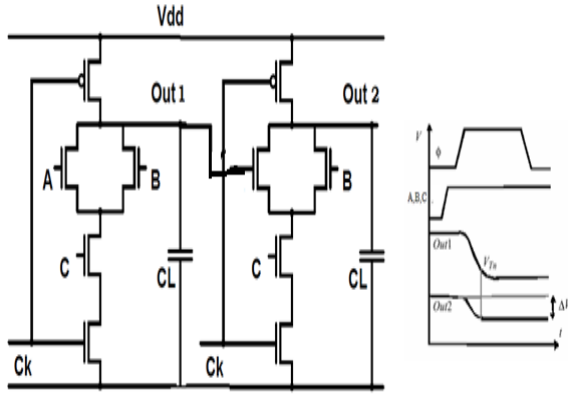

Fig 3.1 CMOS dynamic gate logic

When the clock goes high, the pMOS turns off and the bottom nMOS comes on. The circuit then conditionally discharges the output node, if (A+B).C complement is TRUE. This implements the function (A + B).C.

Precharge:-
When clk=0, the output node "OUT" is precharged to VDD by the PMOS transistor. The precharge phase is occur when clk=0. The path to the VSS supply is closed via the NMOS during clk=1 (evaluate phase). The pull up time is improved by PMOSFET, but the pull down time is increased due to the ground switch (NMOS).

Evaluation:-
When clk=1, the precharge pull up transistor is off, and the evaluation transistor is turned on. Depending on the values of the inputs and the composition of the PDN, a conditional path between OUT and (through the nMOS transistors) GND is created. If such a path exits, OUT is discharged and a low output signal is obtained. If not, the precharge value remains stored on the output capacitor CL, (CL, is a combination of the diffusion capacitors, the wiring capacitance and the input capacitance of the fan-out gates) and a high output value is obtained during the evaluation phase. The only possible path between the output node and a supply rail is to GND, consequently, once "OUT" is discharged, it cannot be charged again. This is in contrast with the static circuit, where the output node is low-impedance under all possible circumstances.

Noise Susceptibility with keeper current mirror transistor:-
The noise generated due to charge sharing in internal nodes is suppressed through the additional NMOS transistor acts as keeper transistor. By using keeper transistors the source voltage is raised to enhance the noise tolerance. A current mirror circuit is also use in place of keeper NMOS transistor. The gate of this transistor is connected to the source and the leakage current is mirrored to the dynamic node through the PMOS current mirror transistors. Even though this method shows excellent tracking of switching delay, the contention is still exist because the keeper is strongly ON during the beginning of the evaluation phase.

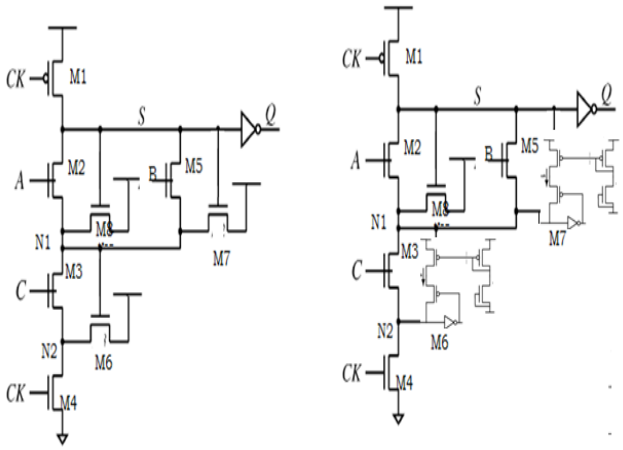

Fig 1 Internal Node Charge Sharing noise susceptible circuit with keeper transistors.

To increase the noise tolerance of dynamic CMOS logic gates is to employ a weak transistor, known as keeper, at the dynamic node as shown in Fig. . The keeper transistor supplies a small amount of current from the power-supply network to the dynamic node of a gate so that the charge stored in the dynamic node is maintained. In the original domino dynamic logic work, the gate of the PMOS keeper is tied to the ground, Therefore, the keeper is always on [6]. Feedback keepers, became more widely used because they eliminate the potential DC power consumption problem using the always-on keeper in the evaluation phase of domino gates [6].

The keeper transistor prevent the internal node from floating by using weak complementary transistor network to improve the noise tolerance on the cost of increase in small amount of area and number of transistors. Fig 1 shows Internal Node Charge Sharing noise susceptible circuit with keeper transistors design using current mirror circuit. This technique reduces routing complexity, increase dynamic node capacitance, and low contention current. It is improve the trade off of speed, power and area in order to achieve noise susceptibility.

Performance Measurement of Timing and Noise Tolerance:-

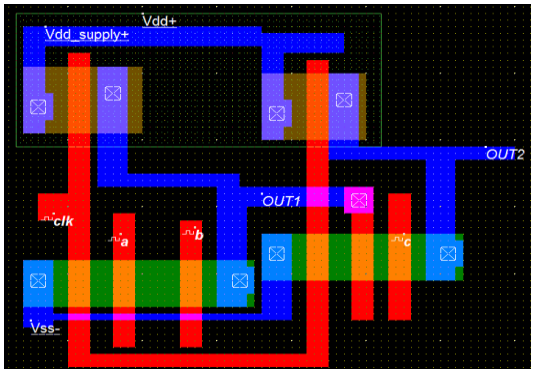

Fig CMOS layout design for cascaded dynamic CMOS Circuit

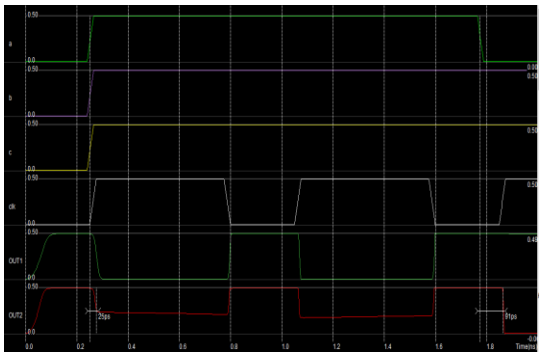

Fig Charge sharing Noise Timing simulation of cascaded dynamic CMOS Circuit.

In dynamic logic structure the inputs can just change at the precharge phase and must be stable at the evaluate phase of the cycle. If this condition is not meet, charge redistribution effects can corrupt the output node voltage. At the end of the evaluation phase output will be erroneous. There are some other limitations associated with domino CMOS logic gates. The additional capacitance at each node of the series connected MOS logic makes speed slow and may cause charge redistribution which results in noisy output.

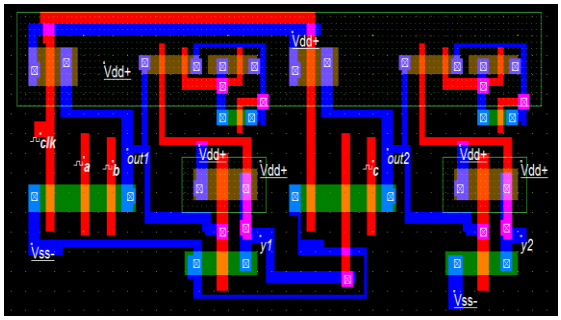

Fig CMOS layout design for cascaded dynamic CMOS Circuit with Current Mirror Keeper Transistor.

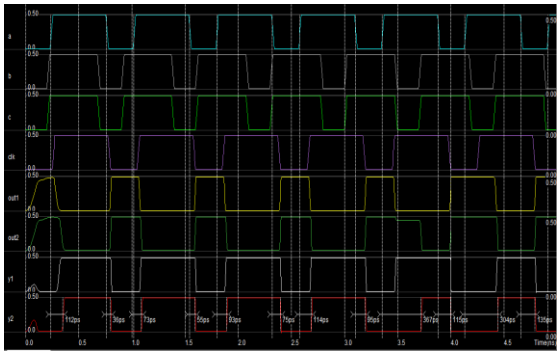

Fig Timing Simulation of cascaded dynamic CMOS Circuit with Current Mirror Keeper Transistor.

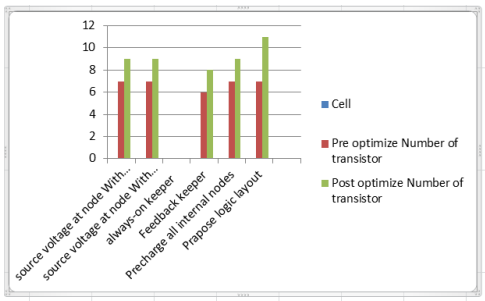

Fig Comparative analysis for number of transistor.

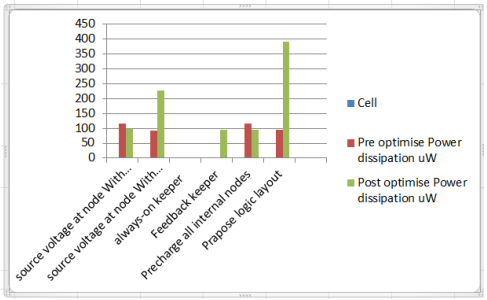

Fig Comparative analysis for Power dissipation across the circuit.

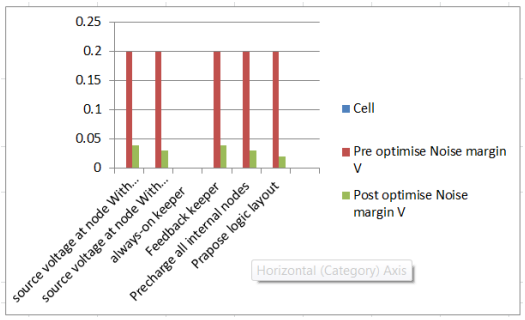

Fig Comparative analysis for Noise margin analysis.

In complex dynamic logic gates with large pull-down network, charge sharing between the dynamic node and the internal nodes in the pull-down network often results in false gate switching. A simple yet effective way to prevent the charge sharing problem is to precharge the internal nodes in the pull-down network along with precharging the dynamic node.

Conclusion:-

In this paper static verses dynamic circuits and Sources of Noise in dynamic Digital Integrated Circuits are discuss. Dynamic logic circuit has less immunity for noise. The noise arises due to charge sharing at internal nodes can be reduce by connecting MOSFET base keeper transistor at internal node. This improves noise tolerance against both internal and external noises are to increase the source voltage of the transistors in the pull-down network. Also the noise tolerance of dynamic CMOS circuit is increase but incorporating the feedback keeper circuits.

References:-

1. Hailong Jiao, Student Member, and Volkan Kursun publish their paper onm title "Reactivation Noise Suppression With Sleep Signal Slew Rate Modulation in MTCMOS Circuits" in IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 21, No. 3, March 2013.

2. Kumar Yelamarthi, Member and Chien-In Henry Chen "Timing Optimization and Noise Tolerance for Dynamic CMOS Susceptible to Process Variations" IEEE Transactions On Semiconductor Manufacturing, Vol. 25, No. 2, May 2012 pp no. 255.
3. Li Ding, Member and Pinaki Mazumder "On Circuit Techniques to Improve Noise Immunity of CMOS Dynamic Logic" IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 12, No. 9, September 2004 pp no. 210-925.
4. Chien-In Henry Chen "Timing Optimization and Noise Tolerance for Dynamic CMOS Susceptible to Process Variations" IEEE Transactions On Semiconductor Manufacturing, Vol. 25, No. 2, May 2012.
5. Domagoj Siprak, Marc Tiebout, Nicola Zanolla, Peter Baumgartner, and Claudio Fiegna "Noise Reduction in CMOS Circuits Through Switched Gate and Forward Substrate Bias" IEEE Journal Of Solid-State Circuits, Vol. 44, No. 7, July 2009 pp no. 1959-1967.
6. Manisha Pattanaik, Muddala V. D. L. Varaprasad and Fazal Rahim Khan " Ground Bounce Noise Reduction of Low leakage 1-bit Nano-CMOS based Full Adder Cells for Mobile Applications" International conference on electronics devices ICEDSA year 2010.
7. UMC 80 Nanometer CMOS Technology [Online]. Available: http://www.umc.com/english/process/g.asp
8. Umesh Dutta, Pankaj Kumar, Naresh Kumar "Noise Tolerance Enhancement with Leakage Current Reduction in Dynamic Logic Circiuts" International Journal of Scientific Engineering and Technology (ISSN : 2277-1581), Volume No.1, Issue No.3, pg : 137-142