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RESEARCH ARTICLE

USING PERCOLATIVE CRYSTALLINE 0.3 CUO/PVDF NANOCOMPOSITE GATE DIELECTRIC FOR FABRICATING HIGH-EFFECT MOBILITY THIN FILM TRANSISTOR OPERATING AT LOW VOLTAGE

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Abstract

Thin-film transistor (TFT) with various layers of crystalline Poly-vinylidene fluoride (PVDF)/CuO percolative nanocomposites based on Anthracene as a gate dielectric insulator have been fabricated. A device with excellent electrical characteristics at low operating voltages (<1V) has been designed. Different layers (L) of the film were also prepared to achieve the best optimization of ideal gate insulator with various static dielectric constants (ε_r). Capacitance density, leakage current at 1V gate voltage and electrical characteristics of OFETs with a single and multi layer films have been investigated. This device was showed highest field effect mobility of 2.27 cm^2/Vs, a threshold voltage of -1.6V, an exceptionally low sub threshold slope of 380 mV/decade and an on/off ratio of 10^6. Such a High-ε three layered (3L) PVDF/CuO gate dielectric appears to be highly promising candidates for organic non-volatile memory, sensor and field-effect transistors (FETs).

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Introduction:-

Flexible Organic Field Effect Transistors (OFETs) exhibiting higher electrical performance, good compatibility with electronic applications such as non-volatile memory and radio frequency identification, sensors[1-5] is of immense importance now-a-days. The conventional dielectric insulators such as silicon and silicon dioxide had already attained the bearable limits in device miniaturizations, although they possessed very low dielectric constant (k=3.9). Suitable gate dielectric material with high dielectric constant is necessary to enable the required drive currents for sub-micrometer scale devices. In pursuit of such flexible dielectric material, searching for different organic polymers blended with inorganic oxides in various concentrations and layers might be interesting thrust. Reducing the thickness of SiO_2 (~2nm) layer, the leakage current would dominate and eventually the device has the detrimental effect. Again typically, $d/L \leq 0.1$ is necessary to ensure that the field created by gate to source voltage (V_G) and not the lateral field, drain to source voltage(V_D), determines the charge distribution within the channel. Few layers of organic polymer nanocomposites with high k is relatively cost effective entail a low temperature processability, less complicated fabrication technique enabling high electrical device functionality. To understand the OFET device operation,[5-8] it is essential to develop polymer based nanocomposite gate dielectrics[9-11] as the choice of gate dielectric.

The major advantages of utilizing this as gate dielectrics due to smooth unhindered surfaces and triggering surface tension effect to pick up the crystallinity, ordering in molecular level of the organic semiconductor layer that were

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developed on surface of the gate dielectric. Low voltage operation is possible by reducing the threshold voltage and sub-threshold slope (*SS*)

$$SS = \frac{dV_G}{d(\log I_{DS})}$$

which are mainly dominated by the properties of gate dielectric moderately than organic semiconductors.[12-15] So, for low operating voltage, a high capacitance is required to induce a high density of free carriers at the channel. The field induced current is proportional to the free carrier density induced at the channel-dielectric interface and mobility (μ) of the organic semiconductor.[16-17] Hence, to overcome high operating voltage requirement either high capacitance gate dielectric can be used or, thickness of the gate dielectric layer should be reduced. Several research groups have fabricated OFETs by using polymers and polymer composites.[12-15] Organic semiconductors have been widely studied from the view point of their fundamental optoelectronic properties and their potential applications such as organic light emitting diode (OLED), organic field effect transistors (OFETs), photovoltaic cells.[18-20] The OFETs with anthracene as organic semiconductor exhibits efficient carrier charge transportation to be used as potential material.[21-24] In this paper, a low voltage operable OFET with high-k PVDF-CuO nanocomposite[10] gate dielectric layer and benzanthracene as organic semiconductor have been fabricated for temperature sensing applications.[25-27] A very simple fabrication process has been used along with step wise poling process for enhancing the pyroelctric effects on the device performance due to choosing PVDF as polymer.[10] The output characteristic of OFET after poling were changed and exhibited linear current-voltage relationship showing the evidence of large polarization. The temperature dependent response of the device was also investigated. The stable performance [26] of the OFET after poling operation makes it reliable in temperature sensor applications.

Experimental Section

CuO nanoparticles were prepared by the sol-gel method by reacting at room temperature acquous solutions of copper nitrate and sodium hydroxide at pH=10. The resulting gel was washed several times with distilled water until free of nitrate ions. This gel was then centrifuged and dried in air. The PVDF powder was purchased from Aldrich (99.9%) and N, N-Dimethyleformamide (DMF) from Merch (99.5%). A desired amount of CuO nanoparticles were completely dispersed in 80mL DMF in an ultrasonic bath for 10hours.10 The calculated quantity of PVDF (such that the amount of CuO in the composite is 10wt% of PVDF)10 were added into the above suspension and stirred well for 7 hours to dissolve the PVDF completely. ITO (Indium Tin Oxide) coated glass was used as substrate where ITO layer was used as gate electrode (G). Now for the formation of the gate dielectric layer cleaned ITO coated glass was dipped into the solution of PVDF-CuO composite in an angle 35° for 15min. It was then lift-off the solution slowly. The sample was dried at 60ºC for 2hr to remove adhered DMF completely. Next, the sample with gate dielectric layer was annealed on a hot plate at 150ºC so that the PVDF-CuO composite layer melted completely and then it was maintained at this temperature for 3 hr. Subsequently it was cooled naturally to room temperature in nitrogen atmosphere. We used Anthracene (Aldrich, 98%pure) as organic semiconductor and toluene (Merck, 99.5% pure) as solvent. Required amount of Anthracene powder was added with toluene and stirred in a water bath for 72 hours. The solution was then remained still for at least 5hr. Subsequently, the organic semiconductor layer was deposited on gate dielectric layer by dip coating process and dried at room temperature. Source (S) and drain (D) electrodes were deposited by a gold coater unit. The transistor characteristics of the anthracene-OTFT were investigate by using a KEITHLEY Model 4200-SCS semiconductor characterization system in a dark box at room temperature. Au source/drain top electrodes onto this film were deposited by a thermal evaporation method using a tungsten basket. These electrodes with ~ 100 nm thickness were made through the shadow mask.

Results and Discussion:-

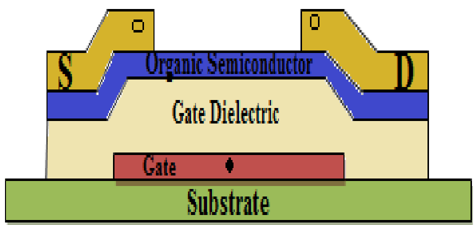

Fig. 1:- Schematic diagram of the as-prepared anthracene Organic thin-film transistor structure with PVDF/CuO nanocomposite as gate dielectric.

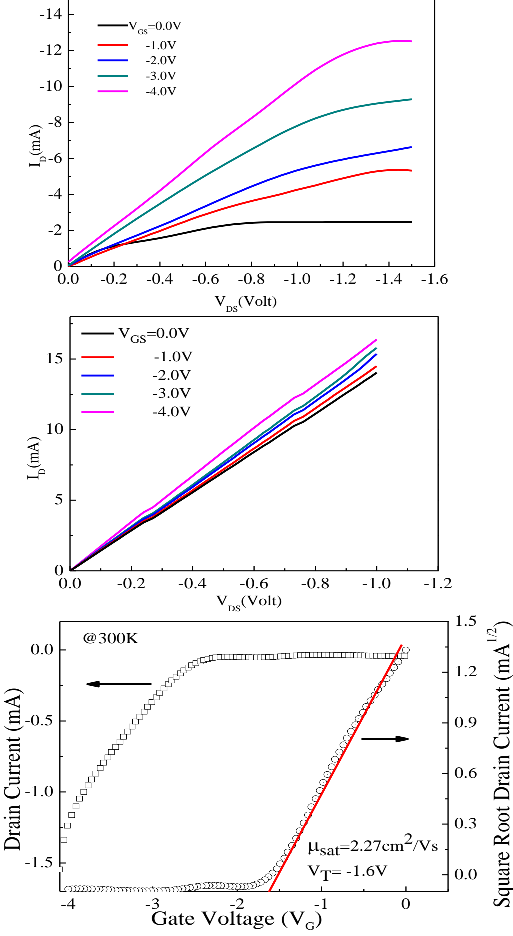

Fig. 2 (a) I_D vs. drain-source voltage, V_{DS} at different V_G (b) shows the transfer characteristic (c) I_D and Sq. root of I_D as a function of V_G

The schematic structure of the benzanthracene OTFT shown in Fig. 1 was developed based on chip poling process where the source (S) and drain (D) electrodes were grounded and gate electrode was connected to a negative bias. The organic semiconductor layer (Benzanthracene in the present case) and gate electrode (ITO) acted as poling electrode and a uniform poling electric field was produced across the gate dielectric (PVDF/CuO composite) layer. Charge transport takes place primarily within the first few layers of semiconductor molecules near the semiconductor/insulator interface and the device performance was dominated by the interfacial layers.

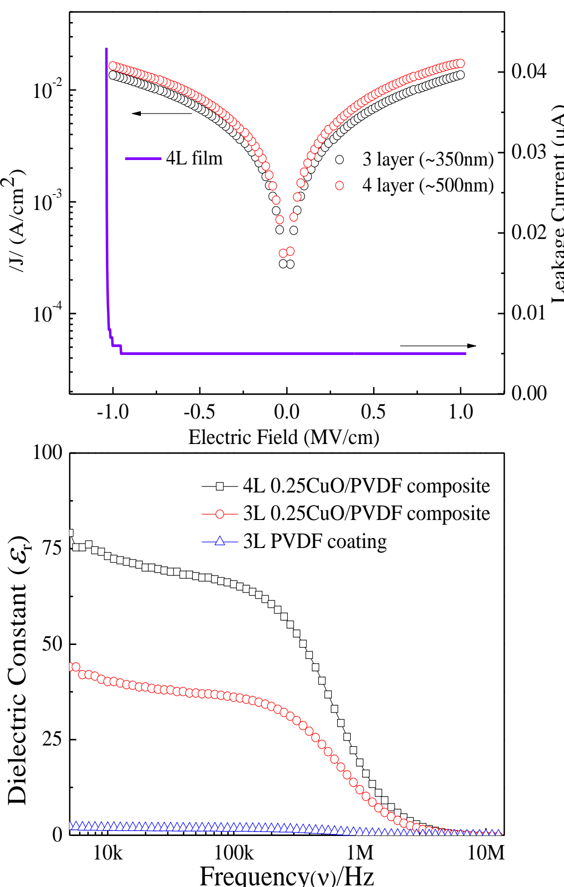

Figure 3 (a) current–density/leakage-current–electric-field measurements for the OTFTs. (b) Frequency response of layered devices at room temperature.

The output characteristics (drain current, I_D vs. drain-source voltage, V_{DS}) at different gate-source voltage, V_G , of the Organic Field Effect Transistor (OFET) before poling shown in Fig. 2(a) were similar to those of conventional ferroelectric field effect transistors (FeFETs).[26-27] As seen in Fig. 2, the drain current increases with drain voltage and reaches a saturation due to a pinch-off of the active channel of the transistor. The benzanthracene OFET works in a p-channel operational mode because the drain current increases with negative gate voltages. This indicates that benzanthracene as a p-type charge transport material. One of the interesting features of these devices is the saturation of drain current (I_D) at higher drain-source voltage (V_{DS}). Contrastingly, for the present device, the saturation occurs, for example, at a drain-source voltage (V_{DS}) of ~ -0.5V for a gate-source voltage (V_{GS}) of -0.2V. It is clearly seen that the operating voltage is much lower compared to those of similar other reported in the literature.[28] One of the reasons behind this feature might be for the use of PVDF/CuO composite[10] as gate dielectric whose capacitance is sufficiently large (C_i=32.18nF). The operating voltage of OFET depends critically on the nature of gate dielectric materials and their interfacial properties, because the surface of the gate dielectric material makes a contact with the channel through which drain current flows. Hence, a gate dielectric of higher capacitance induces higher charge injection into the organic semiconductor layer at a particular gate voltage, allowing a lower operating voltage. Figure 2(b) shows the transfer characteristic of the device from where one may calculate the transconductance[29] of about

17μS at V_{DS}= -0.5V close to the highest reported value for SWCNT-FETs [30] and testifies superior gate coupling and to a large carrier field-effect mobility. The device exhibits a threshold voltage between -0.05 and -0.5 V, depending on whether the threshold voltage is estimated from the plot of the square root of the drain current versus gate-source voltage or from the plot of the drain current versus drain-source voltage. PVDF/CuO is a p-type semiconductor and the device operates in the accumulation mode. However, since the turn-off voltage is small compared to the practical supply voltages, the full ON/OFF ratio between accumulation and depletion can be exploited in many circuit applications. Charge carrier mobilities, however, are still an order of magnitude lower than that for a-Si. From the transfer characteristics in the saturation regime, the mobility is extracted according to the following relation[31]

$$I_{SD} = \frac{W \times C_i}{2 \times L} \cdot \mu_{FE}^{sat} \cdot (V_G - V_T)^2 \qquad (1)$$

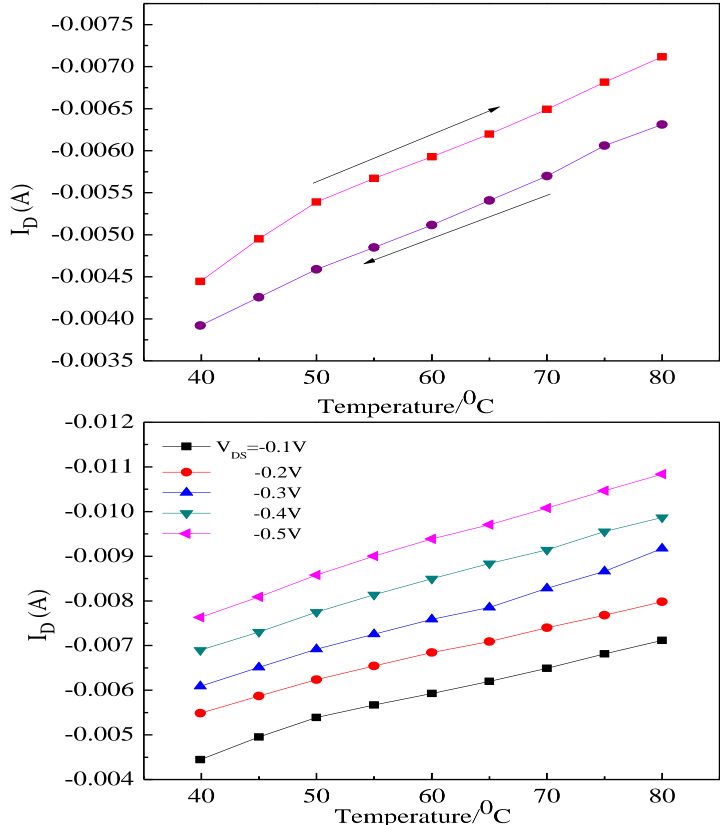

Figure 4 (a) Temperature response of the poled device data of proportional I_D were replotted. (b) I_D of the poled device in poling operation mode.

where μ is the field-effect mobility, C_i=32.18 nF/cm^2 is insulator (PVDF/CuO dielectric layer) capacitance, and W and L are the width and length of the channel, respectively, and V_T is the threshold voltage. The average field-effect mobility was 1.1±0.1 cm^2/V-s (measured at a gate-source voltage of −1 V, i.e., the drain saturation voltage), a threshold voltage of 0.34 V, a sub-threshold slope of 0.38V/decade and an on/off current ratio of 10^6 were obtained. The fabrication of an OTFT with a subthreshold slope within a factor of 6 of the theoretical limit is a significant leap forward.[31] This may be related to the ionic species in the polymer (PVDF in present case) dielectric film remaining from the dichromate cross-linking agent. The experimental characteristics are quadratic only in the range 0.05 V<$|V_g|$<0.25 V and exhibit poor current saturation at higher gate voltages. Within the quadratic range we obtained values of μ_{FE} = 0.02–0.05 cm^2/V.s under optimized deposition conditions. The threshold voltage is low, $|V_T|$< 0.05 V. The TFT characteristics in Fig. 1(a) reveal some non-ideal features. Near V_{DS}=0, the output characteristics is nonlinear, especially for higher gate voltages. Above V_G=-0.2 V, current saturation becomes poor and VSD has to

significantly exceed $|V_G-V_T|$ to drive the transistor into saturation. These non-idealities may at least partly be related to a non-ohmic source/drain contact. Figure 3(a) shows the leakage current and current density of 3L and 4L CuO/PVDF nanocomposites with applied electric field. Such a low value of leakage can be useful for OFET device application which may also be proven in the frequency dispersion of as prepared samples at ambient temperature. Many fold increase in the dielectric constant with respect to pristine PVDF in 3L and 4L proved the candidature of such samples as useful gate dielectric material used in OFETs. Various temperature profile of I_D have have also been plotted to ensure the stability of the OFET and appears to be nice upto 80^0C for different bias voltages. Although anthracene based OFETs exhibited high device performances at low voltages, critical drawbacks, such as ID hysteresis during gate swing, were found in the transfer curve of the device. The hysteresis present during device operation led to a shift in V_{th} when the device was switched from off to on, and back to off. This phenomenon prevents this OFET from being used as a driving unit device in display backplanes or logic circuitry in radio frequency identification (RFID) tags, in which Vth must be stable. In our device, hysteresis showed a specific clockwise loop directionality: on-to-off swept transfer curves shifted towards a higher V_G compared with that of off-to-on sweeps.

Conclusion:-

In conclusion, we have demonstrated the potential of using ultrathin layers of PVDF/CuO as insulator for organic semiconductors by preparing a high performance device with low voltage operation. We have pointed out that that pyroelectric PVDF based insulators can be used to obtain organic transistors with good electrical properties for a cheap and easy processing and that the performance of such devices is significantly improved by using an ultrathin gate insulator PVDF and their temperature sensitive behavior. The use of a built-in pyroelectric gate dielectric would reduce the complexity of the fabrication process. The device we fabricated was found to have a field effect mobility of 1.5 cm^2/Vs (close to the best mobilities reported for pentacene TFTs), and an on/off current ratio of 10^6. Integrating various smart organic dielectric materials directly into the OFET device structure would enable the production of a vast range of functional or smart organic electronic devices.

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