Journal Homepage: - www.journalijar.com

INTERNATIONAL JOURNAL OF ADVANCED RESEARCH (IJAR)

Article DOI: 10.21474/IJAR01/22220
DOI URL: http://dx.doi.org/10.21474/IJAR01/22220

RESEARCH ARTICLE

DESIGN AND ANALYSIS OF CONTENT ADDRESABLE MEMORY USING GNRFET FOR NEXT GENERATION AMPLIFIERS

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Manuscript Info

Manuscript History
Received: 04 September 2025
Final Accepted: 06 October 2025
Published: November 2025

Key words:-
Graphene nano ribbon field effect transistor, Content Addressable Memory,Carbon Nano tube field effect transistor, Power Delay Product(PDP)

Abstract

The ongoing limitations in scaling CMOS technology has forced efforts toward alternative nano electronic devices with a higher speed and lower power. We report on the design and analysis of a Content Addres sable Memory (CAM) employing Graphene Nanoribbon Field Effect T ransistors (GNRFETs) for next generation amplifier applications. Due to GNRFETs possessing high carrier mobility combined with a tunable bandgap and superior electrostatic control compared to traditional MOS FETs, they have a more advantageous switching speed while minimizin g leakage and improving scalability. The designed CAM architecture based on GNRFETs has been modelled and simulated to observe the delay, power dissipation, and search speed. Based on the simulation results, our GNRFET CAM demonstrated a greater degree of energy efficiency and operating frequency ultimately demonstrating the capabi lity of GNRFETs to improve performance limitations in traditional CAM circuits. GNRFET based memory architecture has potential as an ultra-low-power, high-speed computing and amplifier subsystems in future nanoelectronics and mixed-signal integrated circuits.

Introduction:-

The immense potential of carbon nanotubes(CNTs) as a replacement for Si in the channel of field-effect transistor(FET) devices has attracted substantial interest from the research community over the past few years. While electron and hole mobilities have been measured and predicted to be extraordinarily high, such that CNT-based transistors can be considered nearly ballistic, there is no easy method of patterning even the simplest of CNT-based circuits. At present, it appears that revolutionizing process technology for large-scale integration of CNT devices will be important.

A promising alternative to CNTs are graphene(carbon) nanoribbons (GNRs), which are essentially edged-terminated graphene sheets. The GNRs are expected to have similar electronic properties to CNTs, but they offer the possibility of lithographic patterning on SiC substrates, potentially solving the major obstacle to large-scale integration[1]. If we consider a CNR as a vector with the indices(n,m), similarly to CNTs[2][3]. We focus primarly on armchair GNRs that represent the same structure as zigzag CNTs described by the chiral vector (n,0), since they are expected

to be semiconducting. Unlike CNTs, for GNRs, the armchair/zigzag nomenclature refers the direction of the edge, not the chiral vector.

Graphene nanoribbons (GNRs), narrow strips of graphene, are created by unzipping carbon nanotubes (CNTs) [13]. Like their parent CNTs, GNRs have remarkable electronic and charge-transfer characteristics, while also having an ultra-high aspect ratio, frequent edge sides, and a more accessible surface area than CNTs [14]. These characteristics indicate that it should be a worthwhile conductive nanofiller. Moreover, under strictly controlled conditions during their unzipping, GNRs may contain only a few layers of ribbon to make their exfoliation in the host polymer easier than with GNPs [15]. While there are a lot of studies on CNTs and GNPs towards CPNs with improved properties, there is very little research on GNR/polymer nanocomposites [16,17,18].

The electron band structures of CNTs and GNRs are built using the tight-binding (TB) method with the pz orbital basis [2][3]. For CNTs, the full unit cell of the CNT/GNR is used to build the the TB Hamiltonian. Periodic boundary conditions are applied to the edge atoms of the CNT. For GNRs, the edge atoms have dangling bonds, so the full band structure of the ribbon is calculated, including the effect of dangling bonds. Both CNT and GNR are assumed to be infinite and periodic in the transport direction.

In terms of quality, the band structure of the GNR is similar to the CNT's, with the bandgap decreasing as GNR's width is increased. The degeneracy of the nanotube levels is then lifted, and the "new" levels are lowered in energy. Qualitatively, this can be understood by considering the boundary conditions that the electron states of CNTs and GNRs must satisfy. Since a CNT is a periodic structure even in the azimuthal direction, the electron states must themselves be azimuthal periodic. This forces the electron wave function to have at least one azimuthal node, since otherwise it would require a discontinuity in the slope of the wave function. The GNR has no such restriction; the electron wave function at the edges of the CNR must have no periodicity. The extra nodes required in the CNT electron states lead to more curvature in the wave function and hence a larger expectation value for the kinetic energy. Thus, the GNR structure allows for lower energy modes than the CNT one.

A comparison of the characteristics of graphene nanoribbon (GNR) and carbon nanotube (CNT) materials is provided in Table 1 [10]. The data indicate that GNRs have superior characteristics than CNT for transistors design. Moreover, relatively efficient GNR performance can also be attributed to their smooth edges, which are a common defect when using CNTs [11]. The top-down chemical synthesis method has been presented in [12], producing GNRs that are precisely tailored in various chirality's, and form with widths <2 nm.

Table 1: Properties of CNT and GNR

Properties	CNT	GNR
fracture strength, GPa	45	124
density, g·cm−3	1.33	>1.0
electrical conductivity, S·cm−1	5000	10^6
mobility, cm2·V−1·s−1	100000	200000
thermal conductivity, W/mK	3000	5000

The maximum load or stress that a material can withstand before fracture is defined as fracture strength. It illustrates the resistance of the material to failure under a variety of applied stresses and loading modes, which is an important mechanical property. From Table1 the fracture strength of GNR is almost three times that of CNT, so GNR can have three times the resistance of CNT which states that breakdown in CNT is easier than in GNR. This will shorten the transit time of the charge carriers which increases the operational frequency of the device [4].

From the above table, the density of both CNT and GNR are the same, which means that density doesn’teffect GNR performance compared to CNT. However, due to the larger thermal contact resistance, CNTs are not viable for use in CMOS integration. Meanwhile, GNRs can easily be attached to heat sinks, thus eliminating the issues with

thermal contact resistance [19]. This suggests that GNRs could serve as promising materials for thermal management in CMOS devices and circuits.

Graphene is a zero-band-gap material and their 2D natures make it a perfect conductor[20].the energy band gap in graphene sheet can be formed by making graphene single sheet or bi-layer material processed into narrow strips with the channel width of WCH=2nm, which provides finite band gap is presented and resultant graphene layer characterized as a semiconductor[20].the energy band gap of the graphene nano-ribbon can be varied with inversely proportional to the width of nanoribbon strips.the width of the graphenenano-ribbon is determined by the number of dimmer lines N as WCH=√0.75(N+1)[21].SB-type and MOSFET-type GNRFETs are used in this technology. Nevertheless, MOSFET-type GNRFETs with a greater ION/IOFF ratio, SB-type prove better in high- functioning memory cells [22]. Scaling of transistors achieves CAM. The scaling of transistors results in reduced channel. In today's scenario, a need for improved performance is desired in terms of increased speed with a lower level of power dissipation. The high frequency Content-addressable memory (CAM) is a very fast search mechanism which performs fully-parallel comparisons between input search data and a table of storage data in a single clock cycle [5]. CAM has proven effective for applications that require fast search operation namely translation look-aside buffers [6] and PE (processing elements) tag directories in fully associative caches [7], network routers [8], database accelerators and image processing [9].

This paper proposes a BCAM cell built upon GNRFETs, based on the logic.` XNOR logic we detail the analysis of GNRFET for Average power and delay varying device parameters such as numbers of ribbons. We also discover an optimal parameter for minimum delay BCAM cells. GNRFET shows a good improvement in power consumption and delay when the number of ribbons are nominal. The rest of the paper is organized as follows. Section II provides the conventional operation of BCAM operation and the operation of SRAM devices. Section III discusses BCAM Cells using the proposed XNOR gate using different FET's like CNTFET's, MOS-GNRFET's and SBGNRFET's. Section IV contains analysis of performance and results of the proposed XNOR BCAM Cell. Section V concludes the paper. II CONVENTIONAL BCAM Conventional BCAM cell operation is presented to understand the proposed BCAM cell based on GNRFET. The basic operations of conventional BCAM cells such as read operation, write operation and search operation are explained in the following subsections

Conventional Binary CAM

A Binary Content Addressable Memory (BCAM) is used for storing single bit data. It is made up of two parts; a comparison circuit and a SRAM cell. The data is stored in a SRAM cell and search is done using a comparison circuit. In performing the READ and WRITE operations, you use word lines (WL) and bit lines (BLs). Each cell (bit) is connected to a match line (ML) that determines the logic level of the ML. The figure shows the conventional NOR-type BCAM circuitry. The basic SRAM cell is formed by transistors M1 to M6 and it can

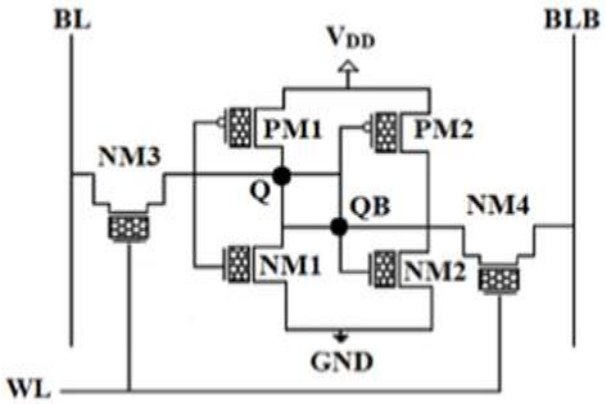

Figure 1: Diagram of 6-T SRAM

store either logic level. The comparison circuit is generated using transistors M7 to M10. If the search bit and stored bit are different, the ML is at logic 0.

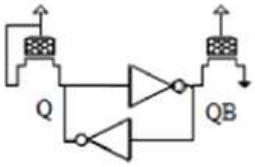

Figure 2: Write

Write operation: The term "access transistors" refers to the transistors M5 and M6. Both the read and write of data is accomplished by these transistors. By enabling the word line WL, the data read/write operations isperformed. When the word line is high, the data will be written on the bit line. For example, if we want to switch the internal node that has been initialized at logic low to logic high set WL=1 and set BL=1. The value will then be retained via the cross-coupled inverters. This process continues until the logic high value must be switched back to logic low, then set WL=1 and set BL=0.

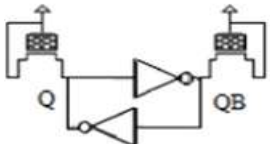

Figure 3: Read mode

Read operation

Figure 3: Read mode This operation is performed by making the word line to high level. The data is accessed through BL which is stored at the

internal nodes. For example, if we want to read the data at the internal nodes, set WL=1 and access the data present on BL

Search operation

The primary function of the cam is used for data storage and search operation, if the data to be searched is present on the internal node and similar to the data retrieved then the value on the ML will be in logic high otherwise, if there is no match, the ML will be logic low.

III PROPOSED BCAM

In this section, the BCAM memory cell made using a XNOR circuit will be examined. The operation of BCAM fundamentally depends on the search and stored data. The mechanism is such that the match line will be high if the search whether it is matched with the stored data which in fact means that the exact data is being searched for because the stored data is actually reference data.

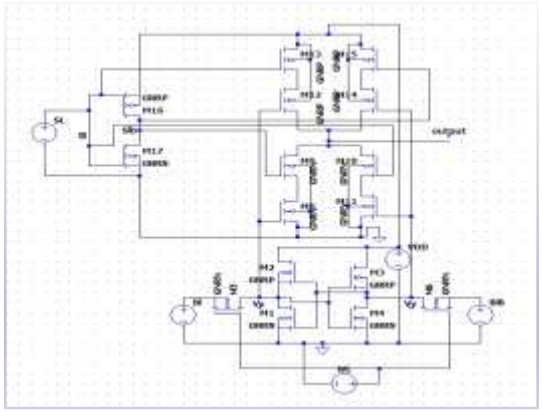

Figure 4: BCAM using XNOR logic

The truth table outlined in Table 3 shows the function of BCAM. The match line output is similar to the output of the XNOR logic. In previous literature the BCAM has been considered based on NAND and NOR logic but in both cases, the output is high only when both the stored data and search data are either one or zero. Other combinations do not give a logic high output for either of these logics. Therefore, this discussion hinges on the XNOR logic. The output of the match line is analogous to the output of the XNOR gate. The truth table of the BCAM associated with the output of the XNOR logic is shown in the following table.

Table 2:Truth table for BCAM XNOR with Transistor logic

V_x	SL	V_y	SLb	ML
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

Results and Discussion :-

The BCAM operates at 16 nm technology with CNTFET and various versions of GNRFET including a single and double gate MOS-type and SBGNR having distinct parameters examined in relation the number of tubes in the CNTFET and the number of ribbons in GNRFET.

1. Number of ribbons/tubes vs Average Power:

The fluctuations of the average power of the suggested model of BCAM for FET models such as CNTFET, MOS-GNRFET and SBGNRFET using single gate and double gate for different number of ribbons/tubes is examined and illustrated in Figure 5. The power used by the suggested circuits increases with the number of tubes/ribbons used. The power used by the CNTFET models and SBGNRFET models are very similar with slight power fluctuation, however the power used by the MOSGNREFT was least at a ribbon count of four, although the value was 1.5 times more than the values of the remaining three types of FETs.

2. Number of ribbons/tubes vs Average Delay:

The variations of the average delay of the proposed model of BCAM for FET models such as CNTFET,MOS-GNRFET and SBGNRFET using single gate and double gate for different number of ribbons/tubes is analysed and is shown in Figure 6.The time delayed by the

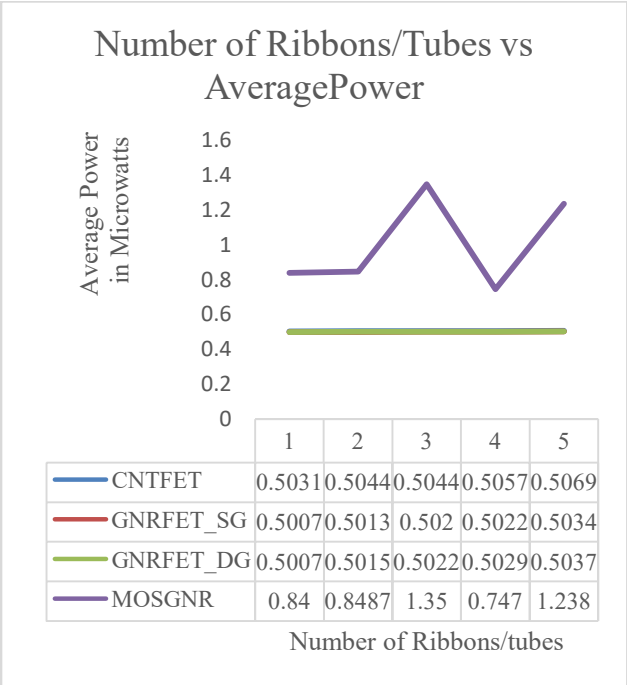

Figure 5:Plot showing relation between number of ribbons/tubes versus Average Power.

proposed circuits remains approximately the same value with increase in the number of tubes/ribbons for both types of SBGNRFET .It is observed that the time taken to initiate any operation is maximum for CNTFET which means that the switching time for CNTFET is compared to that of the GNRFET.The switching time of SBGNRFET is more compared to that of the MOSGNR, so the delay for these GNRFET is very small as shown in below figure

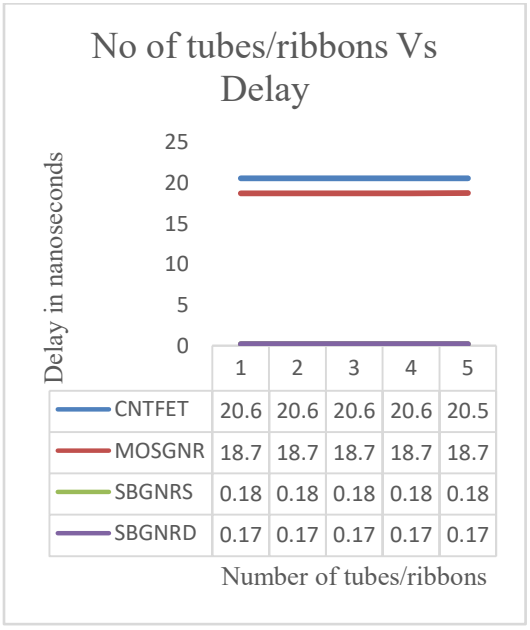

Figure 6: Plot showing relation between number of ribbons/tubes versus Average Delay

3. Number of ribbons/tubes vs Power Delay Product:

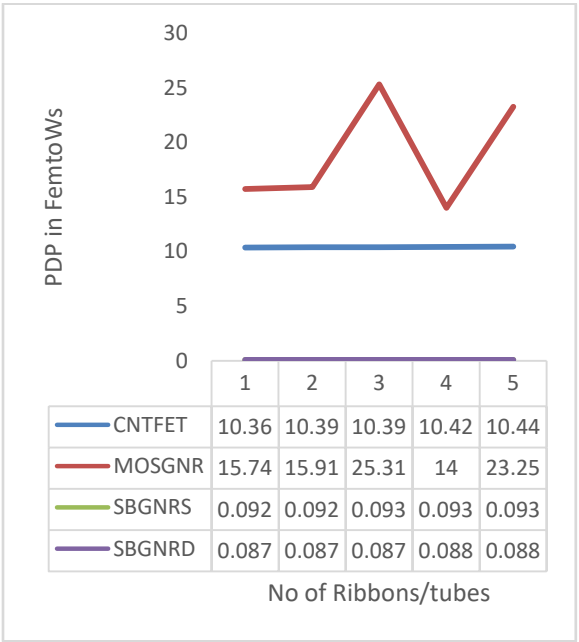

Figure 7:Plot showing relation between number of ribbons/tubes versus PDP.

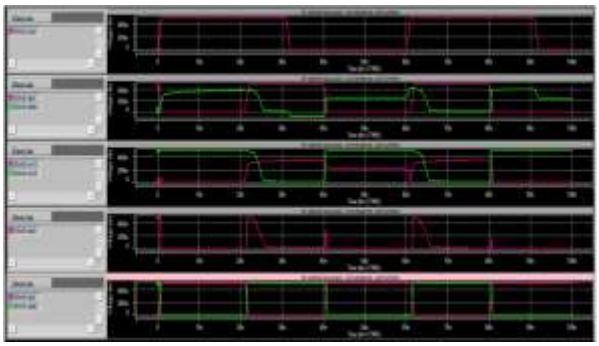

Figure8: Output waveform obtained using CNTFET XNOR logic

From the Figure 8,it is observed that when the wl,slis enabled and the bl is disabled then the value of v1 is disable ,which is given as input of the inverter the ouputblb as high.The value of blb is given as the input to the another inverter ,the values of the v1,v2,sl and slb are given as the inputs of the compensation circuit of the XNOR CMOS logic is high when either sl,v1 are equal or slb,v2 are equal. In this the values of blb,v2 and v1 are not attaining the maximum value due to their low Ion/Ioff ratio and the low mobility of CNTFET

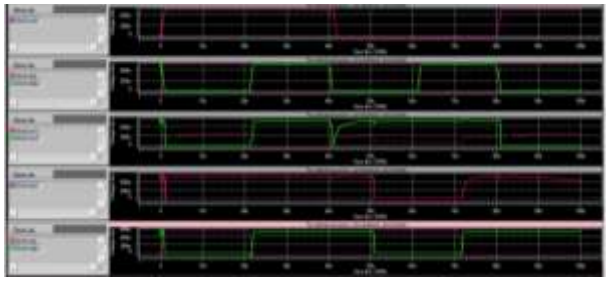

Figure9: Output waveform obtained using MOS-GNRFETwith XNOR logic

From the Figure 9,it is observed that when the wl,sl is enabled and the bl is disabled then the value of v1 is disable ,which is given as input of the inverter the ouputblb as high .The value of blb is given as the input to the another inverter ,the values of the v1,v2,sl and slb are given as the inputs of the compensation circuit of the XNOR CMOS logic is high when either sl,v1 are equal or slb,v2 are equal. In this due to the mobility and conductivity of the GNRFET, it is observed that logic high is obtained

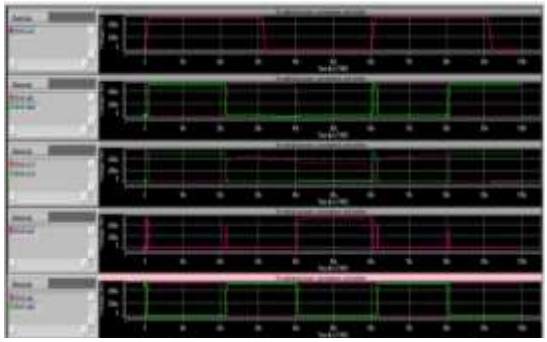

Figure 10: Output waveform obtained usingSB-GNRFET-SG with XNOR logic

From the Figure 10,it is observed that when the wl,sl is enabled and the bl is disabled then the value of v1 is disable ,which is given as input of the inverter the ouputblb as high .The value of blb is given as the input to the another inverter ,the values of the v1,v2,sl and slb are given as the inputs of the compensation circuit of the XNOR CMOS logic is high when either sl,v1 are equal or slb,v2 are equal. In this due to the mobility and conductivity of the GNRFET, it is observed that logic high is obtained.

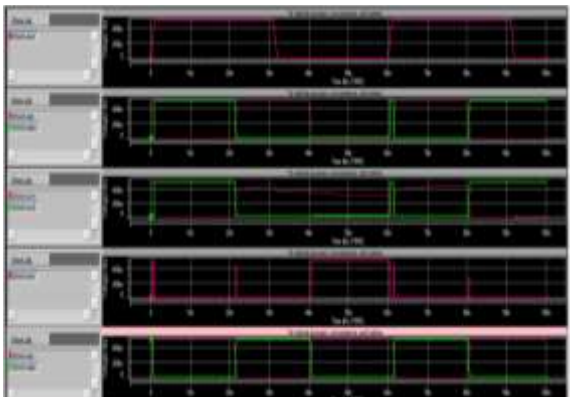

Figure 11: Output waveform obtained using SB-GNRFET-DG with XNOR logic

From the above results of CNTFET and SB-GNRFET, it is observed that the inverters in MOS-GNRFET, CNTFET are not switching as fast as the inverters that are implemented using SB-GNRFET. Due to the low mobility of the transistor in CNTFET and MOS-GNRFET,it is observed that the match of the data stored and searched is not accurate as it is accurate in the SB-GNRFET.

Conclusion:-

This study focuses on the design and evaluation of Content Addressable Memory (CAM) architectures based on Graphene Nanoribbon Field Effect Transistors (GNRFETs) to assess their viability in future generation amplifier circuits. Results show that GNRFETs outperform conventional CAMs in speed, power consumption and scalability. Thanks to characteristics such as high mobility carrier, adjustable bandgap, and reduction in short-channel effects, the approach shows increases in search speeds, decreases in leakage power, and increases in signal integrity which are important for high speed data processing and low power amplifier circuits.

Overall, it is shown in this work that the implementation of GNRFET technology in CAM architectures may improve computational performance with lower power consumption, and it is a strong candidate for future nanoelectronic

systems as well as more advanced analog or digital amplifiers. Future potential will include fabricable studies, variations, and hybrid GNRFET–CMOS integration to facilitate future large–scale applications.

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