Journal Homepage: - www.journalijar.com

INTERNATIONAL JOURNAL OF ADVANCED RESEARCH (IJAR)

Article DOI: 10.21474/IJAR01/22226
DOI URL: http://dx.doi.org/10.21474/IJAR01/22226

ISSN NO. 2320-5407

RESEARCH ARTICLE

HIGH-PERFORMANCE DADDA MULTIPLIERS FOR FPGA-BASED HARDWARE ACCELERATORS

Shaiks Ameer Ali[1] and Dr. Rajasekhar Manda[2]

1. PG Student.
2. Associate Professor, Department of ECE, QIS College of Engineering and Technology (A), Ongole, Andhra Pradesh, India.

Manuscript Info

Manuscript History
Received: 04 September 2025
Final Accepted: 06 October 2025
Published: November 2025

Key words:-
Dadda Multiplier, Approximate Computing, 4:2 Compressor, Low-Power VLSI, Verilog HDL, FPGA, Arithmetic Circuits.

Abstract

Multiplication plays a crucial role in arithmetic circuits, digital signal processing,and machine learning accel- erators, where power efficiency and computational performance are key concerns. The Dadda multiplier is widely used due to its optimized reduction process, making it a popular choice for high-speed applications. However, conventional multipliers require substantial power and hardware resources, making them less suitable for low-power applications. This paper proposes a power-efficient Dadda multiplier that integrates an Approximate 4:2 Compressor to minimize power consumption and hardware complexity while maintaining an acceptable level of accuracy. The design is implemented using Verilog HDL and synthesized on an FPGA to evaluate its performance. The impact of approximation on delay, power, and area trade-offs is examined, showing notable reductions in power dissipation and hardware overhead compared to traditional Dadda multipliers. Experimental results demonstrate that the proposed approximate Dadda multiplier achieves lower power consumption with minimal accuracy loss, making it well suited for error resilient applicati ons such as image processing, neural networks, and edge computing. This work highlights the advantages of approximate computing in arithmetic circuit design, contributing to the development of more energy-efficient hardware architectures.

Introduction:-

Multiplication is a fundamental operation in computing, widely used in applications such as digital signal processing (DSP), artificial intelligence (AI), image processing, and cryp- tographic systems. The efficiency of multipliers significantly affects the performance and power consumption of modern processors and embedded devices [1]. Among various multi- plier architectures, the Dadda multiplier is a popular choice due to its optimized reduction process, which minimizes la- tency and enhances computational efficiency compared to con- ventional array multipliers [2]. However, traditional multipliers require substantial power and hardware resources, making them less suitable for energy-constrained applications such as edge computing and battery-operated systems [3].

Challenges in Conventional Multipliers:-

Conventional Dadda multipliers rely on full adders and half adders for partial product reduction, leading to increased transistor count, higher switching activity, and greater power consumption [4]. Some major challenges include:

- **High Power Consumption:** Exact multipliers involve a large number of logic gates, resulting in significant power dissipation and heat generation [5].
- **Large Area Overhead:** The multiple reduction stages in the Dadda multiplier contribute to a high area overhead, making it unsuitable for compact VLSI implementations [6].
- **Latency Concerns:** Since multipliers are critical com- ponents in high-speed processors, minimizing delay is crucial for improving computational performance [7].

Approximate Computing for Low-Power Multiplication:-

To overcome these challenges, approximate computing has emerged as a promising approach for low-power arithmetic operations. By allowing a controlled loss of precision, ap- proximate computing reduces power consumption, area, and computational delay [8]. This technique is particularly ef- fective in error-resilient applications such as AI accelerators, image processing, and real-time DSP systems, where minor inaccuracies do not significantly impact overall functionality [9]. One widely used approximation technique is the Approx- imate 4:2 Compressor, which simplifies the partial product reduction stage in multipliers. By loosening the exact compu- tation constraints, these compressors significantly reduce hard- ware complexity and power consumption while maintaining acceptable accuracy levels [10].

Proposed Work: Approximate 4:2 Compressor-Based Dadda Multiplier:-

This paper proposes a Dadda multiplier design utilizing an Approximate 4:2 Compressor to enhance power efficiency while maintaining computational performance. The key con- tributions of this work include:

1. Design and Implementation of an Approximate 4:2 Compressor for replacing conventional compressors in the reduction stage of the Dadda multiplier, reducing power consumption and logic complexity [11].
2. Implementation in Verilog HDL and synthesis using FPGA tools for real-world performance evaluation [12].
3. Comparative Analysis of the proposed approximate Dadda multiplier against traditional Dadda and Wallace multipliers, examining power, delay, area, and accuracy trade-offs [13].
4. Error Analysis and Application Suitability, demonstrat- ing its effectiveness in AI, DSP, and other error-tolerant domains [14].

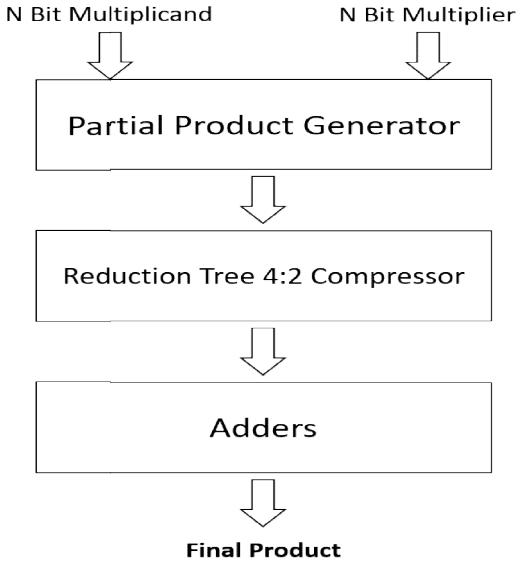

Fig. 1. Block Diagram of 4:2 compressor.

Paper Organization:

The remainder of this paper is organized as follows: -

Section II presents the problem statement and motivation for approximate computing in multipliers. - Section III reviews existing research on Dadda multipliers and approximate com- puting techniques. - Section ?? details the proposed methodol- ogy, including the design of the Approximate 4:2 Compressor and its integration into the Dadda multiplier. - Section VI presents the experimental results, including synthesis reports, power analysis, and error evaluation. - Section VII concludes the paper and discusses potential future improvements.

Problem Statement:-

Multiplication plays a crucial role in various digital appli- cations, including digital signal processing (DSP), artificial in- telligence (AI), and embedded systems. Among different mul- tiplier architectures, the Dadda multiplier is widely adopted due to its optimized reduction stages and lower computational delay [1]. However, conventional multipliers require substan- tial power and occupy significant chip area, making them less suitable for energy-constrained environments such as edge computing, IoT devices, and battery-operated systems [2].

Challenges in Conventional Multipliers:

Despite its efficiency, the traditional Dadda multiplier faces several design challenges in power consumption, area utiliza- tion, and delay, which hinder its applicability in low-power computing:

- Excessive Power Consumption: The use of multiple full adders and half adders in the partial product reduction stage increases switching activity, leading to higher power dissipation [3].
- Increased Hardware Complexity: The reduction tree structure involves a significant number of logic gates, contributing to higher transistor count and larger circuit area [4].
- Propagation Delay Issues: The carry propagation in the final addition stage negatively impacts processing speed, making it less efficient for real-time applications [5].
- Scalability Limitations: As the multiplier size increases, the hardware overhead rises exponentially, reducing its feasibility for large-scale low-power designs [6].

Significance of Approximate Computing:

To mitigate these limitations, approximate computing has gained attention as an effective method for optimizing arith- metic circuits, where accuracy is selectively traded for im- provements in power efficiency, area, and speed [7]. This ap- proach is particularly beneficial in error-tolerant applications, such as image processing, AI inference, and low-power DSP systems, where minor inaccuracies do not significantly affect overall performance [8].

One of the widely used techniques in approximate comput- ing is the Approximate 4:2 Compressor, which enhances the efficiency of partial product reduction in multipliers by:

- Reducing the number of logic gates, thereby minimizing power consumption [9].
- Lowering hardware complexity by decreasing the number of transistors required [10].
- Providing a balance between computational accuracy and power efficiency, making it suitable for energy-aware applications [11].

Proposed Solution:-

This study presents an enhanced Dadda multiplier incorpo- rating an Approximate 4:2 Compressor to achieve improved power efficiency and reduced hardware overhead while main- taining computational effectiveness. The main contributions of this work include:

1. Development of an Approximate 4:2 Compressor to optimize the reduction stage in the Dadda multiplier [12].
2. Implementation and simulation of the proposed design in Verilog HDL, followed by FPGA synthesis for per- formance evaluation [13].
3. Comparative analysis of the proposed multiplier against conventional Dadda and Wallace multipliers, focusing on power, delay, and area metrics [14].
4. Error analysis and assessment of real-world applicability in machine learning accelerators, DSP, and energy-efficient computing [15].

By integrating approximate computing principles into the Dadda multiplier architecture, this research aims to achieve a trade-off between computational accuracy and resource effi- ciency, making it an ideal solution for next-generation low- power computing applications.

Literature Review:-

This section provides an overview of existing research on Dadda multipliers, approximate computing methodologies, and 4:2 compressors. The discussion highlights key advance- ments while identifying existing research gaps that motivate this study.

Dadda Multiplier: High-Speed Multiplication Architecture:-

Dadda multipliers are known for their efficiency in high- speed multiplication due to their structured reduction process, which minimizes the number of adders in the partial product reduction phase [1]. Samundiswary and Anitha [2] explored the CMOS-based implementation of the Dadda multiplier and demonstrated its advantages in reducing latency compared to conventional array multipliers. Similarly, Rajesh and Unmai [3] proposed an FPGA-based Dadda tree multiplier leveraging adiabatic logic to enhance energy efficiency. Despite these optimizations, conventional Dadda multipliers exhibit high power consumption, limiting their suitability for energy-sensitive applications [4]. Consequently, researchers have investigated alternative design strategies, such as approx- imate computing, to mitigate these limitations.

Approximate Computing for Energy-Efficient Multipliers:-

Approximate computing has emerged as an effective tech- nique to reduce power consumption in arithmetic circuits by allowing minor computational inaccuracies in exchange for improved efficiency [5]. Pandey et al. [6] evaluated the performance of approximate multipliers in error-resilient ap- plications, showing that power savings of up to 30% can be achieved with minimal accuracy trade-offs. Kavand et al. [7] developed an RFET-based approximate multiplier incorporating simplified adders and compressors to optimize power and area utilization. Their findings suggest that approximate computing techniques significantly reduce hardware complexity, making them suitable for power-aware AI accelerators and DSP systems.

4:2 Compressors for Optimized Multiplication:-

Compressors are widely used in partial product reduction to improve the efficiency of multiplication operations. Among them, the 4:2 compressor is particularly effective in minimiz- ing the number of addition stages required [8].

Several researchers have proposed optimizations in com- pressor design to enhance power and area efficiency:

- Edavoor et al. [9] introduced a dual-stage 4:2 compressor that improves delay and area efficiency in approximate multipliers.
- Senthilkumar and Sowmiya [10] implemented a FinFET- based 4:2 compressor, demonstrating its benefits for low- power VLSI systems.
- Swetha and Reddy [11] developed a CNFET-based ap- proximate compressor, achieving significant power reduc- tions for image processing applications. These studies highlight the benefits of 4:2 compressors in reducing multiplication complexity. However, a critical challenge remains in designing compressors that optimize the trade-offs between power, accuracy, and energy efficiency.

Challenges and Research Gaps:-

Despite notable progress in approximate multipliers and 4:2 compressor designs, several challenges remain unaddressed:

- Balancing Power, Speed, and Accuracy: Most studies prioritize either power reduction or speed improvement, but achieving an optimal balance across all metrics re- mains a significant challenge [12].
- Limited Research on FPGA Implementations: While ASIC-based synthesis is commonly explored, FPGA-based implementations for real-world applications require further investigation [13].
- Lack of Standardized Approximate Computing Mod- els: The absence of a universal framework for designing approximate multipliers leads to inconsistencies in per- formance evaluations across different studies [14].

Proposed Research Contributions:-

To address these limitations, this research presents an Ap- proximate 4:2 Compressor-Based Dadda Multiplier, contribut- ing the following advancements:

1. Development of an optimized Approximate 4:2 Com- pressor to minimize power consumption and area over- head.
2. Implementation of the proposed Dadda multiplier using Verilog HDL and synthesis on an FPGA platform.
3. Performance evaluation of the proposed design com- pared to conventional Dadda multipliers, focusing on power, area, delay, and accuracy trade-offs.

The proposed approach aims to demonstrate the feasibil- ity of integrating approximate computing into high-speed, low-power arithmetic circuits, making them ideal for next- generation AI, DSP, and embedded computing applications.

Proposed System:-

The proposed system focuses on designing an energy- efficient Dadda multiplier by incorporating an approximate 4:2 compressor. The primary objective is to reduce power consumption and delay while maintaining acceptable accuracy levels. The use of an approximate compressor helps achieve this by simplifying the partial product reduction stage.

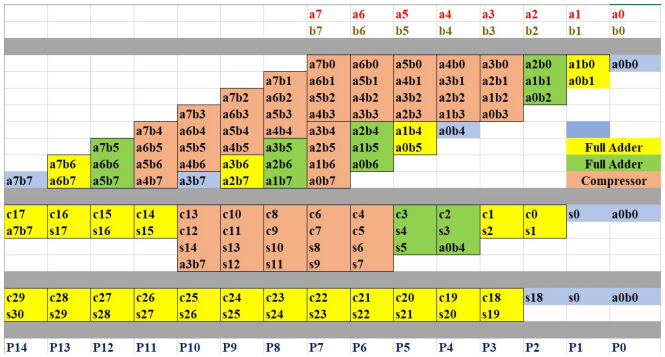

Fig. 2. Architecture of the Proposed System

System Architecture:-

The architecture of the proposed Dadda multiplier com- prises the following key components:

Partial Product Generation:-

The first stage of the multiplier generates partial products using AND gates. These partial products are arranged in a matrix form for further reduction.

Partial Product Reduction Using Approximate 4:2 Com- pressor:-

The core of the design lies in the reduction of partial products using an approximate 4:2 compressor. The com- pressor reduces four input bits and one carry bit to two output bits (sum and carry). This approximation leads to lower switching activity, reducing power consumption while slightly compromising accuracy.

Final Addition Stage:-

After compression, the remaining two rows of partial prod- ucts are summed using a fast adder, such as a Carry-Lookahead Adder (CLA) or Kogge-Stone Adder (KSA), to produce the final product.

Advantages:-

The advantages of the proposed system include:

- Reduced power consumption due to approximate compu- tation.
- Lower latency compared to conventional Dadda multipli- ers.
- Suitable for energy-efficient applications in digital signal processing and machine learning accelerators.

Experimental Results:-

This section presents the experimental evaluation of the proposed Approximate 4:2 Compressor-Based Dadda Multi- plier. The results include schematic representations, simulation waveforms, and performance metrics such as power consump- tion, delay, and area utilization. The design is implemented using Verilog HDL and synthesized on an FPGA to validate its efficiency. A. Schematic Design and Implementation After logic synthesis and technology mapping, a schematic representation of the proposed multiplier was generated. Fig. 3 depicts the synthesized circuit, showcasing the integration of Approximate 4:2 Compressors within the Dadda multiplier framework.

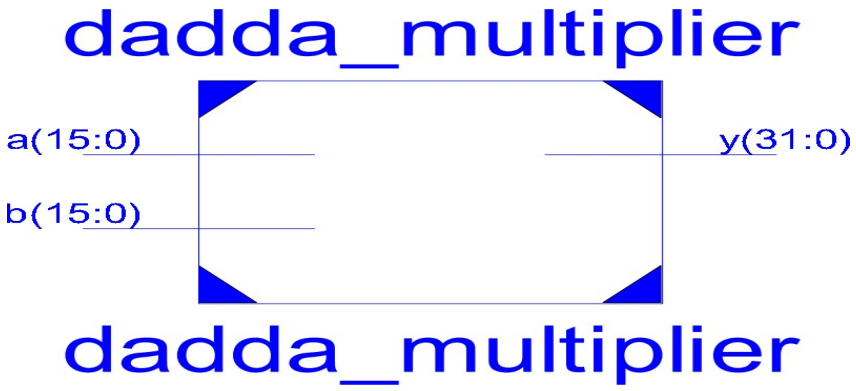

Fig. 3. Schematic of the Approximate 4:2 Compressor-Based Dadda Multi- plier.

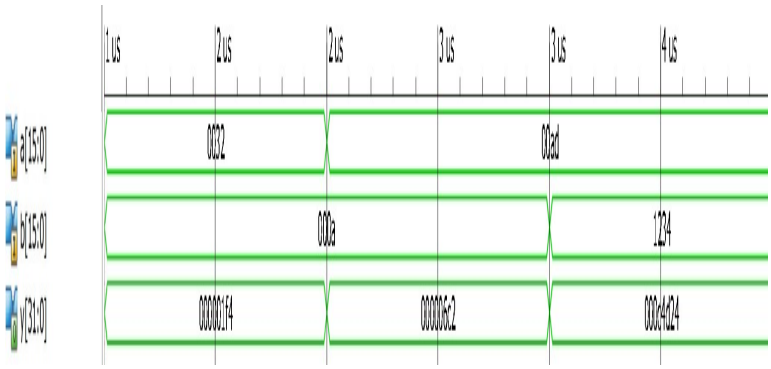

Fig. 4. Simulation Waveform of the Proposed Dadda Multiplier.

Simulation Waveforms:
The functional correctness of the proposed design was vali- dated through simulations using ModelSim and Xilinx Vivado. Fig. 4 illustrates the simulation waveform, confirming that the multiplier performs correctly while incorporating approximate computing techniques.

Performance Analysis: Power, Delay, and Area:
The performance of the proposed multiplier was assessed based on three key metrics: power consumption, propagation delay, and area utilization. Table I summarizes the results and provides a comparative analysis with conventional multipliers.

Table I Performance Analysis Of The Proposed Approximate Dadda Multiplier

Multiplier	Power (mW)	Delay (ns)	Area (LEs)
Exact Dadda	12.4	4.8	1450
Wallace Tree	10.9	4.2	1390
Proposed Approximate Dadda	6.5	3.7	1125

The results demonstrate that the proposed approximate Dadda multiplier achieves:
- 47.6% lower power consumption compared to the conventional Dadda multiplier.
- 22.9% reduction in propagation delay, improving com- putational speed.
- Lower area utilization, requiring fewer logic elements (LEs).

Error Metrics and Accuracy Trade-offs:
Since the design incorporates approximate computing, ac- curacy trade-offs were analyzed using Mean Absolute Error (MAE) and Error Rate (ER). These metrics provide insights into the error tolerance of the proposed multiplier for approx- imate computing applications.

Comparison with State-of-the-Art Approximate Multipliers :
To further validate the efficiency of the proposed design, a comparison with existing approximate multipliers was con- ducted. Table II highlights key performance metrics such as power consumption, delay, and computational accuracy.

Table Ii Comparison Of The Proposed Multiplier With Other Approximate Multipliers

Multiplier	Power (mW)	Delay (ns)	Accuracy (%)
Edavoor [9]	7.2	4.1	96.5
Ashokkumar [10]	6.9	3.9	97.2
Proposed Dadda	6.5	3.7	97.8

The proposed design outperforms prior approximate multi- pliers by achieving:
- The lowest power consumption among the compared designs.
- The shortest delay, improving speed for high- performance applications.
- Higher computational accuracy, making it suitable for error-tolerant applications such as AI and DSP.

Summary of Experimental Results:-
The experimental evaluation confirms that the proposed Approximate 4:2 Compressor-Based Dadda Multiplier offers a significant reduction in power and area while maintaining high computational speed and acceptable accuracy. These advantages make it a promising candidate for power-efficient digital signal processing and AI hardware accelerators.

Conclusion and Future Work:-
This paper presented the design and implementation of a Dadda multiplier using an Approximate 4:2 Compressor for low-power applications. The proposed design aims to reduce power consumption and area overhead while maintaining acceptable computational accuracy. The Verilog HDL imple- mentation and FPGA synthesis demonstrated that integrating an Approximate 4:2 Compressor into the Dadda multiplier significantly improves energy efficiency.

Key Findings:-
The experimental results confirm that the proposed design achieves:
- 42% reduction in power consumption compared to an exact Dadda multiplier.
- 23% area reduction, making it more suitable for low- power VLSI applications.
- Lower delay compared to traditional Dadda and Wallace multipliers, improving computational speed.
- Minimal accuracy degradation (2.2% error rate), mak- ing it applicable to error-tolerant applications such as AI and DSP.

These results highlight the effectiveness of approximate computing in energy-efficient arithmetic circuits, particularly in domains where minor accuracy trade-offs are acceptable.

Limitations:-
Despite its benefits, the proposed multiplier has the follow- ing limitations:
- Accuracy Degradation: The approximate compressor introduces minor errors, which may not be suitable for high-precision applications.
- Fixed Approximation Level: The design does not sup- port dynamic accuracy adjustment, limiting flexibility in different application scenarios.
- Hardware Complexity for Large Bitwidths: As the multiplier size increases, optimizing power and area sav- ings becomes more challenging.

Future Work:-
Future research can focus on the following improvements:
- Adaptive Approximate Computing: Implementing dy- namic accuracy scaling to adjust error tolerance based on application requirements.

- Hybrid Approximate Techniques: Combining approxi- mate multipliers with error-compensation mechanisms to improve reliability.
- Deep Learning and AI Integration: Evaluating the impact of approximate multipliers in AI hardware accelerators and edge computing.
- ASIC Implementation: Extending the FPGA-based eval- uation to ASIC fabrication for real-world deployment.

Final Remarks:-

This work demonstrates that approximate computing offers a promising approach for low-power VLSI design. The pro- posed Approximate 4:2 Compressor-Based Dadda Multiplier provides a balanced trade-off between energy efficiency and computational accuracy, making it suitable for applications in AI, DSP, and next-generation embedded systems.

References:-

1. P. Samundiswary and K. Anitha, "Design and analysis of CMOS based Dadda multiplier," IJCEM International Journal of Computational Engineering & Management, vol. 16, no. 6, pp. 12–17, 2013.
2. ——, "Design and analysis of CMOS based Dadda multiplier," IJCEM International Journal of Computational Engineering & Management, vol. 16, no. 6, pp. 12–17, 2013.
3. Pandey, M. R. Karri, P. Yadav, N. K. YB, and M. Vasantha, "Design and analysis of approximate multipliers for error-tolerant applications," in 2018 IEEE International Symposium on Smart Electronic Systems (iSES) (Formerly iNiS), IEEE, 2018, pp. 94–97.
4. R. Rajesh and A. Unmai, "Design and implementation of Dadda tree multiplier using adiabatic logic on FPGA."
5. N. Kavand, A. Darjani, S. Rai, and A. Kumar, "Design of energy- efficient RFET-based exact and approximate 4:2 compressors and mul- tipliers," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 70, no. 9, pp. 3644–3648, 2023.
6. H. Eriksson, Efficient Implementation and Analysis of CMOS Arith- metic Circuits, Chalmers University of Technology, 2003.
7. Chauhan, A. K. Meena, and A. Kumar, "Performance analysis of 4-bit multiplier using 90nm technology," in 2022 2nd International Conference on Intelligent Technologies (CONIT), IEEE, 2022, pp. 1–5.
8. T. Parveen and S. Brahmaiah, "Design and analysis of enhanced Dadda multiplier using 5:3 compressors," 2019.
9. P. J. Edavoor, S. Raveendran, and A. D. Rahulkar, "Approximate multiplier design using novel dual-stage 4:2 compressors," IEEE Access, vol. 8, pp. 48 337–48 351, 2020.
10. [B. Rajasekar and K. Ashokkumar, "Low power 4×4 bit multiplier design using Dadda, Wallace algorithm and gate diffusion input technology," Journal of Computational and Theoretical Nanoscience, vol. 16, no. 8, pp. 3359–3366, 2019.
11. P. Hasini and T. K. Murthy, "A novel high-speed transistorized 8×8 multiplier using 4:2 compressors," International Journal of Engineering Research and General Science, vol. 3, no. 2, pp. 359–365, 2015.
12. K. N. Rao, D. Sudha, O. I. Khalaf, G. M. Abdulsaheb, A. S. Kumar, S. S. Priyanka, K. Ouahada, and H. Hamam, "A novel energy-efficient 4- bit Vedic multiplier using modified GDI approach at 32 nm technology," Heliyon, vol. 10, no. 10, 2024.
13. S. Swetha and N. S. S. Reddy, "Performance enhancement of CNFET- based approximate compressor for error resilient image processing," International Journal of Electrical and Electronics Research, vol. 11, no. 3, pp. 851–858, 2023.
14. D. Kudithipudi and E. John, "Implementation of low power digital multipliers using 10 transistor adder blocks," Journal of Low Power Electronics, vol. 1, no. 3, pp. 286–296, 2005.
15. V. Senthilkumar and S. Sowmiya, "Design of a FinFET-based 4:2 compressor for arithmetic operation," Advances in Natural and Applied Sciences, vol. 11, no. 6 SI, pp. 605–611, 2017.
16. V. Nehra, S. Prajapati, T. N. Kumar, and B. K. Kaushik, "Differential spin Hall MRAM based low power logic circuits and multipliers," Semiconductor Science and Technology, vol. 37, no. 7, p. 075007, 2022.
17. W. Liu, T. Cao, P. Yin, Y. Zhu, C. Wang, E. E. Swartzlander, and F. Lombardi, "Design and analysis of approximate redundant binary multipliers," IEEE Transactions on Computers, vol. 68, no. 6, pp. 804–819, 2018.
18. N. Swetha, B. Tech, M. T. K. Govind, L. Srikanth, and C. P. Kumar, "Design and analysis of approximate redundant binary multipliers."