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RESEARCH ARTICLE

THE HARDWARE-EFFICIENT IMPLEMENTATION OF A RECONFIGURABLE LOW-LATENCY POLAR CODING PROCESSOR FOR 5G SYSTEMS

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Abstract

People often use polar codes, which are error correcting codes, in com munication networks. Polar codes are better at fixing mistakes than other codes.This study suggests a VLSI architecture for the Polar decod er. The Maximum- Posteriori (MAP) algorithm is used for interleavers, deinterleavers, and soft-in-soft-out decoders. This study employs two recursive convolutional encoders and a pseudorandom interleaver on the encoder side. We used Verilog HDL to design the system and Xilinx ISE 13.2 to test it. The most traffic on 5G mobile broadband is projected to be 20Gbps. After 5G, data speeds are expected to reach terabits per second. The fastest polar code implementations can send data at 5Gbps. Because of this, Turbo and LDPC codes, which made 3G and 4G systems work, are missing from many new 5G apps. Polar coding is a new thing in 5G. It is a strong candidate for 5G New Radio since it guarantees top performance in 5G situations. This article says that polar codes are good for 5G uses.

Introduction:-

Part I: Introduction:-

Current works in computer-aided design, design analysis, implementation, simulation testing, and VLSI design are presented. It comprises studies on current VLSI design difficulties, technical advances, and education. This gives academic, industry, and other scholarly VLSI Design authors a dynamic, exceptional global venue for original papers and tutorials. Since microelectronics were invented, four generations have passed—a far shorter time period than the normal human lifespan. In the early 1960s, SSI low-density manufacture used roughly 10 transistors. In the late 1960s, when a chip could hold 100 transistors, Medium Scale Integration took over. In contrast to past years when the military handled much of the job, research prices dropped and private enterprises began to compete. The

first integrated circuit revolution began with transistor-transistor logic (TTL), which outlasted ECL and had higher integration density. In the early 1970s, transistor counts rose to 1000 per chip, called "Large Scale Integration." VLSI creates integrated circuits by assembling hundreds of transistor-based circuits on a chip. When sophisticated semiconductor and communication technologies were developed in the 1970s, VLSI began. The microprocessor is VLSI. Chips today have hundreds of millions of transistors, making the expression less popular.Trace concentrations of some substances can influence semiconductors' electrical properties, including free electrons and holes and crystal structure.

N-type semiconductors have free electrons and antimony, arsenic, or phosphorus dopants. Free-hole semiconductors are P- type. Boron, indium, and gallium are common dopants. Implants are utilized to introduce dopants into the semiconductor, then heat disperses them. The SIA Roadmap, Semiconductor Manufacturers 2001 Ranking, speed/power performance of existing technologies, and microelectronics development are the main uses of IC technology. PMOS, NMOS, CMOS, Bi CMOS, GaAs, and other VLSI technologies are MOS technologies. Minimum line width, transistor cross section, charge inversion channel, source attached to substrate, enhancement vs. depletion mode devices, and PMOS being 2.5 times slower than NMOS due to electron and hole mobility are basic MOS transistors. Massive crystals of chemically pure silicon. Wafers are sliced crystals with optical smooth surfaces, thicknesses of less than 1 mm, and diameters of 150, 200, and 300 mm. Finally, the wafer is processed.

Each wafer produces many chips with chip die sizes ranging from 5 mm by 5 mm to 15 mm by 15 mm. Processing is done per wafer. Each die will 1 have P- or N-type components and a few additional atoms implanted or doped. Most connections use metal insulation, usually SiO2 or SiN. The twin-tub, n-well, and p-well CMOS manufacturing techniques make all wafer devices simultaneously. Application-specific integrated circuits (ASICs) are ICs built for a specific function. ASIC is a semiconductor designed to power a cell phone. Application-specific standard products differentiate ASICs and industry-standard ICs like the 7400 or 4000 series. With smaller feature sizes and better design tools, an ASIC's maximum complexity (and utility) has expanded from 5,000 gates to over 100 million. Full 32-bit CPUs and massive memory blocks like ROM, RAM, EEPROM, Flash, and others are common in modern ASICs. Such ASICs are called SOCs.

Preliminaries:-

A. SCL with CRC assistance and SCL SCL maintains L candidate paths by forking at each information bit and keeping the best L by path metric (PM). Better performance, but more difficult. CRC is appended to K bits in CRC-aided SCL, and at the end, a path that passes CRC—which is typical in 5G—is selected. For route management, metric sorting (partial sort), and parallel path memory (L copies), SCL technology requires a significantly larger space. FPGA and VLSI considerations Quantize LLRs: usually 6–8 bits. Test the effect on FER/BER using a fixed point. Memory: LLR and partial-sums on FPGA are stored in BRAMs. Use SRAM blocks for ASIC. The encoder and decoder can be fully pipelined for throughput; the SC decoder is serial, but it is possible to instantiate multiple PEs or pipeline PE chains for node processing in parallel. Throughput vs. area: To boost throughput at the expense of area, instantiate more PEs (spatial parallelism). Low-power and clock gating: employ bit-serial units if space is limited, and gate when not in use. Use PE complexity plus memory size to estimate gate counts for ASIC. LLR memory of 1024*8 bits ~ 8Kb plus control and PEs for N=1024.

Encoder, SC Decoder:-

The coding world looks up to polar codes since they let you decode several times to get near to channel capacity with a basic constituent code. Polar coder architecture is made up of polar encoders and decoders. The encoder has two RSCs and one interleaver. The pseudo-random interleaver used in this paper makes the interleaved code large and hard to read, which helps random code work better. Polar code implementation utilizes RSC encoders in lieu of convolutional encoders due to their provision of low-weight parity codes. The MAP algorithm decodes polar encoded data that has been purposefully corrupted to create output that is free of errors. We use the uniform interleaver assumption to figure out the average WEF of concatenated code. Simulations demonstrate that upper constraints on BLER can accurately predict the performance of concatenated codes in terms of BLER. Using multiple Q SCL decoders at the same time for Q > 1 makes it easier to read the concatenated code. The suggested concatenated code with P = Q = 2 does better than the CRC-aided i-polar code with P = Q = 1 at high SNRs for the same length and code rate, according to analysis and simulation.

Proposed work:-
Use systematic RRA or IRA codes [9] for the code on the outside. The upper limits of BLER are good at predicting how well concatenated code will work.

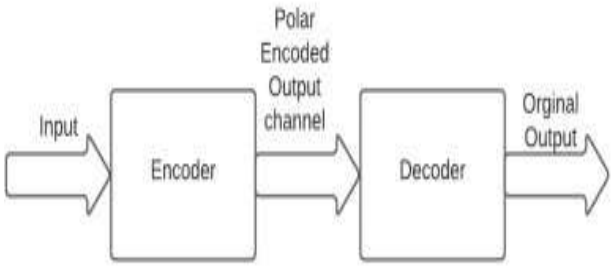
System model:-
The suggested (CNN,Deep learning) algorithm system model stages are below:

- Polar codes achieve channel capacity they can transmit at the highest possible rate over binary- input memory less symmetric (BMS) channels.
- The generator matrix GN = F⊗log2N (where F = [[1, 0], [1, 1]]) allows fast O (N log N) encoding using a structured XOR network.
- Recursive techniques allow O (N log N) complexity for both encoding and SC decoding.
- Combine information bits uA and frozen bits uAc into uN, then apply recursive polar encoding using Kronecker products.
- Decoding process Successive Cancellation (SC) decoder estimates transmitted bits uN from received yN, keeping only information bits uA.
- SC decoding uses frozen bits to sequentially estimate each bit, with complexity O (N log N), making it practical for hardware implementation.

Working:-
In Fig.1 Two identical the polar encoder is made up of pseudorandom interleavers and recursive convolutional encoders (RSC) (figure 1). A 1/3 rate parallel concatenated polar coding is used by LTE. Two distinct sets of data are used by each RSC. The first encoder gets the original data, and the second encoder gets the interleaved input. Interleaving is mixing up bits of data using a set procedure. Interleaving has an effect on how well the decoder works. Figure 6 demonstrates how the polar encoder's 24-bit output is made by combining systematic input with the outputs of the RSC1 and RSC2 encoders. The channel will send this to the Polar decoder. Figure 3 displays a standard polar decoder block architecture that has two SISO modules, two pseudorandom interleavers, and a deinterleaver. .

Results of tests:-
SISO decoders use the real (soft) value of the signal as input. The decoder then figures out how likely it is that each bit of data sent matches each bit of input. This work examines a maximum a-posteriori (MAP) polar decoder for the SISO component decoder. The MAP algorithm does not restrict bit estimations to legitimate trellis paths. So, a Viterbi decoder that finds the most likely trellis path shouldn't make that. AES can be implemented in both software and hardware. With fewer ramifications and low seed, software implementation is less costly and resource-intensive. We need a lot of data these days, and hardware implementation has become necessary due to our high speed requirements. We only have application-specific IC and FPGA as hardware. FPGA is a programmable device that allows for a wider range of functions than ASIC. As a result, we prefer implementing AES on FPGAs. During interleaving, the interleaver arranges the message symbols across multiple code blocks before sending them over network channels. This results in long burst noise patterns scattered across multiple blocks. When the decoder rearranges the blocks, the errors manifest as independent random errors or short-length burst errors. The decoder can correct the errors thanks to the error correcting algorithm. The required depth of interleaving depends on the duration of the noise bursts from which the ECC can recover.

Block Diagram:-



Polar Coder Block Diagram

Fig. 1. Polar code Block Diagram

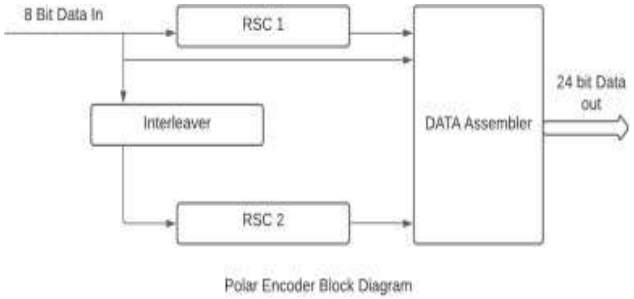


Fig. 2. Polar Encoder Block Diagram

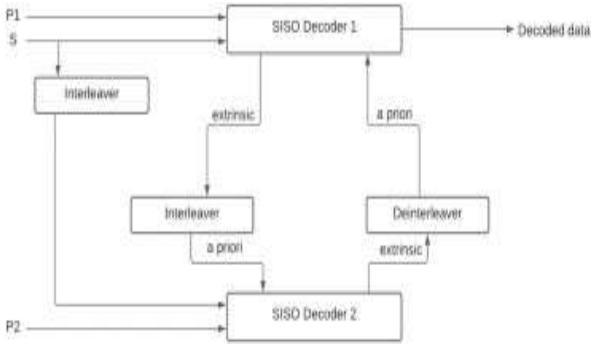


Fig.3. Polar Decoder Block Diagram.

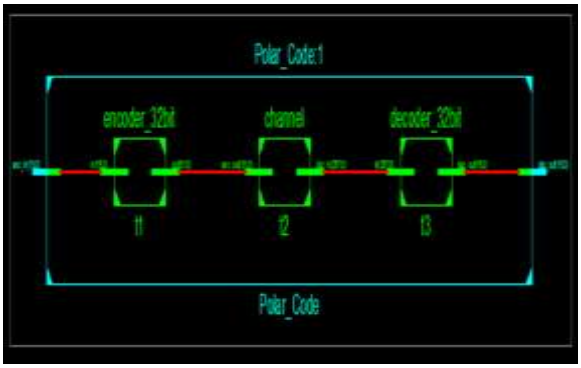


Fig.4 Polar code steps

Fig.5. RTL View of Proposed Model. Table: Comparison of Simulation results

Sr No.	Parameter	Previous Work [1]	Proposed Work
1	Method	Polar Decoder	Polar Encoder & Decoder
2	Area	2.189 mm2	2 mm2
3	Delay	99.94 ns	80.67 ns
4	Power	193.5 mW	125 mW
5	Throughput	11.9 Gbps	12.4 Gbps

Conclusion:-

Xilinx ISE12.2 mimics the polar encoder and decoder that were made with Verilog HDL. XILINX displays technology and RTL diagrams. The synthesis repost gives a lot of information on our proposed design. This example shows how 3GPP uses CRC-Aided Polar coding for information on the New Radio broadcast channel (BCH) and the control channel. It shows how to use QPSK over an AWGN channel for encoding, decoding, rate-matching, and rate-recovery. Under changes to parametric and simulation assumptions, the highlighted performance results for varied coding rates and message lengths follow patterns. As a result, the simulation results show that the suggested polar code outperforms earlier research by a large margin.

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