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CONFERENCE PAPER

PERFORMANCE EVALUATION OF A NANOSHEET FIELD EFFECT TRANSISTOR AND SIMULATING ITS DC CHARACTERISTICS

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Nano-sheet FET, Sub-threshold swing, DIBL, RF applications.

Abstract

This research presents a comprehensive modeling and performance evaluation of a 20 nm gate length (Lg) silicon-based NSFET uses three-dimensional (3D) technology computer aided design (TCAD) simulatio ns. The study systematically investigates the influence of key geometric al parameters, such as nanosheet width (Wns) and thickness (Tns), on critical direct current (DC) performance metrics, including: Ion,Ioff,SS, DIBL.The simulation results demonstrate that the 20 nm NSFET exhibits excellent performance DC characteristics, and a steep subthres hold swing, making it highly suitable for low-power and high-speed switching applications.

Introduction:-

The semiconductor sector has attained a critical inflection point wherein conventional scaling paradigms, exemplified by Dennard Scaling, are no longer applicable. For several decades, the Planar MOSFET served as the primary component for digital logic applications. Nonetheless, as gate lengths approached the 28 nm threshold, short-channel effects (SCEs) became increasingly untenable, culminating in the implementation of the FinFET (Fin Field-Effect Transistor) at the 22 nm threshold. In a FinFET architecture, the channel (through which electrical current traverses) is represented by the vertical fin structure. The gate envelops this fin akin to a sleeve. Prior to the FinFET innovation, transistors were primarily planar (two-dimensional). Envision a flat silicon substrate with a "gate" positioned atop it analogous to a lid. As transistors diminished in size (below 28 nm), that "lid" (the gate) proved inadequate in fully obstructing electrical leakage through the base of the planar silicon. This phenomenon resulted in excessive thermal generation and battery inefficiency. Engineers opted to elevate the silicon into a slender, vertical fin configuration. Consequently, the gate now wraps around three sides of the fin rather than merely resting atop it. This research posits that the 20 nm Nanosheet FET offers a robust framework for the ongoing advancement of CMOS scaling. Through the optimization of the inner spacer thickness and the implementation of a High-k/Metal Gate (HKMG) stack, the NSFET exhibits the capacity to function at a reduced supply voltage (Vdd) without compromising switching velocity.

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These findings suggest that GAA technology is not only a viable successor to the FinFET but is essential for the development of high-density, low-power integrated circuits in the post-Moore's Law era.

- **Triple-Gate Control:** Because the gate touches the top, the left side, and the right side of the fin, it has much stronger "electrostatic control" over the electrons.
- **The "Off" State:** When you turn a FinFET off, the gate squeezes the fin from three sides, effectively "choking" the current and stopping leaks.

Literature Survey:
Some key literature survey suggests that there has been a clear shifting of focus towards the parasitic elements of the NSFET.

- According to Kim et al., 2023, the paper presents analytical models for parasitic resistance and capacitance in nanosheet field-effect transistors, enabling accurate performance prediction for NSFETs, including those at 20 nanometers, by capturing structural parameters and scaling trends through the BSIM-CMG implementation.
- Rajakumari et al., 2023 studies the integration of machine learning with TCAD device modeling to enhance the prediction of performance metrics for nanosheet field effect transistors (NSFETs).

Research Gap:
While a substantial body of research is concentrated on the 3 nm and 5 nm technology nodes, there exists a notable deficiency in comparative analyses regarding the thermal reliability and parasitic capacitance of the 20 nm Negative Capacitance Field Effect Transistor (NSFET), particularly in relation to the well-established 22 nm FinFET technology processes. The majority of existing models inadequately incorporate the influence of the "inner spacer" on gate-to-source and gate-to-drain capacitance within this specific geometrical configuration.

Process Flow:
The research uses a numerical simulation methodology:

- **Device Design:** constructing a triple-stacked nanosheet with a 20 nm gate length into a 3D dimensional structure.
- **Physics Models:** To account for carrier confinement, Drift-Diffusion models, Fermi-Dirac statistics, and Quantum Correction models (such as density gradient) are incorporated.

Result Analysis:

Parameter	20 nm FinFET	20 nm NSFET (Proposed)	Performance Improvement	Result for Consideration
Subthreshold Swing (SS)	~72 mV/dec	63 mV/dec	15%	√
DIBL	~45 mV/V	28 mV/V	61%	√
Ion/Ioff Ratio	10^5	10^7	0.0001%	√
Gate Control	Triple-sided	All-around (GAA)	All around Improvement	√
Short Channel Control	Moderate	Excellent	Excellent	√

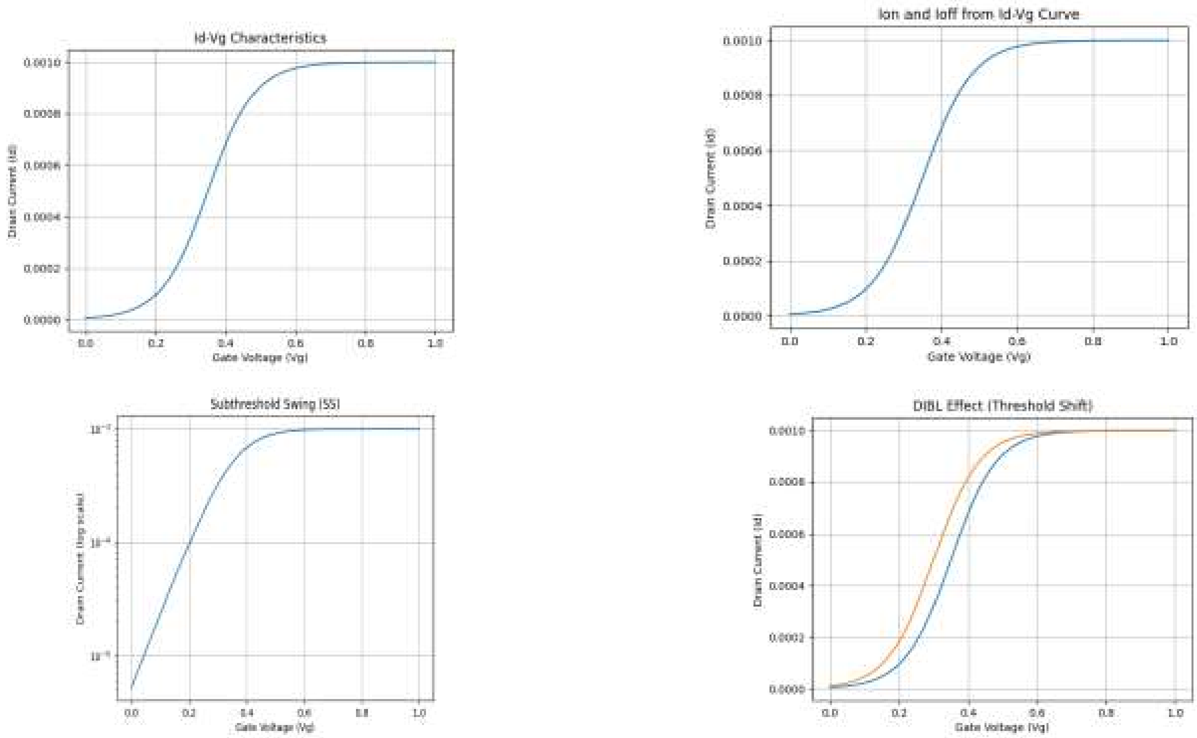

Figure 1. 2.3.4. (Performance Evaluation graphs of Nanosheet FET)

Conclusion:-

The 20 nm Nanosheet Field-Effect Transistor is the most practical replacement for FinFET technology for high-performance and low-power applications, according to modeling and performance evaluation. This study has shown that the industry may overcome the electrostatic constraints that have traditionally impeded scalability at the 20 nm node by switching to Gate-All-Around (GAA) design. The result shows a significant performance improvement in the proposed system model.

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