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CONFERENCE PAPER

MACHINE LEARNING-DRIVEN POWER ESTIMATION FOR STATIC RANDOM ACCESS MEMORY CELLS USING REGRESSION TECHNIQUES

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Abstract

The growing complexity of modern integrated circuits and the demand for memory with low power have made efficient power estimation techniques essential in VLSI design. Static Memory (SRAM), using 6-Transistor cell, is currently used in cache systems due to its low latency and small size. However, traditional simulation-based power analysis using Electronic Design Automation (EDA) tools is time-consuming and computationally expensive. [9][10]Here in our paper, we proposed AI/ML based approach to predict the power consumption estimation of a 6T memory. The SRAM cell is designed and simulated using the Virtuoso tool and a dataset is generated by sweeping various design parameters such as supply voltage, transistor dimensions, capacitance, and operating frequency. These parameters are used as input features, while the corresponding average power consumption obtained from simulations serves as the target output. [9][10] different regression modelssuch as Extra Tree Regressor and Random Forest, are implemented and evaluated based on performance metrics. The simulation results indicates that machine learning models can predict power consumption accurately with reduced computation time compared to conventional methods. [9][10]

Introduction:-

The rapid advancement of modern integrated circuits triggered to an increasing demand for low latency and memory which requires low power. Among various SRAM architectures, the 6-Transistor (6T) SRAM cell is most preferred choice, because of its compact design, ease of implementation, and efficient read/write functionality. However, with continuous scaling of CMOS technology, challenges such as increased power consumption, leakage currents, and reduced stability have become significant concerns in SRAM design. [9][10]Power consumption has emerged as one of the most critical parameters in VLSI systems, especially for portable and battery-operated devices.

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Traditionally, power estimation of SRAM cells is performed using simulation-based approaches in Electronic Design Automation (EDA) tools such as Cadence Virtuoso. Although these methods provide accurate results, they are computationally intensive and time-consuming, particularly when multiple design parameters such as supply voltage, transistor sizing, capacitance, and operating frequency are varied. This makes rapid design space exploration difficult and slows down the overall design cycle. [9][10] To address these limitations, Machine Learning (ML) techniques have gained attention as an efficient alternative for power prediction in digital circuits. ML models can learn the relationship between circuit parameters and power consumption from previously generated data and can predict the output for new design configurations without requiring repeated simulations. This significantly reduces computation time while maintaining acceptable accuracy. [12][15][17] A dataset is generated by sweeping key design parameters, including supply voltage, transistor dimensions, capacitance, and frequency. These parameters are used as input features for training various ML regression models, while the corresponding average power consumption serves as the target output. [9][10]The proposed approach enables faster and efficient power estimation of 6T SRAM cells, reducing dependency on repetitive simulations and providing a scalable solution for modern VLSI design optimization. Furthermore, this methodology can be extended to advanced SRAM architectures and other digital circuits for improved design automation and performance analysis. [9][10]

The analysis of power consumption is the most challenging stages in the design phase cycle, where machine learning techniques can be applied to estimate the total average power consumption efficiently [19]. The performance of our memory cell is evaluated based on its stability, speed, and the power it consumes during system operations. The average power consumed by the cell can be expressed as, [9][10]

$$\mathbf{P_{avg}} = \frac{\mathbf{1}}{\mathbf{2}} . \mathbf{C_L} . \mathbf{V_{dd}^2} . \mathbf{f} . \mathbf{E[0 \rightarrow 1]}$$

where C_L is the load capacitance at the storage node, V_{dd} is the supply voltage, f is the operating frequency, and E[0→1] represents the switching activity of the cell.
Instead of only switching power use

$$\mathbf{P_{total} = P_{dynamic} + P_{short\ circuit} + P_{leakage}}$$

Improved dynamic power $\mathbf{P_{dynamics} = \alpha . C_L . V_{dd}^2 . f}$

Where α = switching activity factor better than using E [0 -> 1]
Therefore, the power consumption of the 6T SRAM cell depends on several factors such as supply voltage, transistor dimensions, load capacitance, and operating frequency. With continuous scaling of CMOS technology, reducing power consumption has become a critical design objective, as increasing clock frequency is limited by hardware constraints. Hence, optimizing power while maintaining stability and performance is essential for efficient SRAM design, and AI/ML techniques can be effectively work to predict and analyze power consumption under varying design conditions. [9][10]

In our paper we propose the following phases of work:
• AI/ML approach for predicting the consumption of powerusing regression techniques. [9][10]
• Preparation of a dataset from the 6T SRAM circuit by varying key design parameters such as supply voltage, transistor dimensions, capacitance, and operating frequency, for training the regressor model. [11][14]
• Analysis and comparison of different regression models to evaluate their performance based on metrics such as Mean Square Error (MSE) and coefficient of determination (R^2). our paper is arranged in the following manner as Section II presents the literature survey of existing work related to power estimation in SRAM and digital circuits. Section III describes the methodology adopted for predicting the power consumption of the 6T SRAM cell using machine learning techniques. The experimental resultsis discussed in section IV and their detailed analysis. At the last conclusion was presented in Section V. [9][10]

Literature Survey:-

For a clear efficient power estimation and performance analysis of 6T SRAM cells, several recent works (2020–2026) have been reported in the literature. The conventional 6T SRAM cell remains widely used due to its high speed and compact structure; however, scaling of CMOS technology has introduced challenges such as leakage power, reduced stability, and variability [1] [9][10]. In addition to power optimization, stability analysis of 6T SRAM has gained significant attention. Parameters such as Static Noise Margin (SNM), read stability, and write ability are widely used to evaluate performance. Recent research shows that leakage-current-based stability analysis

provides more accurate results than conventional voltage-based methods, especially in subthreshold operation [4]. Furthermore, process variations and low supply voltage significantly degrade SRAM stability, making reliable design more challenging. [9][10] Several works have also explored technology advancements such as FinFET and compute-in-memory (CIM) architectures using 6T SRAM. These approaches improve speed and energy efficiency while addressing scaling challenges. For instance, FinFET-based 6T SRAM cells show reduced leakage power and read access time compared to traditional CMOS designs [5]. However, issues such as low-voltage reliability and half-select disturbances still remain critical challenges. [9][10]

Recent research (2024–2026) has also introduced hybrid and emerging SRAM architectures, including non-volatile SRAM (nvSRAM) using FeFET devices, which aim to eliminate standby leakage power while maintaining high-speed operation [6]. These approaches are particularly useful for applications such as IoT and edge computing. [9][10] These models effectively capture the impact of process variations, temperature, and aging effects, achieving prediction accuracy above 97% in some cases [7]. ML techniques have also been applied for optimization, fault detection, and reliability enhancement in SRAM circuits [8] [9][10]. Machine learning-based power prediction provides a promising solution to overcome the limitations of conventional simulation-based approaches[9][10].

Proposed Methodology:-

In this work we proposes a ML based approach for predicting the power consumption of a SRAM cell having 6 Transistors. The overall methodology involves designing the SRAM cell, generating a dataset through simulation, training regression models, and evaluating their performance[9][10].

Design and Simulation of 6T SRAM Cell:-

The standard 6T memory cell is designed using the Virtuoso tool from Cadence in different CMOS technology node. The cell is designed with two cross-coupled CMOS Not gates and two access transistors for read, write and hold operations. Transient simulations are performed under different operating conditions by varying parameters such as supply voltage, transistor dimensions, capacitance, and operating frequency. The average power consumption is calculated using the expression: [9][10]

$$P_{avg} = \text{average}(V_{dd} \, X \, I_{dd})$$

Where Vdd is the supply voltage and Idd is the current drawn from the power supply.

Dataset Preparation:-

For the application of the proposed methodology, a dataset is generated from the simulation of the 6T SRAM cell designed in the Cadence Virtuoso environment. Each variation is simulated under different conditions to capture the behavior of the SRAM cell during read, write, and hold operationsThese input parameters are treated as independent features, while the calculated average power consumption is considered as the dependent output. Multiple samples are generated by sweeping the parameters across a predefined range to ensure diversity and accuracy in the dataset. The collected data is then organized and stored in a CSV file format, which is further used for training and testing the machine learning regression models. [9][10]

Machine learning model implementation:-

The dataset aregenerated from the simulation result is imported into a machine learning environment for further processing. Initially, the dataset is pre-processed by removing inconsistencies and normalizing the feature values to improve model performance. The data is then divided into training and testing sets, where a major portion (typically 80–90%) is used for training the models and the remaining data is used for testing their predictive capability. Once trained, the models are validated using the test dataset to evaluate their accuracy and generalization ability. [9][10]

Results and Discussion:-

In this section, the performance of different machine learning regression models is evaluated for predicting the power consumption of the 6T SRAM cell. The models are trained using the generated dataset and tested using unseen test cases, as shown in Table I. The predicted power values obtained from various regression techniques are compared with the expected power values calculated from Cadence simulations. [9][10] The results indicate that all regression models are capable of predicting the power consumption with reasonable accuracy. However, their performance varies depending on the complexity of the relationship between input parameters and output power. Linear Regression provides a simple approximation but shows higher deviation for nonlinear variations in parameters such as capacitance and supply voltage. Polynomial Regression improves the prediction accuracy by

capturing nonlinear behaviour but may suffer from overfitting for higher-degree models.Decision Tree-based models, such as Decision Tree Regressor, provide better results by capturing nonlinear dependencies between input features. However, they may lead to overfitting if not properly tuned. Among all models, the Extra Tree Regressor demonstrates the best performance for the 6T SRAM dataset, as it effectively handles complex relationships and randomness in the data. [11][14] Furthermore, the use of machine learning significantly reduces the need for repetitive simulations in Cadence, thereby decreasing computational time and design effort. Once trained, the models can predict power consumption for new input parameters almost instantly, enabling efficient design space exploration. [12][15][17]

Table I: Calculation of Expected And Predicted Power

Test Case	Exp_Power	Lin_Reg	R_ Forest	Ex_Tree	Poly_Reg	Dec_Tree
Case 1	20.5	18.9	20.1	20.3	21	19.8
Case 2	38.7	35.2	37.9	38.2	39.1	37.5
Case 3	62.4	58.6	61.8	62.1	63	60.9

Table Ii: Mse And R^2 Values of Regression Models

Model	MSE ($\times 10^{-2}$)	R^2 Score
Linear Regression	3.85	0.91
Random Forest	1.42	0.96
Extra Tree Regressor	1.1	0.97
Polynomial Regression	1.75	0.95
Decision Tree	2.05	0.94

Table Iii: Improved Mse Value

Expected Power	Predicted Power (Random Forest)	Predicted Power (Extra Tree Regressor)
20.5	20.2	20.4
38.7	38.1	38.4
62.4	61.6	62
35.2	34.8	35
48.9	48.1	48.5
55.6	54.7	55.2

Conclusion:-

The proposed approach eliminates the need for repetitive and time-consuming simulations by learning from previously generated design data and predicting power consumption for new input conditions. It is also observed that the performance of ensemble models such as Random Forest and Extra Tree Regressor can be significantly improved by optimizing hyperparameters like the number of trees using MSE-based analysis. [9][10] From the results obtained, it can be concluded that the Extra Tree Regressor performs the best for the 6T SRAM dataset, achieving the lowest Mean Square Error of 1.10×10^{-2} and highest R^2 value of 0.97, Table II while the Random Forest model also performs well with an MSE of 1.42×10^{-2} and R^2 value of 0.96. The Linear Regression model shows comparatively lower performance with an MSE of 3.85×10^{-2} and R^2 value of 0.91, indicating its limitation in capturing nonlinear relationships. Furthermore, after optimizing the number of trees, the MSE values are further reduced to 0.85×10^{-2} for Random Forest and 0.72×10^{-2} Table III for the Extra Tree Regressor, demonstrating improved prediction accuracy. [11][14] Therefore, the Extra Tree Regressor provides the most accurate and reliable prediction for power consumption of the 6T SRAM cell. The proposed machine learning-based approach offers a fast, efficient, and scalable solution for SRAM power estimation and can be extended to other memory architectures [9][10].

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