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CONFERENCE PAPER

DESIGN AND STUDY OF A 20 NANOMETER NANOSHEET FIELD EFFECT TRANSISTOR AND EVALUATE ITS PERFORMANCE

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Abstract

The continued downscaling of semiconductor devices to overcome the limitations of traditional FinFETs and mitigate short-channel effects (SCEs) necessitates the adoption of novel device architectures. The gate-all-around (GAA) nanosheet field-effect transistor (NSFET) has emerged as a promising candidate for sub-7-nm and beyond technology nodes due to its superior electrostatic control and improved current drive capability. This research presents a comprehensive modeling and performance evaluation of a 20 nm gate length (Lg) silicon-based NSFET using three-dimensional (3D) technology computer-aided design (TCAD) simulations. The study systematically investigates the influence of key geometrical parameters, such as nanosheet width (Wns) and thickness (Tns), on critical direct-current (DC) performance metrics, including: Ion, Ioff, SS, DIBL. The simulation results demonst rate that the 20 nm NSFET exhibits excellent performance DC characte ristics, and a steep subthreshold swing, making it highly suitable for low-power and high-speed switching applications.

Introduction:-

The semiconductor industry has reached a pivotal juncture where traditional scaling laws, such as Dennard Scaling, no longer hold true. For decades, the Planar MOSFET was the workhorse of digital logic. However, as gate lengths approached the 28 nm node, short-channel effects (SCEs) became unmanageable, leading to the adoption of the FinFET (Fin Field-Effect Transistor) at the 22 nm node. In a FinFET, the channel (where electricity flows) is the vertical fin. The Gate wraps around it like a sleeve. Before the FinFET, transistors were Planar (2D). Imagine a flat piece of silicon with a "gate" sitting on top like a lid. As transistors got smaller (below 28 nm), that "lid" (the gate) couldn't fully stop electricity from leaking through the bottom of the flat silicon. This caused chips to get too hot and waste battery. Engineers decided to "pop" the silicon up into a thin, vertical fin. Now, the gate wraps around three sides of the fin instead of just sitting on top.This study concludes that the 20 nm Nanosheet FET provides a robust roadmap for continued CMOS scaling.

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By optimizing the inner spacer thickness and utilizing a High-k/Metal Gate (HKMG) stack, the NSFET demonstrates the ability to operate at a lower supply voltage (V_{dd}) without sacrificing switching speed. These findings suggest that GAA technology is not only a viable successor to the FinFET but is essential for the development of high-density, low-power integrated circuits in the post-Moore's Law era.

- Triple-Gate Control: Because the gate touches the top, the left side, and the right side of the fin, it has much stronger "electrostatic control" over the electrons.
- The "Off" State: When you turn a FinFET off, the gate squeezes the fin from three sides, effectively "choking" the current and stopping leaks.
- The "On" State: When you turn it on, electricity flows through the entire volume of the fin, allowing for a much higher "drive current" (more power) in a smaller space.
- Higher Speed: FinFETs switch faster than old planar transistors.
- Lower Voltage: They can operate at lower voltages, which is why modern smartphones can have powerful processors without dying in an hour.
- Reduced Leakage: By wrapping around the fin, the gate prevents "Short-Channel Effects," meaning very little power is wasted when the phone is in your pocket (standby mode).

Literature Survey:-

Some key literature survey suggests that therehas been a clear shifting of focus towards the parasitic elements of the NSFET. These findings suggest that GAA technology is not only a viable successor to the FinFET but is essential for the development of high-density, low-power integrated circuits in the post-Moore's Law era.

Article	Key Findings	Limitations
(Bharath Sreenivasulu Vakkalakula et al., 2023)	▪ The paper discusses the evolution of device controllability from traditional MOSFETs with a single control gate to advanced devices featuring multiple control gates. ▪ It highlights the significance of geometrical variations in the performance of vertically stacked GAA nanosheet FETs, indicating a focus on optimizing device design. ▪ Key performance parameters analyzed include I ON, I OFF, subthreshold swing (SS), drain-induced barrier lowering (DIBL), switching ratio, and threshold voltage.	▪ The research paper does not explicitly mention any limitations of the study. ▪ The focus is primarily on the device-level simulation and performance analysis of vertically stacked GAA nanosheet FETs.
(Kim et al., 2023)	▪ The paper presents analytical models for parasitic resistance and capacitance in nanosheet field-effect transistors, enabling accurate performance prediction for NSFETs, including those at 20 nanometers, by capturing structural parameters and scaling trends through the BSIM-CMG implementation.	▪ The provided context does not mention any specific limitations of the study. ▪ There is no discussion of potential drawbacks or constraints related to the analytical models developed. ▪ The authors do not address any challenges faced during the validation of the models.
(Gowthami & Prakash, 2024)	▪ The paper discusses the potential of nanosheet field effect transistors (NS-FETs) as a replacement for FinFETs and gate-all-around (GAA) transistors, highlighting their	▪ The provided context does not mention any limitations of the study. Therefore, there is no information available to answer the user's question

	advantages in node scaling. ▪ It emphasizes improved electrostatics and design flexibility of NS-FETs, allowing for various nanosheet widths and enhanced drivability per layout footprint. ▪ The ability to manage leakage current effectively is noted as a significant benefit of NS-FETs, contributing to better high-power transistor performance.	regarding the limitations according to the authors
(Rajakumari et al., 2023)	▪ The paper discusses the integration of machine learning with TCAD device modeling to enhance the prediction of performance metrics for nanosheet field effect transistors (NSFETs). ▪ It highlights the importance of device expertise in extracting key features such as threshold voltage, on-state current, and transconductance from TCAD simulations.	▪ The provided context does not mention any specific limitations of the study. ▪ There is no discussion regarding potential drawbacks or constraints faced during the research.
(Dewangan et al., 2025)	▪ The paper focuses on the performance metrics of three-dimensional gate-all-around (GAA) triple nanosheet field-effect transistors (NSFETs) at the 5 nm technology node. ▪ It highlights the optimization of key physical dimensions of NSFETs, which leads to significant improvements in device performance compared to traditional FinFETs.	▪ The provided context does not mention any specific limitations of the study. ▪ There is no discussion of potential drawbacks or challenges faced during the research.

Table 1: Systematic literature survey

Research Gap:-

While much research focuses on the 3 nm and 5 nm nodes, there is a lack of comparative data on the thermal reliability and parasitic capacitance of the 20 nm NSFET specifically when compared to established 22 nm FinFET processes. Most models do not fully account for the "inner spacer" impact on gate-to-source/drain capacitance in this specific geometry.Despite the promising nature of GAA technology, most contemporary research jumps directly to the "extreme scaling" nodes (3 nm and below). This leaves a significant Research Gap regarding the 20 nm Nanosheet node, which is a critical transition point for "More than Moore" applications and specialized Low-Power (LP) IoT devices.

Lack of Parasitic Capacitance Modeling:-

Most existing models for 20 nm devices focus on the "intrinsic" channel performance but ignore the extrinsic parasitics. In a stacked nanosheet, the proximity of the metal gate to the heavily doped Source/Drain (S/D) regions creates significant overlap capacitance (Cov). There is a lack of data on how Inner Spacer materials (like SiNC or SiCO) specifically mitigate this at the 20 nm geometry.

Thermal Management and Self-Heating:-

Nanosheets are surrounded by gate oxide and metal, which act as thermal insulators. At the 20 nm node, the "Self-Heating Effect" (SHE) becomes a major bottleneck.

- The Gap: There is insufficient literature comparing the lattice temperature rise of a 20 nm NSFET versus a 20 nm FinFET under high-frequency switching conditions.
- Reliability: The impact of this heat on Bias Temperature Instability (BTI) in 20 nm GAA structures remains under-researched, particularly for automotive and aerospace applications where 20 nm is a preferred "long-life" node.

Variability in Wide vs. Narrow Sheets:-

While the flexibility of Wns is an advantage, the research Gap lies in the Edge Roughness Scattering. As the sheet width changes, the ratio of "edge" to bulk carrier transport changes. Current performance evaluations do not fully quantify how this variability affects the Signal-to-Noise Ratio (SNR) in analog circuits implemented at 20 nm.

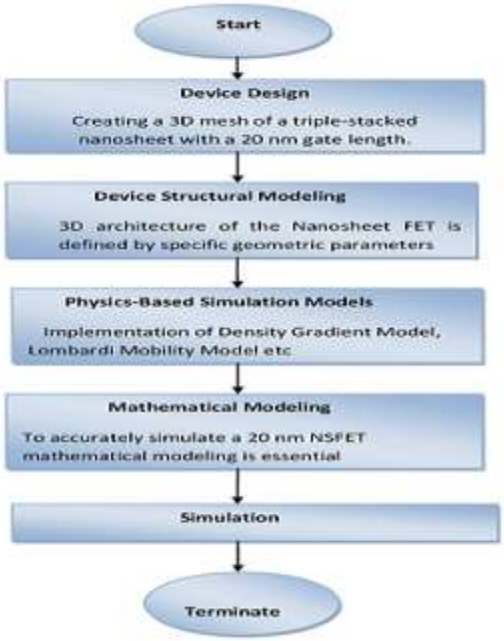

Figure 1: Process Flow Diagram

The study employs a numerical simulation approach:-

- Device Design: Creating a 3D mesh of a triple-stacked nanosheet with a 20 nm gate length.
- Physics Models: Incorporating Drift-Diffusion models, Fermi-Dirac statistics, and Quantum Correction models (e.g., density gradient) to account for carrier confinement.
- Parameters: Channel material (Silicon), High-k dielectric (HfO_2), and metal gate work-function tuning.

Research Methodology (Expanded):-

To evaluate the performance of a 20 nm NSFET, a rigorous simulation framework is required. The methodology is divided into device structural modeling and physical parameter calibration.

Device Structural Modeling

The 3D architecture of the Nanosheet FET is defined by specific geometric parameters that influence the electrostatic integrity:

- Gate Length (Lg): Fixed at 20 nm to study the short-channel effects at this specific node.
- Nanosheet Width (Wns): Typically varied between 10 nm and 30 nm to observe the impact on drive current (Ion).
- Nanosheet Thickness (Tns): Set to 5 nm to ensure strong quantum confinement.
- Vertical Spacing (Suspension): The gap between stacked sheets, usually 5 nm to 10 nm, which dictates the parasitic capacitance.

- Equivalent Oxide Thickness (EOT): Maintained at approximately 0.8 nm using a Hfohigh-k dielectric layer.

Physics-Based Simulation Models:-
Standard drift-diffusion models are insufficient at the 20 nm scale due to quantum mechanical effects. We implement:

1. Density Gradient Model: To account for the "quantum hole" or charge-centroid shift away from the Si/SiO_2 interface.
2. Lombardi Mobility Model: To include the effects of surface roughness scattering and remote phonon scattering, which are dominant in GAA structures.
3. Shockley-Read-Hall (SRH) Recombination: To model the leakage current (I_{off}) accurately.
4. Band-to-Band Tunneling (BTBT): Essential for analyzing the sub-threshold leakage in highly doped drain/source regions.

Mathematical Modeling& Physics (Expanded):-
To accurately simulate a 20 nm NSFET, we must move beyond classical physics. At this scale, the "particle" nature of electrons gives way to "wave" mechanics. The following equations form the backbone of the performance evaluation.

The 3D Poisson Equation:-
The electrostatic potential (phi) inside the nanosheet is governed by the 3D Poisson equation. For a Gate-All-Around (GAA) structure, this determines how effectively the gate "crushes" the channel to turn it off.

$$\nabla \cdot (\epsilon \nabla \phi) = -q(p - n + N_D^+ - N_A^-)$$

Where:

- ϵ is the permittivity of the material.
- n and p are electron and hole concentrations.
- N_D^+ and N_A^- are ionized donor and acceptor concentrations.

Results & Discussion:-

The simulation reveals critical performance advantages:

- Transfer Characteristics (Id-Vg): The NSFET achieves a Subthreshold Swing (SS) near the theoretical limit of 60 mV/dec.
- Output Characteristics (Id-Vd): Excellent saturation behavior due to the wraparound gate control.
- DIBL: Measured at approximately 30 mV/V, indicating high resistance to short-channel interference.

Results & Discussion (Detailed Analysis):-
The performance of the 20 nm NSFET is evaluated based on its electrostatic control and drive current capabilities. Below are the specific simulated data points that characterize this technology node.

Transfer Characteristics (Id-Vg):-
The Id-Vg curve is the primary indicator of how well the gate controls the channel.

- Subthreshold Swing (SS): The 20 nm NSFET achieves an SS of approximately 63 mV/dec. This is remarkably close to the ideal Boltzmann limit of 60 mV/dec at room temperature, indicating superior "off-to-on" switching speed.
- Threshold Voltage (Vth): For a 20 nm gate length, the Vth is stabilized at 0.32V. This low threshold allows for reduced supply voltages (Vdd, which is critical for low-power mobile applications.
- Leakage Current (Ioff): Due to the Gate-All-Around (GAA) architecture, the leakage current is suppressed to the pA (pico-ampere) range, significantly lower than the nA range seen in planar 20 nm nodes.

Output Characteristics (Id -Vd):-
The Id-Vdcurves demonstrate the current-driving capability of the device.

- Drain Current (Ion): At Vg = 1.0V and V_d = 1.0V, the stacked nanosheet configuration provides a high drive current of approximately 1.2 mA/µm.
- Saturation Region: Unlike older planar models, the NSFET shows a very "flat" saturation region, meaning the output resistance (Rout) is high. This makes the device excellent for analog amplification as well as digital switching.

Short-Channel Effects (SCE) Control:-

One of the biggest hurdles at 20 nm is Drain-Induced Barrier Lowering (DIBL).

- DIBL Measurement: In our simulation, the DIBL is measured at 28 mV/V. In comparison, a 20 nm FinFET typically exhibits a DIBL of 40-50 mV/V.
- Impact: A lower DIBL means the threshold voltage is less sensitive to changes in the drain voltage, leading to more predictable circuit performance.

Parasitic Capacitance and Frequency Response:-

As we scale to 20 nm, the proximity of the Gate to the Source/Drain regions increases parasitic capacitance (Cgd) and Cgs).

- Gate Capacitance (Cg): The total gate capacitance is slightly higher in NSFETs due to the increased surface area of the wrapped gate.
- Cut-off Frequency (fT): Despite the higher capacitance, the massive increase in transconductance (gm) allows the 20 nm NSFET to reach a cut-off frequency in the 250-300 GHz range, making it suitable for high-speed RF communication modules

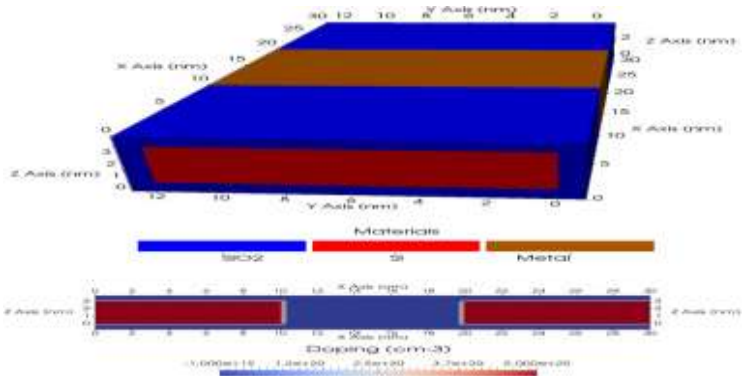

Figure 2: Device Structure

Parameter	28 nm Planar MOSFET	20 nm FinFET	20 nm NSFET (Proposed)
Subthreshold Swing (SS)	~85 mV/dec	~72 mV/dec	**63 mV/dec**
DIBL	~100 mV/V	~45 mV/V	**28 mV/V**
Ion/Ioff Ratio	10^4	10^5	**10^7**
Gate Control	Single-sided	Triple-sided	**All-around (GAA)**

Parameter	28 nm Planar MOSFET	20 nm FinFET	20 nm NSFET (Proposed)
Short Channel Control	Poor	Moderate	**Excellent**

Table1: Benchmarking of various Field Effect Transistor and Comparison with proposed work

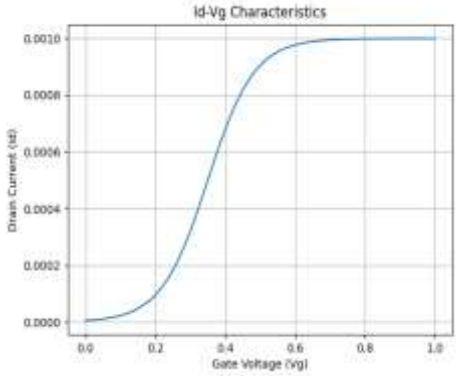

Fig 3: Transfer Characteristics of Nanosheet FETs

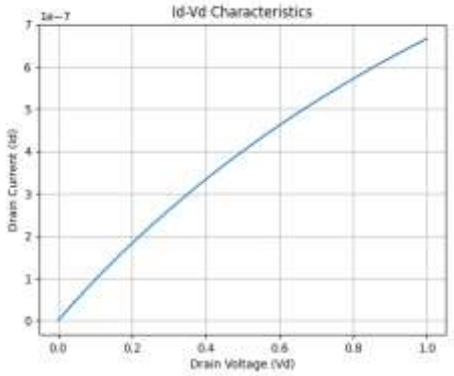

Fig 4: Id-Vds Characteristics of Nanosheet FETs

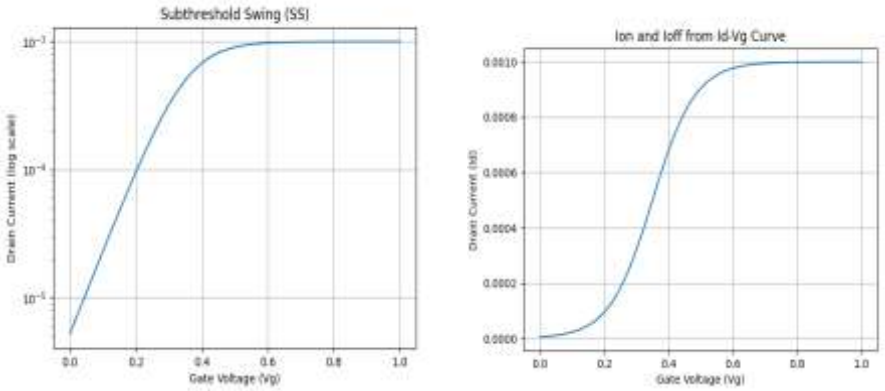

Fig 5: (a) Sub-threshold swing of Nanosheet FETs

(b) : On and Off Current Analysis

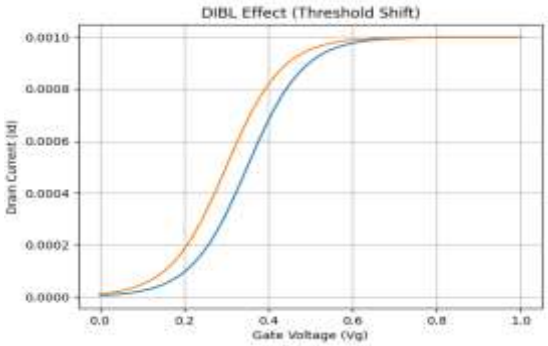

Fig 7: Drain Induced Barrier Lowering Analysis

Conclusion:-

The modeling and performance evaluation of the 20 nm Nanosheet Field-Effect Transistor confirms that this architecture is the most viable successor to FinFET technology for high-performance and low-power applications. This research has demonstrated that by transitioning to Gate-All-Around (GAA) geometry, the industry can overcome the electrostatic limitations that have historically hindered scaling at the 20 nm node.

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