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RESEARCH ARTICLE

FOUR BIT COUNTER USING VERILOG

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Abstract

Hardware Description Language (HDL) is a computer language which is specialized and is used to describe the structure and behavior of digital circuits and systems. HDLs are very important in the designing and development of integrated circuits (ICs) and field-programmable gate arrays (FPGAs). Verilog is a hardware description language (HDL) used to model and design digital circuits. It's widely used in the semiconductor industry for designing and verifying digital systems, especially in the context of Field Programmable Gate Arrays (FPGAs) and Application - Specific Integrated Circuits (ASICs) They allow designers to model, simulate, and synthesize hardware designs, effectively creating a blueprint for the physical hardware. In this paper we presented Four bit Counter which was implemented using Verilog.

Introduction:-

Hardware Description Language (HDL) allows designers to model, simulate, and synthesize hardware designs, effectively creating a blueprint for the physical hardware. HDLs are used to create models of digital circuits, allowing designers to simulate their behavior before physical fabrication. HDL code can be automatically converted into physical implementation (e.g., an IC) using specialized software tools, a process called synthesis. HDLs support various levels of abstraction, from high-level behavioral descriptions to low-level gate-level representations. Popular HDLs include VHDL and Verilog, both of which are IEEE standards.Verilog enables designers to describe the connections and behavior of digital circuits, allowing for a structured and systematic approach to hardware design. It provides a way to create test benches that simulate the behavior of the designed circuit, ensuring its correctness before physical implementation. Verilog code can be translated into actual hardware implementations using synthesis tools, which convert the code into logic gates and their connections.

A synchronous counter is a type of digital counter where all the flip-flops are clocked simultaneously by the same clock signal. This means that all flip-flops in the counter change their state at the same time in response to a clock pulse, unlike asynchronous (ripple) counters where flip-flops are triggered sequentially. An asynchronous counter, also known as a ripple counter, is a type of digital counter where flip-flops are not all triggered by the same clock signal. Instead, the output of one flip-flop serves as the clock input for the next flip-flop in the sequence. This creates a "ripple" effect, where changes in one flip-flop trigger changes in subsequent flip-flops. In an asynchronous counter, only the first flip-flop is clocked by an external clock signal. Subsequent flip-flops are clocked by the output of the preceding flip-flop.

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RTL schematic:-
RTL (Register Transfer Level) schematic provides block diagram representation of a digital circuit at an abstract level. It focuses on how data moves between registers and the logical operations performed on that data, rather than on the detailed implementation using individual logic gates.

Technology schematic:-
Technology schematics are schematics that uses technology-specific or target specific FPGA components like LUTs (Look Up Tables), I/O buffers, carry logic and other technology-specific components.

Device Utilization Summary:-
In the context of Verilog, device utilization summary is a report generated by synthesis and implementation tools (e.g., Xilinx, Intel Quartus Prime, Vivado) after processing a Verilog module for a target ASIC or FPGA. That is device utilization summary is a synthesis report generated after simulating Verilog Test bench module using Behavioural model. A number of devices can be selected to generate synthesis reports. In this paper device 7a100tcsg324-3 is selected to generate synthesis report. This summary provides a detailed breakdown of how the logic described in the Verilog code translates into physical resources available on the chosen device.The device utilization summary includes Slice Logic Utilization, Slice Logic Distribution, IO Utilization, Specific Feature Utilization, Partition Resource Summary, I/O Pin Utilization, and Clock Resources. The device utilization summary is required for Cost Estimation, Design Feasibility, Resource Management and Performance Analysis.

Timing Summary:-
The Timing Summary is a type of synthesis report that provides details about Minimum period, Minimum input arrival time before clock, Maximum output required time after clock, Maximum combinational path delay. In Verilog, timing summaries gives overview of the timing behavior of a Verilog design generated during synthesis or static timing analysis (STA). They illustrate how signals propagate within the circuit, potential timing violations like hold time and setup issues. They summarize the timing characteristics of paths within the Verilog module.

Block Diagram of 4 bit counter:-
A 4-bit up/down counter is a digital circuit that can count up (0 to 15) or down (15 to 0) in binary, using four flip-flops. It typically uses an external input signal to switch between counting up or down. 4-bit Counter is simulated and synthesized by using Verilog. The model has been simulated by writing Verilog code and Verilog test bench code.

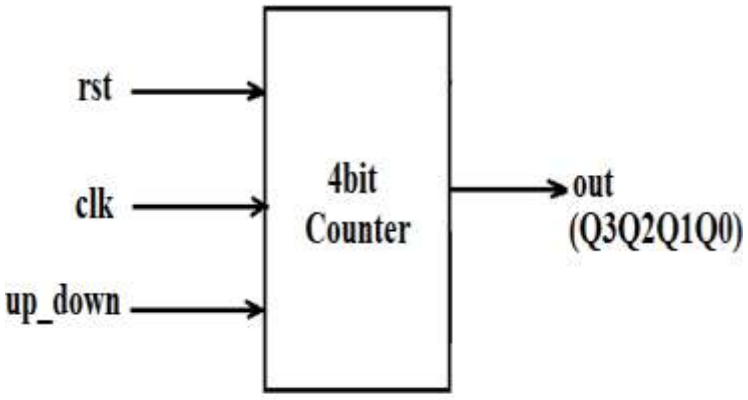


Fig: Block Diagram of 4bit Counter

The working of 4-bit counter is as follows: when the signal reset bit (rst = 1), the counter remains in reset state, all the output bits Q3Q2Q1Q0 = 0000. When rst = 0 and clk = 1(clock input), the counter acts as either up counter / down counter depending on up_down value.

Working of 4 bit up counter:-

When rst = 0, clk = 1(clock input) and up_down = 1 the counter acts as either up counter. In the up counter mode, the counter counts from 1 to 15 that is the output bits changes from Q3Q2Q1Q0 = 0001 to Q3Q2Q1Q0 = 1111.

Truth Table of 4bit up counter:-

rst	clk	up_ down	Q3	Q2	Q1	Q0
1	1	0	0	0	0	0
0	1	1	0	0	0	1
0	1	1	0	0	1	0
0	1	1	0	0	1	1
0	1	1	0	1	0	0
0	1	1	0	1	0	1
0	1	1	0	1	1	0
0	1	1	0	1	1	1
0	1	1	1	0	0	0
0	1	1	1	0	0	1
0	1	1	1	0	1	0
0	1	1	1	0	1	1
0	1	1	1	1	0	0
0	1	1	1	1	0	1
0	1	1	1	1	1	0
0	1	1	1	1	1	1

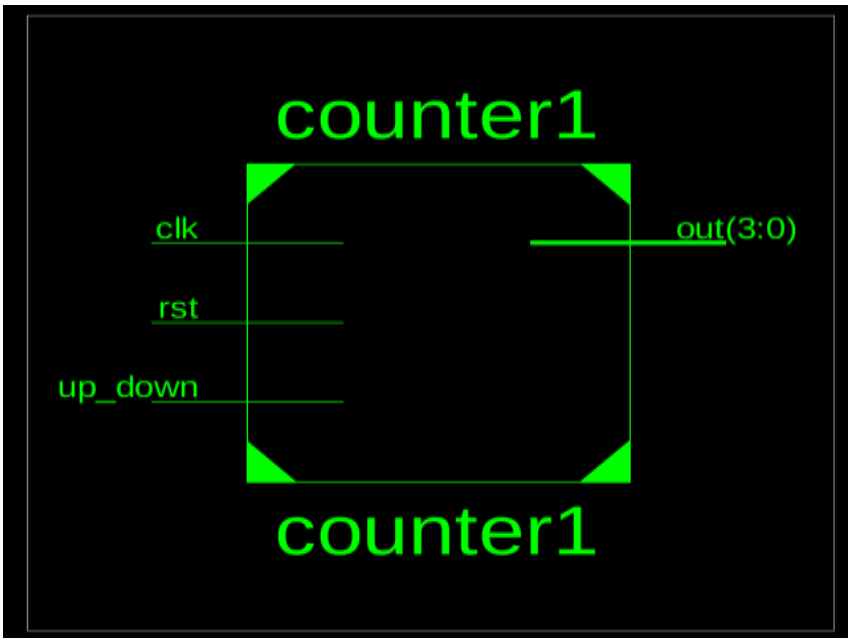
Working of 4 bit down counter:-

When rst = 0, clk = 1(clock input) and up_down = 0 the counter acts as either down counter. In the down counter mode the counter counts from 15 to 0 that is the output bits changes from Q3Q2Q1Q0 = 1111 to Q3Q2Q1Q0 = 0000.

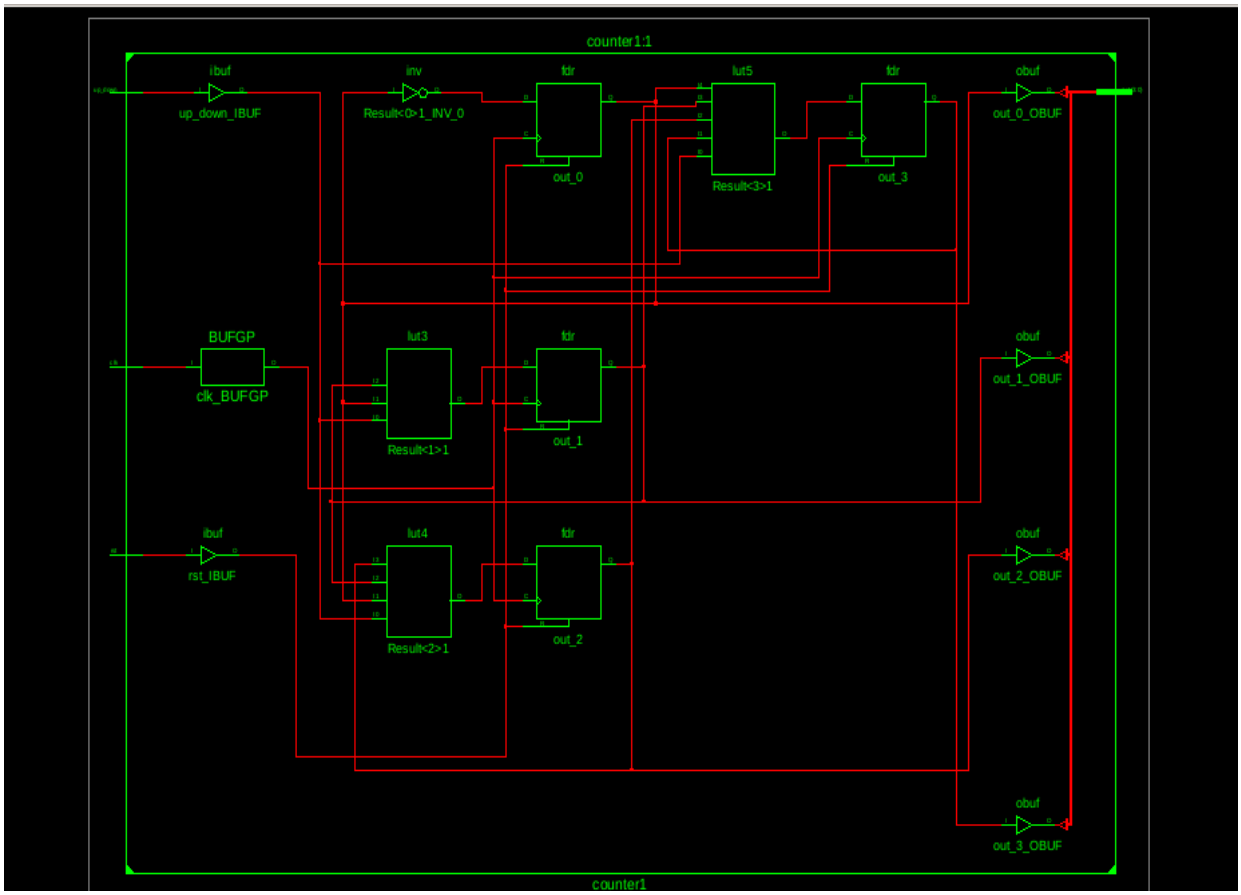
Truth Table of 4bit down counter:-

rst	clk	up_ down	Q3	Q2	Q1	Q0
0	1	0	1	1	1	1
0	1	0	1	1	1	0
0	1	0	1	1	0	1
0	1	0	1	1	0	0
0	1	0	1	0	1	1
0	1	0	1	0	1	0
0	1	0	1	0	0	1
0	1	0	1	0	0	0
0	1	0	0	1	1	1
0	1	0	0	1	1	0
0	1	0	0	1	0	1
0	1	0	0	1	0	0
0	1	0	0	0	1	1
0	1	0	0	0	1	0
0	1	0	0	0	0	1
1	1	0	0	0	0	0

RTL schematic:- 4 bit Counter:-



Technology schematic:- 4 bit Counter:-



Timing Summary:- 4 bit counter:-

Speed Grade: -3

Minimum period	1.059ns (Maximum Frequency: 943.842MHz)
Minimum input arrival time before clock	0.799ns
Maximum output required time after clock	0.659ns
Maximum combinational path delay	No path found

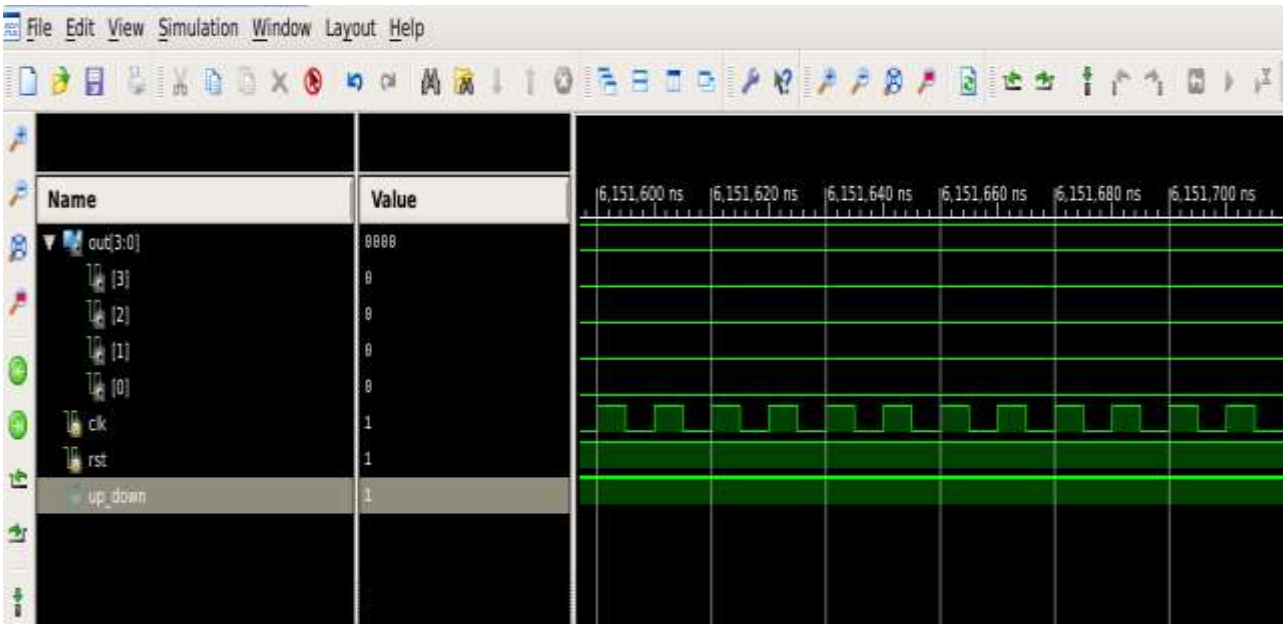
Device utilization summary:- 4 bit counter:-

Slice Logic Utilization:	
Number of Slice Registers:	4 out of 126800 0%
Number of Slice LUTs:	4 out of 63400 0%
Number used as Logic:	4 out of 63400 0%
Slice Logic Distribution:	
Number of LUT Flip Flop pairs used	8
Number with an unused Flip Flop	4 out of 8 50%
Number with an unused LUT	4 out of 8 50%
Number of fully used LUT-FF pairs	0 out of 8 0%
Number of unique control sets	1
IO Utilization:	
Number of IOs	7
Number of bonded IOBs	7 out of 210 3%
Specific Feature Utilization:	
Number of BUFG/BUFGCTRLs	1 out of 32 3%

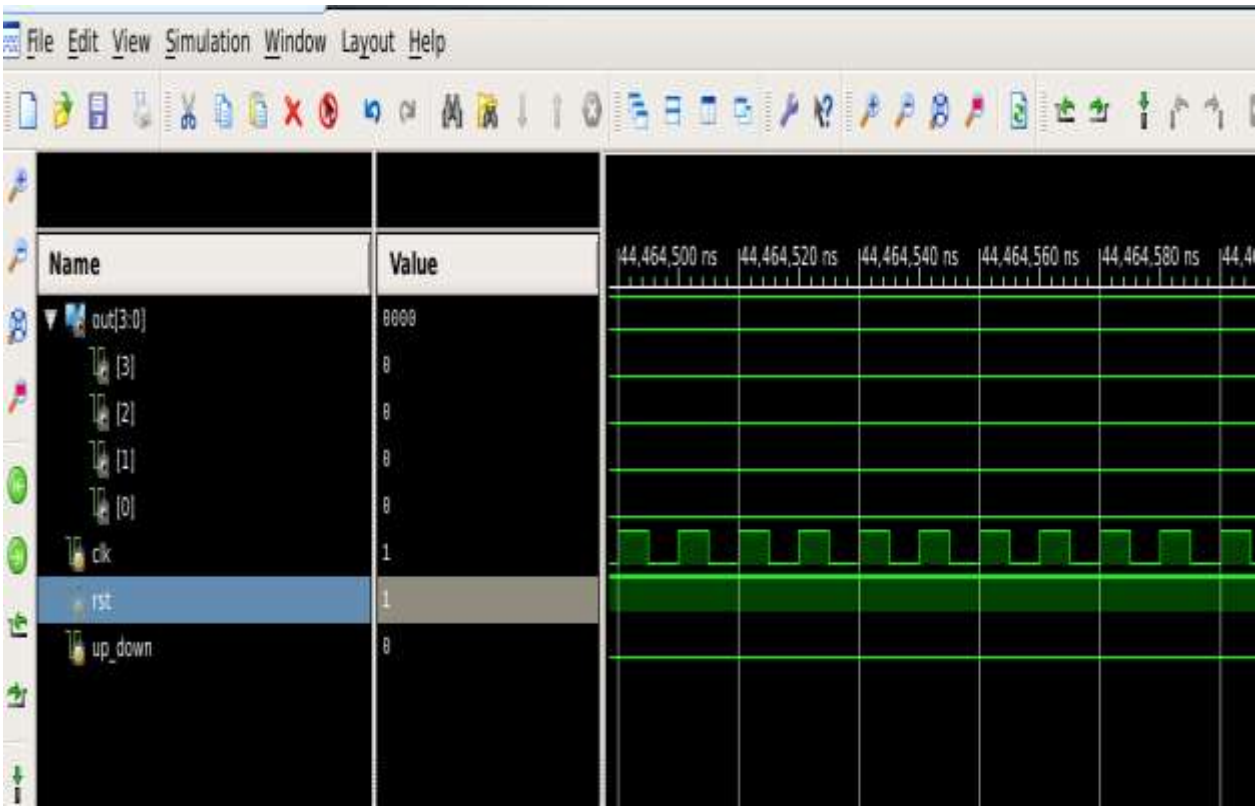
Primitive and Black Box Usage:- 4 bit counter:-

#BELS	4
#INV	1
#LUT3	1
#LUT4	1
#LUT5	1
# FlipFlops/Latches	4
# FDR	4
# Clock	1
# Clock Buffers	1
# BUFGP	1
# IO Buffers	6
# IBUF	2
# OBUF	4

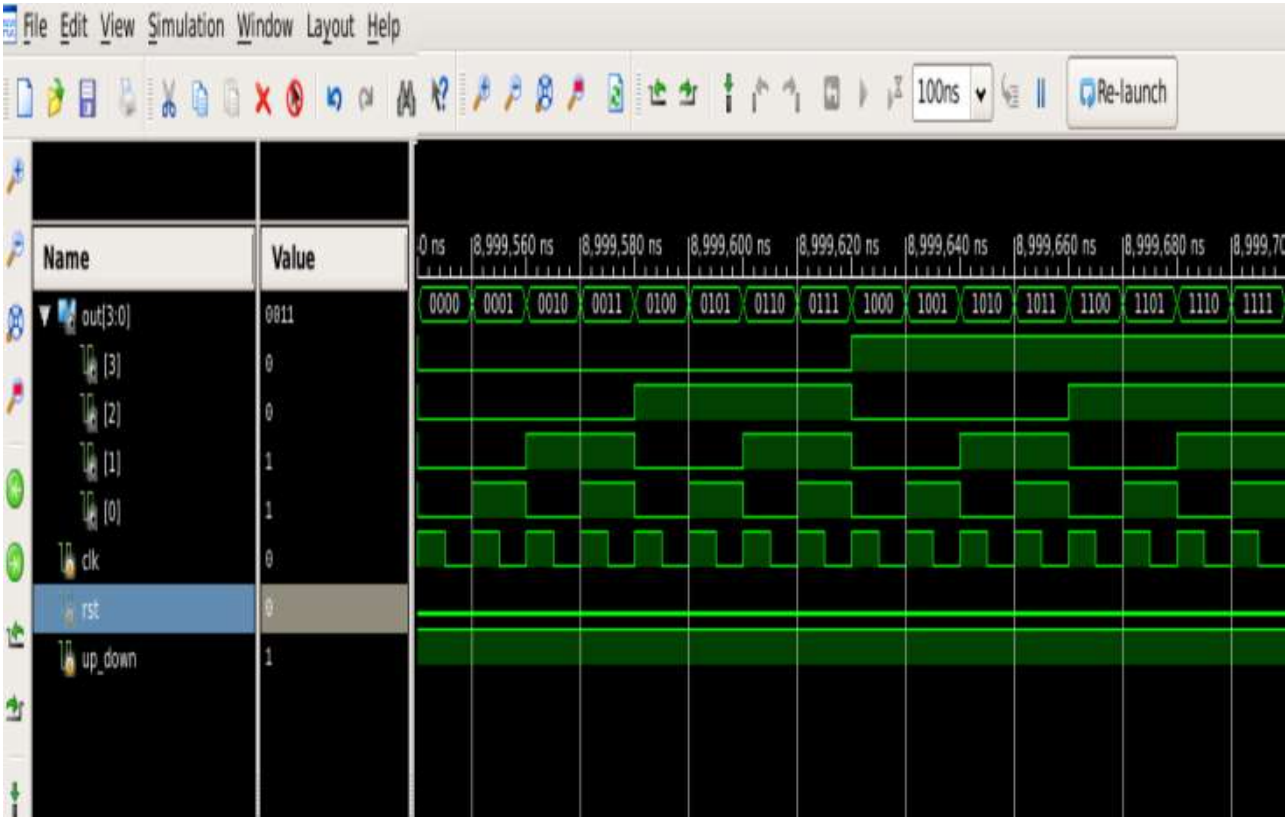
Output waveform:-4 bit up down counter when rst=1 and up_down=1:-



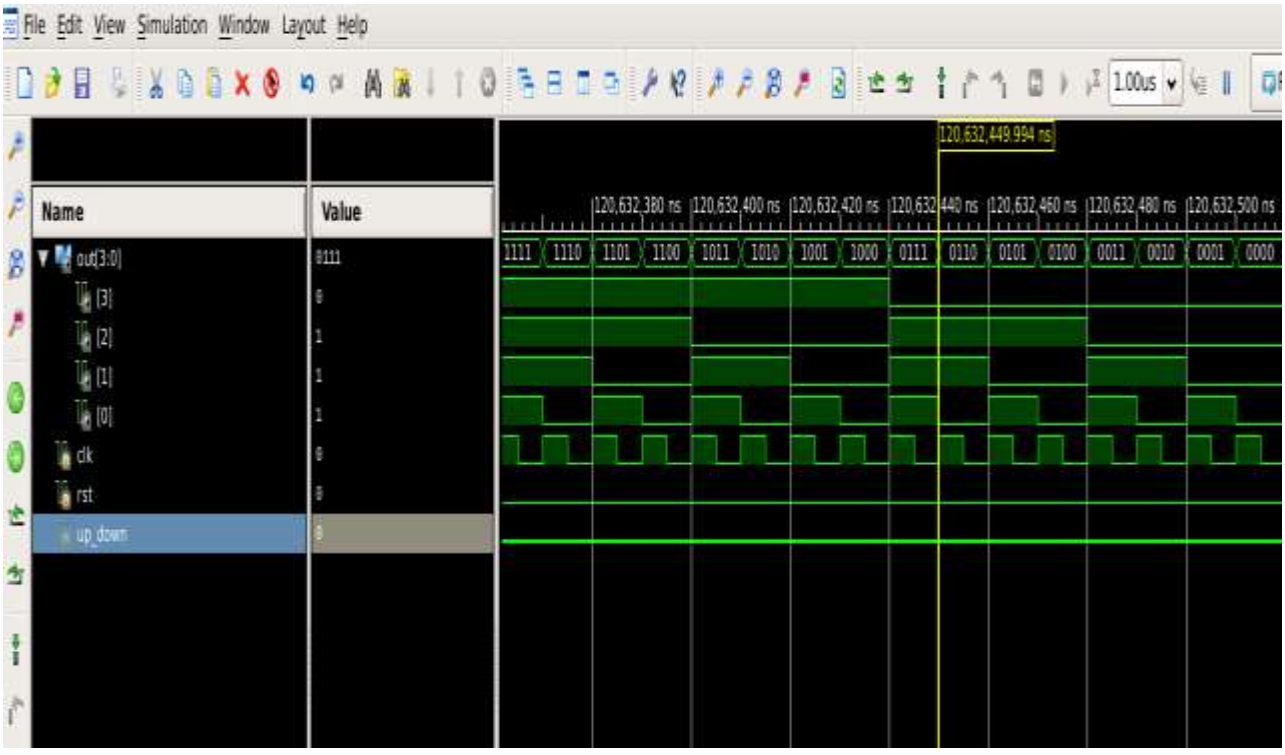
Output waveform:-4 bit up down counter when rst=1 and up_down=0:-



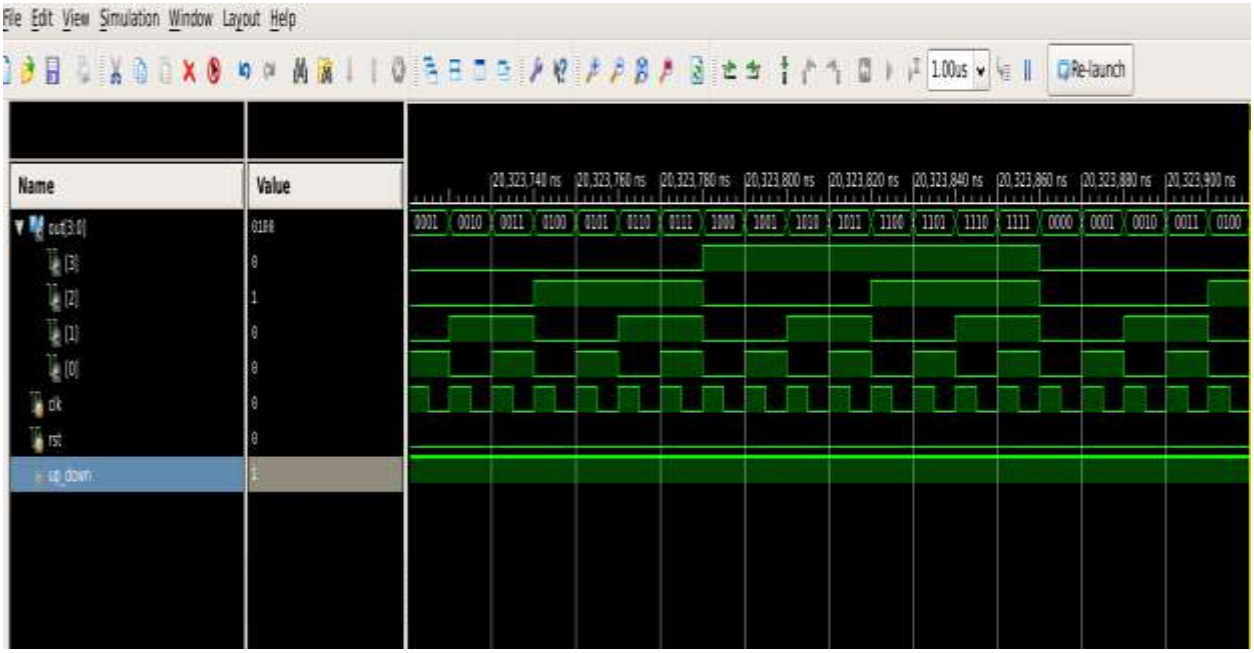
Output waveform:-4 bit up counter:-

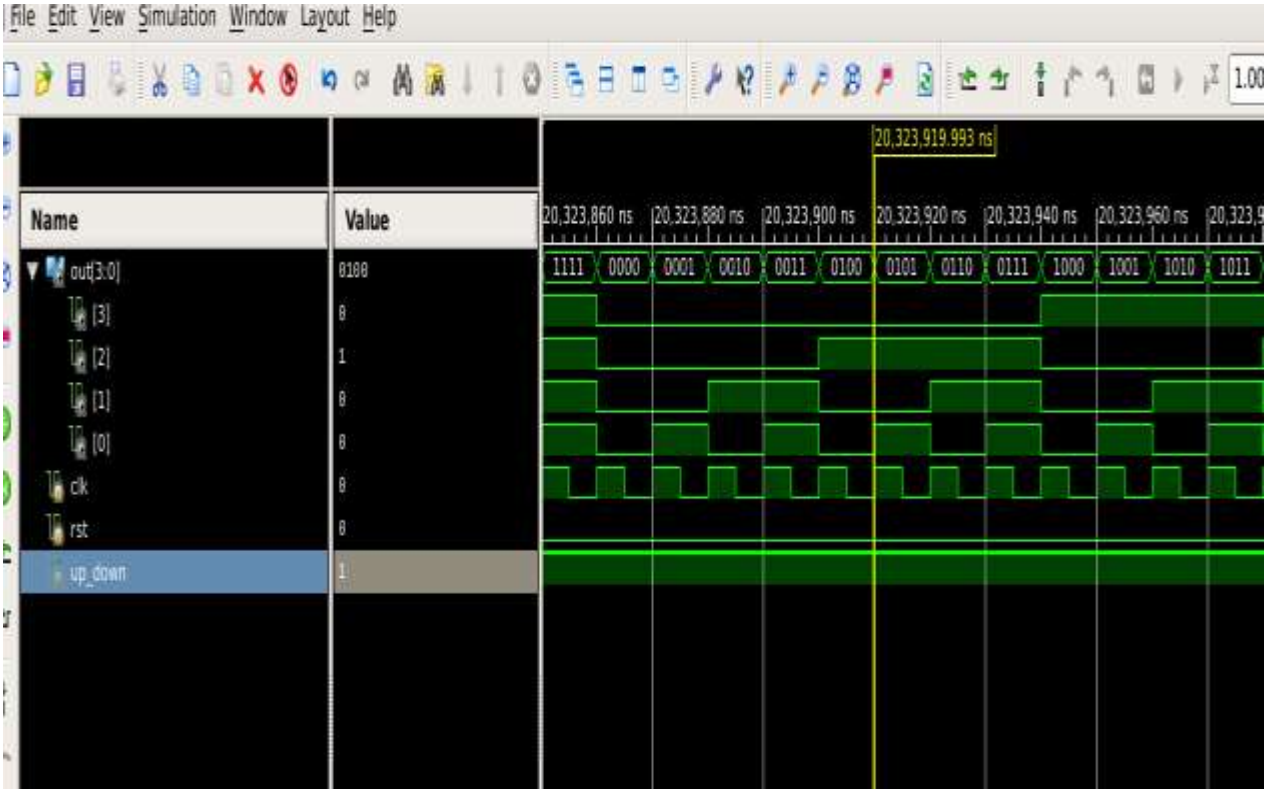


Output waveform:-4 bit down counter:-



Output waveform:-4 bit up down counter:-





Conclusion:-

In this paper 4 bit counter was implemented and simulated and synthesized using Verilog. RTL and Technology schematics were obtained. Device Utilization Summary, Timing Summary and Primitive and Black Box Usage were summarized.

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