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RESEARCH ARTICLE

DESIGN OF A MULTIPLEXER USING DOUBLE BASED NUMBER SYSTEM

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Abstract

This paper presents a novel method for designing a double based multiplexer. This multiplexer is designed using binary number systems as well as ternary number systems. A binary multiplexer selects one out of 2^n number of input lines and passes the information to a single output line whereas a ternary multiplexer selects one out of 3^m number of input lines and passes the information to a single output line. A double based multiplexer selects one out of $2^n \times 3^m$ number of input lines and passes the information to a single output line.

Introduction:-

Multiplexer is a circuit that allows to select a signal that is to be placed on a common output line. A single line is required to pass two or more digital signals, in a large scale digital system, but only one signal should be passed on one line at a time.

Multiplexers are used in various applications such as Communication System, Computer Memory, Telephone Network and Transmission from the Computer System of a Satellite wherein multiple-data need to be transmitted by using single line[14].

It is well known that the binary numerical systems are used in most computers and most people consider about ternary number systems also.This paper discusses the double based number system (2,3) , that is the combination of base 2 and base 3. Multiplexers have been designed using base 2 and base 3 separately, but, no literature could be found on multiplexers developed by considering both bases together. A binary multiplexer selects one out of 2^n number of input lines and ternary multiplexer selects one out of 3^m number of input lines. So here, selecting one out of $2^n \times 3^m$ number of input lines is considered. Combinational circuits such as comparator, half adder and full adder can be designed using multiplexers. So, higher focus should be given to the designing of multiplexers.

Binary And Ternary Logic And Numeral Systems:-

Binary and Ternary Logic:

The two states of binary numeral systems 0 and 1, are called as binary digits. In Boolean logic (two valued logic), 0 is considered as false and 1 as true. The states of ternary numeral systems 0, 1 and 2, are called as ternary digits. Three valued logic is an extension of two valued logic. In three valued logic 1 is considered as True, 0 is considered as False while, 2 is considered as Unknown. Here, Unknown means ‘undefined’, ‘neither’ or both True and False.

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Physical implementation:
Before ternary digit implementation, binary digit implementation should be considered. In logic, bit 1 means 3.3 voltage and 0 means zero voltage whereas in ternary digit implementation bit 1 means 3.3 voltage, 0 means zero voltage and 2 means -3.3 voltage.

Binary And Ternary Logic Gates:-
A logic gate is an idealized or physical device implementing a Boolean function, that is, it performs a logical operation on one or more logic inputs and produces a single logic output[13].

In this multiplexer design, NOT gate, AND gate and OR gate are mainly focused in the case of binary and ternary logic gates. In binary logic gates, the truth value of NOT gate is defined as complement of input, truth value of AND gate is defined as product of inputs of truth values and truth value of OR gate is defined as maximum of inputs of truth values.

In ternary logic gates, truth value of AND gate is defined as maximum of inputs of truth values, truth value of OR gate is defined as minimum of inputs of truth values and truth value of NOT gate is defined as cyclical transformation of input. Since there are several non-cyclical methods to define truth value of NOT gate, according to cyclical and non-cyclical methods, different double based multiplexer can be implemented.

Designing Double Based Multiplexer:-
Binary gates :

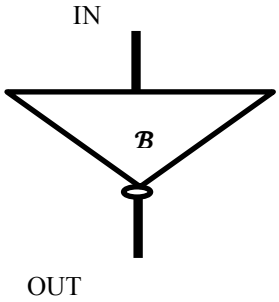

Figure 1:- Binary NOT gate.

In this design binary NOT gate has been used and $\mathcal{B}$ has been used to represent binary NOT gate. Truth values of binary NOT gate is given in table 1.

IN	OUT
A	$\bar{\mathbf{A}}$
0	**1**
1	**0**

Tabel 1:- Truth table for binary NOT gate.

Design of Ternary gates:
Ternary NOT gate has been used here. Also $\mathcal{T}$ has been used to represent ternary gates. In the law of Boolean logic, double negetion law states that, a term that is inverted twice is equal to the variable itself. In other words $\bar{\bar{\mathbf{A}}} \equiv \mathbf{A}$. In this design table 2 shows that, $\widetilde{\mathbf{B}}$ represents cyclical transformation of **B** and also $\widetilde{\widetilde{\mathbf{B}}}$ represents cyclical transformation of $\widetilde{\mathbf{B}}$. So, it can be suggested that, $\widetilde{\widetilde{\widetilde{\mathbf{B}}}} \equiv \mathbf{B}$ in three valued logic. It is a property that was observed here in this design, which is similar to the double negation law in boolean logic.

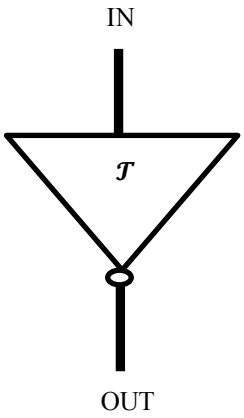

Figure 2:- Ternary NOT gate.

According to cyclic or un-cylic nature of the ternary NOT gate, different double based multiplexers can be desinged. But here cyclical transformation of input system has been taken into account.

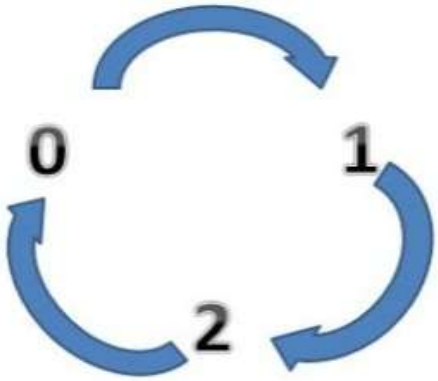

Figure 3:- Cyclical transformation of input system.

Input	Cyclical transformation of		
	B	$\widetilde{B}$	$\widetilde{\widetilde{B}}$
B	$\widetilde{B}$	$\widetilde{\widetilde{B}}$	$\widetilde{\widetilde{\widetilde{B}}}$
0	1	2	0
1	2	0	1
2	0	1	2

Table 2:- Truth table of the ternary NOT gate.

Design of Double Based gates:

Output of the BinaryTernary(Double Based) AND gate is always the maximum of the inputs (Table 3), whereas output of the BinaryTernary(Double Based) OR gate is always the minimum of the inputs (Table 4). Also $\mathcal{BT}$ has been used to represent BinaryTernary(Double Based) gates.

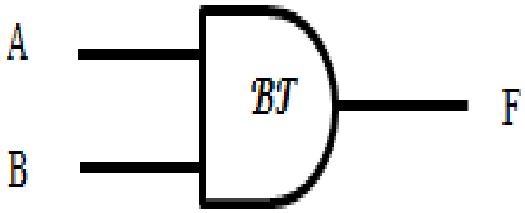

Figure 4:- BinaryTernary AND gate.

A	B	F=Max(A,B)
0	0	0
0	1	1
0	2	2
1	0	1
1	1	1
1	2	2

Table 3:- Truth table of the BinaryTernary AND gate.

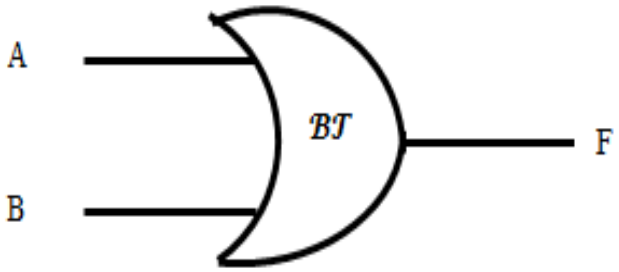

Figure 5:- BinaryTernary OR gate.

A	B	F=Min(A,B)
0	0	0
0	1	0
0	2	0
1	0	0
1	1	1
1	2	1

Table 4:- Truth table of the BinaryTernary OR gate.

Block diagram of $2^n3^m \times 1$ Multiplexer:

The Block diagram given in figure 6 gives an overview of how many number of inputs and selection lines have been considered in designing the 6×1 Multiplexer. Normally, different combinations of selection lines are enabled with different inputs. So, table 5 shows the different values of selection lines and what inputs are enabled in this double based multiplexer.

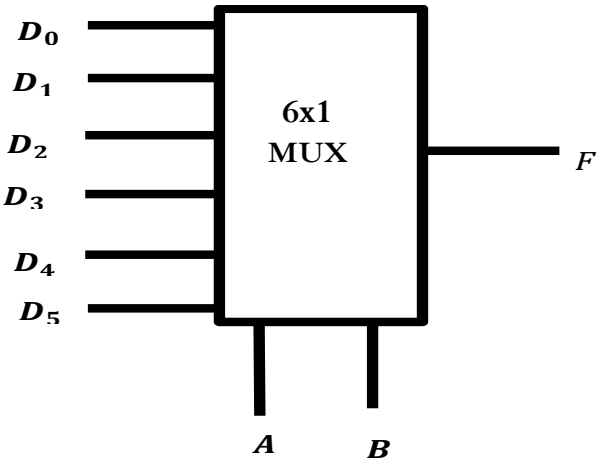

Figure 6:- Block diagram of 6×1 Multiplexer.

A	B	F
0	0	D_0

0	1	D_1
0	2	D_2
1	0	D_3
1	1	D_4
1	2	D_5

Table 5:- Combinations of slection values and corresponding outputs.

Design of 6x1 multiplexer:

In this design, six BinaryTernary(Double Based) AND gates, two ternary NOT gates, one binary NOT gate and one BinaryTernary(Double Based) OR gate have been used. There are six inputs namely D_0,D_1, D_2, D_3, D_4 and D_5. According to the values of two selection lines A and B, one input is enabled.

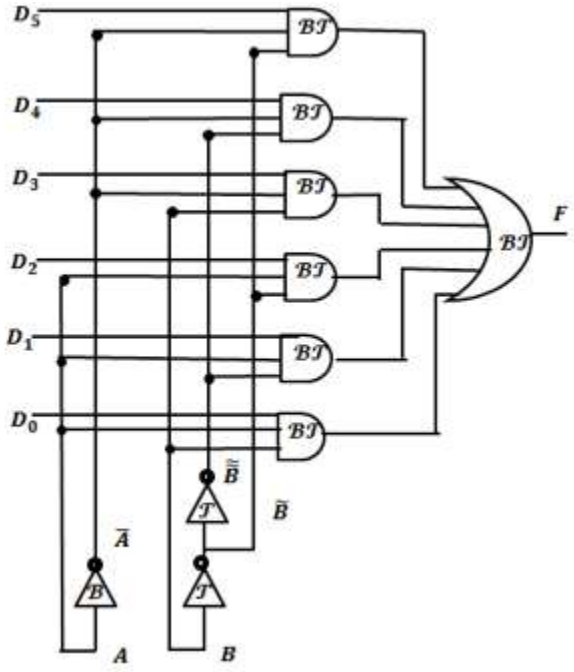

Figure 7:- Design of 6x1 multiplexer.

Conclusion:-

A new design of a device can be implemented by combining two different logics, two valued logic and three valued logic. Reducing power consumption of the device is also important. Also, there is a consistence between law of Boolean logic and suggested law of three valued logic.

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