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RESEARCH ARTICLE

Optimal Design of R-2R Ladder Based DAC with Better Performance Parameter in 45nm CMOS Process

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Abstract

A/D or D/A converter provides interface between analog world and digital processing system, hence used extensively today. Most of the signal in the nature is analog, so digital to analog converter takes digital input from digital processing system and converts it into analog signal. In VLSI design, number of devices increases in system as complexity increases, hence die size required for system increased. As availability of die size becomes more and more critical, optimization of each function in system is important for area consumption. This paper discusses the development and design of 4 bit R2R based D/A converter using MOS transistors as element defining the accuracy. This paper describes the design of a DAC with average speed, linearity and resolution with minimum power dissipation and low area consumption. Also it provides design of an 4 bit DAC with good accuracy by using Microwind 3.5. For Pre Layout simulation 45 nm CMOS process technology has been used.

Introduction

An R-2R Ladder is a simple and reasonable way of performing digital to analog conversion. R-2R ladder consists of repetitive arrangements of precision resistor networks in a ladder-like configuration. It converts a parallel digital input into an analog voltage. Individual digital input (B0, B1, B2, etc.) adds its own weighted contribution to the analog output. This network has some unique and interesting features.

- Easily adaptable to any wanted number of bits
- Uses only two values of resistors which make fabrication and integration process easy.
- Output impedance is equal to R, disregarding of the number of bits, which simplifies filtering and further analog signal processing circuit design[1].

Behavior of switches is non-ideal. Due to this non-ideal behavior, non-linearity exists in converter, there exist a small difference between the ideal analog output "V_{out_ideal}" and the actual analog output "V_{out}". The deviation of "V_{out}" from the ideal value "Vout_ideal" is called the integral non-linearity (INL)[2]. The normalized integral non-linearity can be expressed in "Equation (1.1)"

$$INL_i = \frac{Vout_i - Vout_{ideal}}{\Delta V} \qquad (1.1)$$

Where;
INL_i=the integral non-linearity for input i (Relative error
Between -1 and +1)
$Vout_I$ = the real DAC output for input i
$Vout_{ideal}$ = the ideal DAC output for input i
ΔV= ideal voltage step

The difference between two adjacent analog outputs may be significantly different from the theoretical voltage step. This deviation is called the differential non-linearity (DNL)[2]. The normalized differential non-linearity includes the voltage step ΔV to get the relative error. "Equation (1.2)" expresses the differential non linearity.

$$DNL_i = \frac{Vout_{i+1} - Vout_i - \Delta V}{\Delta V} \qquad (1.2)$$

Where;
DNLi=the differential non-linearity for input i (Relative error, usually between -1 and 1)
Vouti+1=the real DAC output for input i+1
Vouti=the real DAC output for input i

Fig 1 illustrates graphical representation of integral and differential nonlinearities.

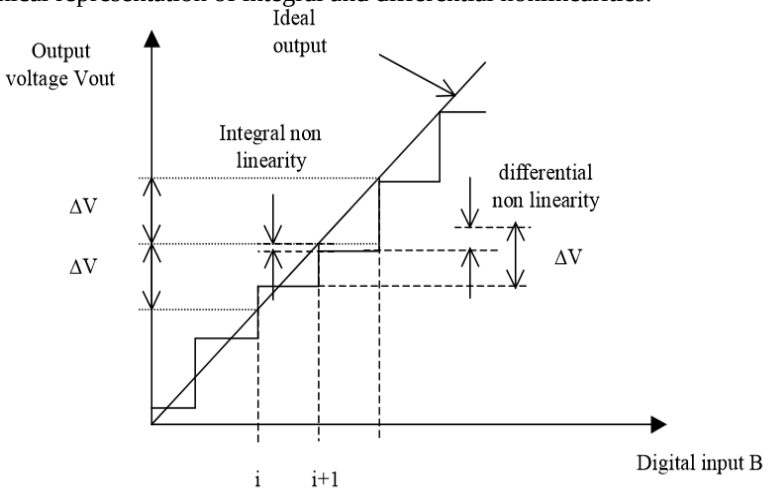

Fig 1: Illustration of integrate and differential non-linearity

Resistance ladder or resistor string converter is basic type of DAC. This DAC consist of simple resistor string of 2^N identical resistors, and binary switch array whose inputs are binary word. The analog output is the voltage division of the resistors flowing via pass switches. The output is connected to at most N switches On and N switches Off[2]. In the following example, the digital-analog converter converts a digital four-bit input (B3, B2, B1, and B0) into an analog value $V_{out.}$. The supply voltage is 1V, which corresponds to the core voltage of the CMOS 45 nm process. The voltage step can be expressed in "Equation (1.3)".

$$\Delta V = \frac{Vdac}{2^N} = \frac{1}{2^4} = 0.0625v \qquad (1.3)$$

For 4-bit R-2R based DAC, value of output voltage will be change in the step of 0.0625v.
In R-2R ladder DAC, the origin of the non-linearity is the resistor ladder design which do not create perfectly regular resistance values

A. R-2R ladder converter

It is not easy to construct a resistor-based DAC with a high resolution, due to the resistance spread, and the needs for 2^N serial resistors. A better choice is the R-2R ladder configuration. Fig 2 shows the schematic layout of 4-bit R-2R ladder base d DAC. This configuration consists of network of resistors alternating in value of R and 2R. For 4 bits DAC, 4 cells based on resistors R and 2R connected in serial. At the right of this network is output voltage "Vout". We used 7 resistors for the 4-bit implementation of the R 2R DAC that is twice less than for the previous R-ladder. The difference is even more significant in the 8-bit circuit, with only 15 resistors, while the simple ladder would require 255 resistors in serial. The digital input (B3,B2 B1 B0) determines whether each cell is switched to ground tied to Vdac through the resistors Each cell's output voltage is a ratio of Vdac because of the voltage division of the ladder network[1]. The final output voltage VOUT depends on the value of B, following the given formula "Equation (1.4)".

The DSCH3.5 program of Microwind is a logic editor and simulator. DSCH3.5 is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH2 provides a user-friendly environment for hierarchical logic design, and simulation with delay analysis, which allows the design and validation of complex logic structures[3].

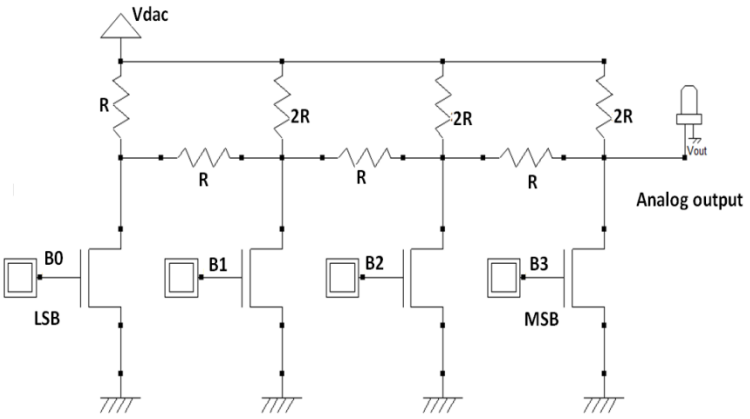

Fig 2: The Schematic layout of 4 bit R-2R ladder DAC

$$V_{out} = V_{dac} \frac{(2^N - B)}{2^N} \qquad (1.4)$$

On this principle, TABLE I gives the value of *VOUT* versus the input code, with *Vdac* equal to 1V.

B3	B2	B1	B0	Vout
0	0	0	0	1
0	0	0	1	0.9375
0	0	1	0	0.875
0	0	1	1	0.8125
0	1	0	0	0.745
0	1	0	1	0.687
0	1	1	0	0.625
0	1	1	1	0.5625
1	0	0	0	0.5
1	0	0	1	0.43
1	0	1	0	0.375
1	0	1	1	0.3125
1	1	0	0	0.25
1	1	0	1	0.1875
1	1	1	0	0.125
1	1	1	1	0.0625

TABLE I. VOUT OF THE 4 BITS R-2R DAC vs. INPUT CODE

In VLSI design, as complexity increases, number of devices in the system increases, and hence, an increase in the die size required for that system. As the die space available becomes more and more critical, each function in the system need to be optimized for area consumption. The DAC is optimized for large integrated circuit systems where possibly dozens of such DAC would be employed for the purpose of digitally controlled analog circuit calibration[4].

Physical layout & consideration

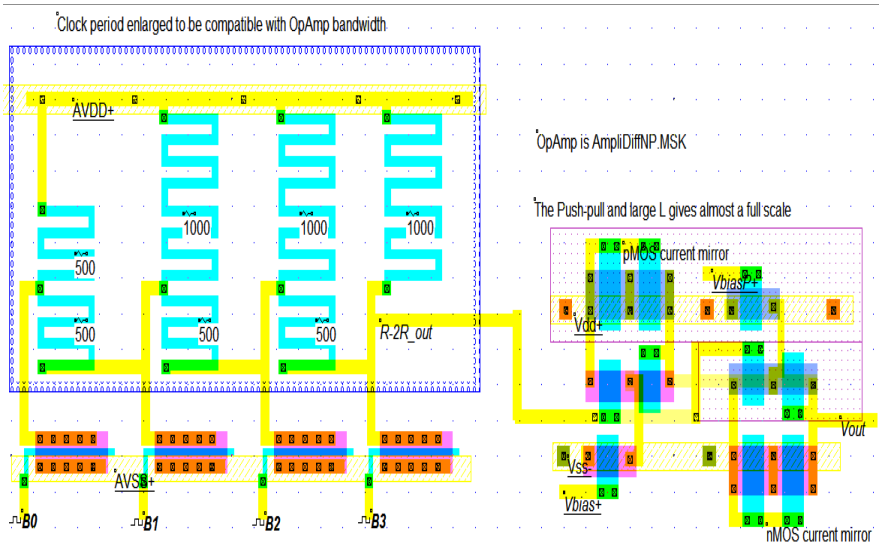

Fig.3: Physical layout of four-bit 2-2R digital to analog converter

The resolution of the R-2R DAC is linked with the accuracy of the resistors and of the resistance of the switches which must be negligible to avoid a voltage drop and associated non-linearity. It is important to implement a low *Ron* switch (Large width, minimum length), together with large resistors. The elementary resistor pattern has a fixed value of 500 ohm.

A long path of poly silicon between VDD and VSS may give intermediate voltage references required for the DAC circuit. Unfortunately, the poly silicon has a low resistance due to a surface deposit of metal, called salicidation. The resistance per square is quite small (Around 5Ohm per square) due to this thin metal coat. The physical layout of R-2R ladder DAC is as shown in Fig 3.

Simulation results

We provide the digital input from 0000 to 1111 given to this converter. After providing input, we have got the simulation result as shown in TABLE II.

The simulation result shows a regular decrease of the output voltage V_{out}. The value of V_{out} for input B=1111 is higher than the predicted 0.0625V, because of the R_{on} of MOS devices is not negligible. This non-linearity may be reformed by expanding the MOS switch and increasing the length of the serpentine resistor. Alternately, a dummy switch, whose pass resistance is half R_{on}, may be inserted inside each cell in serial with R.

Digital Inputs				**Analog Output Values**		**INL**	**DNL**
B 3	***B 2***	***B 1***	***B 0***	***Theoretical***	***Practical***		
0	0	0	0	1	1	0	-0.1425
0	0	0	1	0.9325	0.92	-0.0125	-0.1425
0	0	1	0	0.875	0.84	-0.035	-0.1125
0	0	1	1	0.8125	0.79	-0.0225	-0.1525
0	1	0	0	0.75	0.70	-0.05	-0.1225
0	1	0	1	0.6875	0.64	-0.0475	-0.1025
0	1	1	0	0.625	0.60	-0.025	-0.1025
0	1	1	1	0.5625	0.56	-0.0225	-0.1825
1	0	0	0	0.500	0.44	-0.06	-0.1025
1	0	0	1	0.4375	0.40	-0.0375	-0.1125
1	0	1	0	0.375	0.35	-0.025	-0.0825
1	0	1	1	0.3125	0.33	0.0175	-0.1025
1	1	0	0	0.25	0.29	0.04	-0.0925
1	1	0	1	0.1875	0.26	0.0725	-0.0825
1	1	1	0	0.125	0.24	0.115	-0.0725
1	1	1	1	0.0625	0.23	0.1675	

TABLE II. READINGS OF R-2R DAC CIRCUIT FOR ALL POSSIBLE INPUTS.

Fig 4 shows the simulation result of R-2R ladder DAC for input (B3, B2, B1,B0) from 1111 to 0000. Fig 5 shows the AC analysis of DAC. Here, we can observe constant output frequency response of DAC output voltage, which is constant at 63 MHz, with no jitter after few startup cycles.

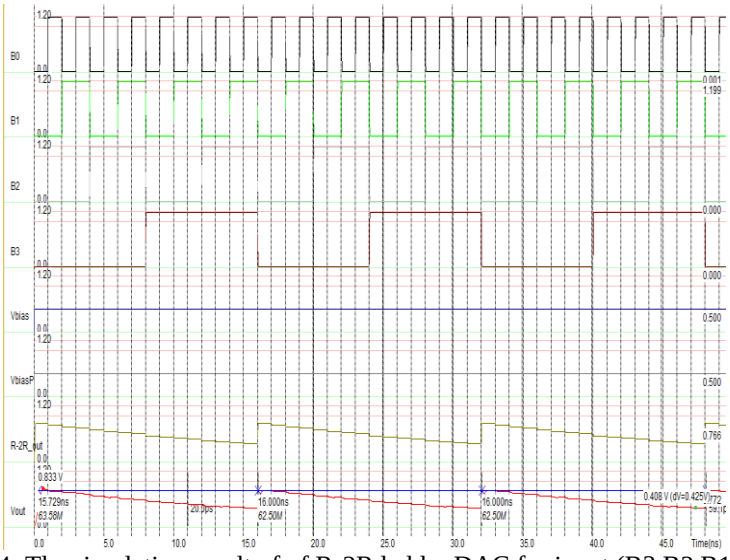

Fig. 4: The simulation result of of R-2R ladder DAC for input (B3,B2,B1,B0)

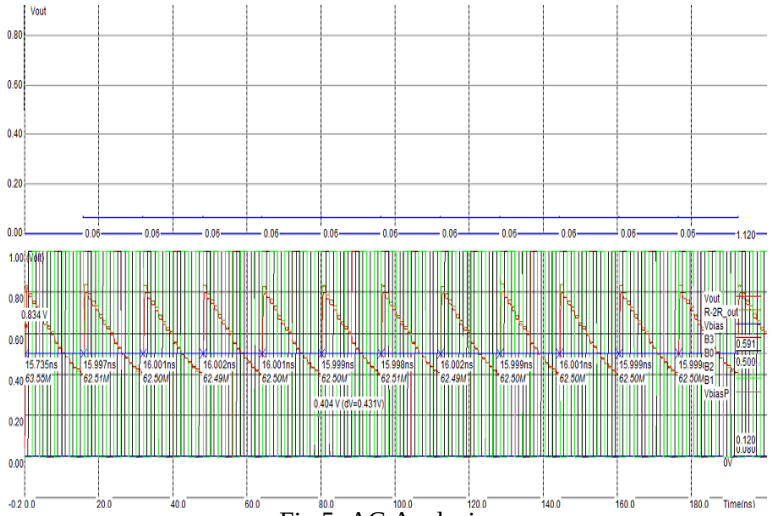

Fig.5: AC Analysis

Conclusion

With an increasing trend to a system-on-chip, DAC has to be implemented in a low-voltage submicron CMOS technology in order to achieve low manufacturing cost while being able to integrate with other circuits. Experiments were performed on 4 bit R2R DAC, the accuracy of theoretical and Microwind 3.5 experimented scenarios are expressed in previous chapter.
In this paper 4-bit R-2R DAC simulated in submicron technology, the average power is found to be 2.050 mw with very low area of 24.0µm2 with excellent INL and DNL. From this results could conclude that conversion is performed for all combination successfully and a low-power 4-bit R-2R DAC in a 45 nm CMOS process with a 1 V supply voltage is designed.

References

[1] Tutorial: "Digital to Analog Conversion – The R-2R DAC", Alan Wolke, May2013.

[2] Anshul Agarwal, "Design of Low Power 8-Bit Digital-to-Analog Converter with Good Voltage-Stability", Center for VLSI and Embedded System Technologies International Institute of Information Technology Hyderabad, India May 2013.

[3] Etienne SICARD, CHEN Xi, "A PC- based educational tool for CMOS Integrated Circuit Design", INSA, Department of Electrical & Computer Engineering Av de Rangueil

[4] Brandon Greenley, Raymond Veith, Dong-Young Chang, and Un-Ku Moon, "A Low- Voltage 10-Bit CMOS DAC in 0.01-mm2 Die Area", IEEE TRANSACTIONS ON CIRCUIT AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 52, NO. 5, MAY 2005

[5] "CMOS Integrated Analog To Digital & Digital To Analog Converters",2nd ed.,Rudy Van deplassche.