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AN EXPERIMENTAL STUDY OF LOW-POWER HIGH-SPEED AND COMPACT TERNARY VLSI CIRCUIT DESIGNS WITH SPECIAL REFERENCE TO CARBON NANOTUBE FIELD EFFECT TRANSISTORS

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ABSTRACT

Carbon nanotube field effect transistor (CNTFET) demonstrates extraordinary guarantees as extension to Silicon MOSFET for building superior and low power VLSI circuit. Three-esteemed (ternary) rationale is a promising contrasting option to conventional binary rationale for achieving straightforwardness and vitality effectiveness in present day advanced design. Ternary rationale has an exquisite relationship with CNTFET on the grounds that the most ideal approach to design ternary circuit is the multiplethreshold strategy and wanted edge voltage can be effortlessly accomplished by using unique diameter of CNT in CNTFET gadget.

This postulation creates designs of ternary math and rationale unit (TALU) and substance addressable memory cell utilizing CNTFETs. Initial, 2-bit hardware advanced ternary ALU (HO-TALU) is introduced. 2-bit HO-TALU gets minimization in required hardware at both design and additionally at circuit level. At engineering level, HO-TALU has another addersubtractor (AS) module which performs both expansion and subtraction operations utilizing an snake module just with the assistance of multiplexers. Along these lines, it disposes of a subtractor module from the regular engineering. At circuit level, HO-TALU limits ternary capacity articulations and uses binary gates alongside ternary entryways in acknowledgment of useful modules: AS, multiplier, comparator and select OR. AS module has a minor misfortune in powerdelay item (PDP) however multiplier, comparator and selective OR modules demonstrate moved forward PDP. As an outcome, HO-TALU gets critical diminishment in gadget number with insignificantly increment in PDP for expansion and subtraction operations just in correlation with CNTFET-based ternary designs accessible in the literature. Design of 2-bit HO-TALU is altered to build up a 2-bit HO-TALU cut which could be effortlessly fell to develop N-bit HO-TALU.

Ternary full viper (TFA) which is a fundamental sub-square of AS module, is changed utilizing distinctive circuit procedures to enhance its productivity as far as PDP. Three new designs of TFA are introduced. The main TFA design named as rapid TFA (HS-TFA) utilizes a symmetric draw up and pull-down networks alongside a resistive voltage divider as its fundamental part, which is designed utilizing transistors. Contrasted with as of late created TFA accessible in literature, HS-TFA gets enhanced speed however high power scattering. So as to decrease

control utilization, a moment TFA named as low power TFA (LP-TFA) is proposed. LP-TFA makes utilization of complimentary pass transistor rationale style and accomplishes low power utilization with peripheral reduction in PDP. To get enhanced PDP further, a third TFA is actualized in powerful rationale. This TFA is named as unique TFA (DTFA) which utilizes a manager designed for ternary esteems keeping in mind the end goal to ease charge sharing issue. The acknowledgment of each of the three TFA takes the upsides of inborn binary nature (0 and 1) of info convey prompting effortlessness in designs.

Next, another design of comparator module of 2-bit HO-TALU is displayed. Initial, 1-bit comparator is created utilizing pass transistor rationale with lessened number of stages in basic postpone way. At that point, 1-bit design is used to make 2-bit and N-bit comparator where a static binary tree arrangement is utilized to rectify the voltage levels. The proposed 2-bit comparator accomplishes better PDP in correlation with that of accessible partners. This comparator, HSTFA also, DTFA have high driving ability. Also, all new TFAs and 2-bit comparator are less touchy to voltage and temperature varieties concerning existing designs. Next, design of 2-bit control improved ternary ALU (PO-TALU) utilizing CNTFETs is exhibited. 2-bit PO-TALU useful modules: snake subtractor-selective OR (ASE) and multiplier, are designed utilizing new corresponding CNTFET-based binary computational unit and a low multifaceted nature encoder. ASE disposes of select OR and subtractor modules from the traditional engineering. Multiplier utilizes another productive convey include (CA) obstruct in place of ternary half viper. Subsequently, PO-TALU design gets critical upgrades in terms of energy and power-defer item with gadget check contrasted with existing designs. Design of 2-bit PO-TALU cut is demonstrated so parallel N-bit PO-TALU can be built with N/2 cuts associated in course. Further, expanded fascination for data transfer capacity hungry constant applications like web has raised an interest for rapid CAM circuits to perform table query undertaking. Binary CAM (BCAM) and ternary CAM (TCAM) cells designed in view of low capacitance seek rationale are displayed in CNTFET innovation. Another three-esteemed CAM (3CAM) cell is too displayed. This cell utilizes CNTFETs with two distinctive limit voltages in usage of low capacitance look arrange which prompts a quick and reduced CAM design with regard to CNTFET based 3CAM cell as of late distributed in the literature.

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Chapter 1

Introduction

1.1 Background

Since the presentation of coordinated circuits (ICs) in 1952 and the realization of the first IC at Texas Instruments in 1958, the most recent five decades saw a phenomenal development of Silicon (Si) based microelectronics industry. Fast advancements in this industry are accomplished chiefly because of constant scaling or miniaturization of all hardware parts (uninvolved and dynamic) coordinated on the ICs. IC miniaturization systems supported the scaling of complementary metal oxide semiconductor (CMOS) gadgets and metallic interconnects that utilized for the association of gadget terminals with control supply voltage. Miniaturization in IC innovation makes less testing necessities at framework level, accomplishes noteworthy cost reserve funds and quicker changing, and prompts minimal, low power furthermore, exceedingly solid designs. As an outcome, it gives speedier and enhanced ICs to high definition advanced TV, computerized beneficiary, DSP, rapid microprocessor, correspondence, business exchanges, activity control, space direction, therapeutic treatment, climate checking, web, and numerous other business, modern, and logical ventures. Further, as per Moore's law, the quantity of transistors that can be fabricated on a solitary chip is relied upon to develop exponentially with time. This forecast ended up being valid as delineated in Figure 1.1. Figure 1.1 plots the decrement in number of transistors coordinated on a solitary microprocessor chip as a capacity of time. As can be watched, reconciliation thickness pairs in at regular intervals. To meet the IC thickness anticipated by Moore's law, innovation scaling has been sought after forcefully until today since 1970s. The gate length of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is downsized by a factor of 0.7 in at regular intervals, as appeared in Figure 1.1. Since 2006, at 65 nm innovation hub the entryway length of a MOSFET has landed at profound sub-micron/nano run. Today, innovation hub is 20 nm, and 14 nm has been normal as highlight estimate sooner rather than later.

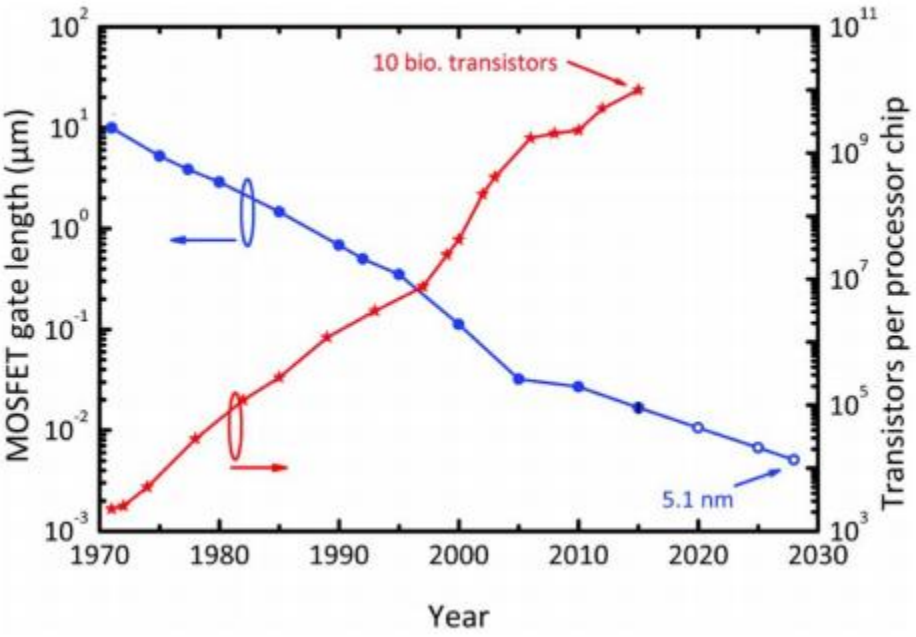


Figure 1.1: Evolution of MOSFET gate length (filled blue circles and open blue circles for ITR targets) and integration complexity of microprocessor chip (red stars), as a function of time.

Further, downsizing the entryway length of CMOS innovation in nano ranges brings about different basic difficulties and unwavering quality issues. One of the issues is expanded leakage current which happens because of different quantum mechanical tunneling including band-to-band tunneling, coordinate gate oxide tunneling, and source to deplete tunneling [9]. Different issues are vast process varieties, the effects of gem mis arrangements, the arbitrariness of discrete doping, and addition of interface scatterings since the mean free way of electrons ends up plainly equivalent to part measurements. These gadget level effects cause the current-voltage (I-V) qualities to be generously unique in relation to very much tempered MOSFET. Subsequently, analysts have significant concerns in regards to additionally enhancing gadget execution by downsizing the component size of MOSFET. Plus, circuit level effects for example, short channel effects, augment in the resistance of metallic on-chip interconnects furthermore, control dissipation will clearly lessen the appropriateness of MOSFET for cutting edge applications so as to come.

Scientists grew twofold entryway MOSFETs and FinFET/tri-gate gadgets to decrease short channel effects. In these gadgets, entryway is put on two/three sides of the channel, which brings about better control on the direct and significant diminishment in deplete to source sub-edge leakage current.

Analysts additionally have started the investigation of new gadgets and direct material in sub- 10 nm innovation node, which could be the conceivable other options to Si-CMOS. In light of ITRS , a portion of the developing gadgets which have the abilities to supplant InTechnology in post Si time are nanowire field effect transistor (NWFET), III-V compound semiconductor field effect transistor, grapheme field effect transistor , and carbon nanotube field effect transistor (CNTFET). NWFET utilizes a semiconducting nanowire having diameter around 0.5 nm as a channel material. This nanowire can be produced using Si, germanium, III-V, In2O3, ZnO or SiC semiconductors. The schematic perspective of silicon based NWFET is appeared in Figure 1.2 . The principle points of interest offered by NWFET because of utilization of little diameter are 1-D conduction and limited short channel effects. The fundamental test confronted by this gadget is creation of diffused P-N intersections. For this, present innovation uses metal deplete source intersections which result in am bipolar conduction yet delivers a huge OFF state current.

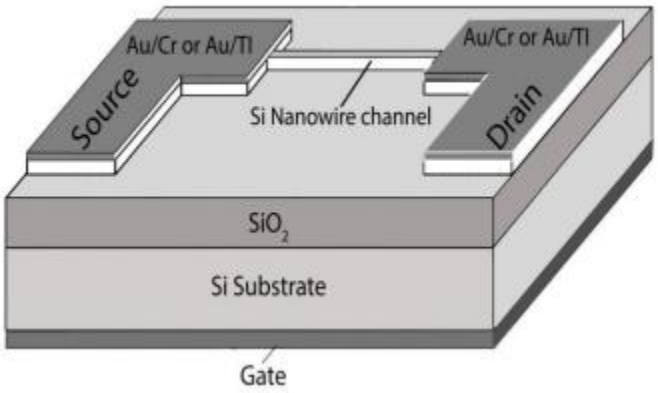


Figure 1.2: Schematic view of Si based NWFET

In the III-V compound semiconductor FET, III-V compound semiconductor like InSb, InAs, InGaAs is utilized as a channel material. These materials give high mobility of transporters in the channel. As an outcome, these III-V compound semiconductor FETs are ready to convey three times higher execution with same power consumption or they can lessen control by one tenth

with same execution, contrasted with Si-MOSFETs. The schematic perspective of a n-sort transistor is appeared in Figure 1.3 where ZrO2 and InGaAs are utilized as the entryway dielectric and the channel material, individually. In this gadget, the bearer mobility is observed to be 3000 cm2 /V-S. Two noteworthy difficulties confronted by III-V compound semiconductor FET are bring down bandgap of III-V material which brings about over the top leakage and expansive static power consumption, and arrangement of a perfect high - k dielectric interface which is fundamental in the electrostatic control of the gadget.

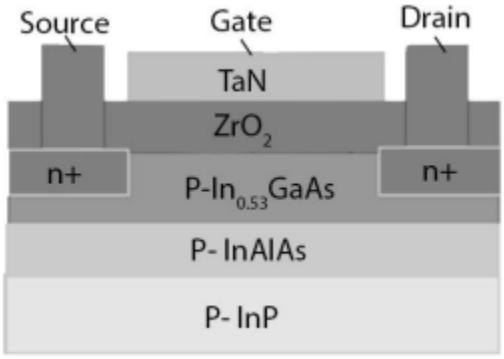


Figure 1.3: Schematic view of n-type III-V compound semiconductor FET

The graphene nano lace transistor utilizes a mono layer of carbon particles, stuffed into a 2-Dhoneycomb cross section as the channel material. Figure 1.4 demonstrates the schematic perspective of this gadget which is manufactured with nano strips having a width around 2 nm. The utilization of graphene as channel material gives high mobility (15,000 cm2/V-S) bringing about quick exchanging, mono layer thin body for ideal electrostatic scaling, and excellent warm conductivity. Thusly, graphene nano strip transistor is competent toconvey 100 or 1000 times' higher execution than Si-MOSFET. The principle challenge confronted by this gadget is the similarly low ION/IOFF proportion (~7), which cause an tremendous measure of vitality in the incorporated circuit made of billions of graphene transistors

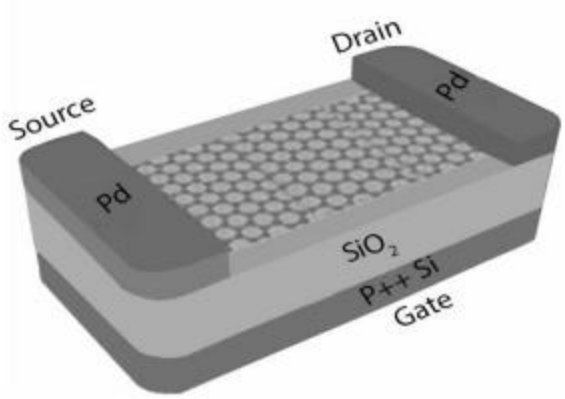


Figure 1.4: Schematic view of graphene nanoribbon transistor

CNTFET utilizes a solitary or a variety of semiconducting single divider carbon nanotubes (SWCNTs) as a channel material. The entryway cathode is put over the CNT channel and isolated from it by a thin layer of entryway dielectric. The schematic perspective of CNTFET is appeared in Figure 1.5, where a variety of four SWCNTs is utilized for channel. CNTFET could be more achievable and promising contender to expand or supplement conventional Si gadget because of its excellent properties, for example, ballistic transport operation, high carrier mobility (103 - 104 cm /V-S), simple coordination of high-k dielectric material (other than SiO2) bringing about better gate electrostatics, solid compound holding, high warm conductivity (1700-3000 W/mK), high compound security, and better coordinating of P what's more, N-sort CNTFETs which streamlines transistor measuring in complex circuits.

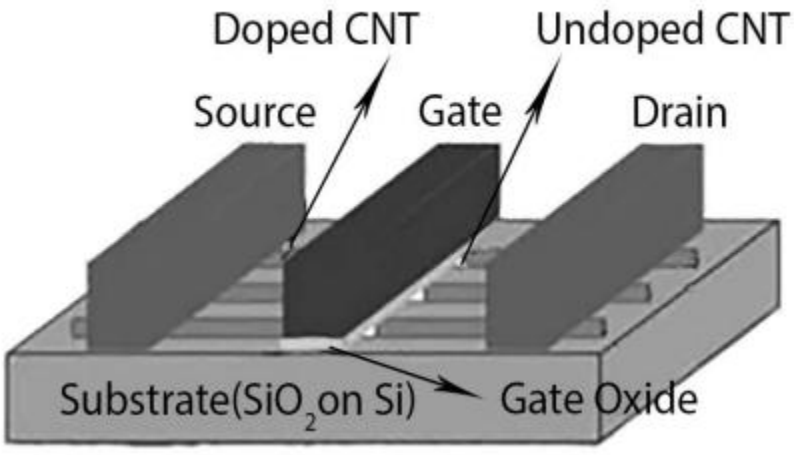


Figure 1.5: Schematic view of CNTFET

The main CNT-based transistor is declared.From that point onward, noteworthy advancements were accomplished in the fabrication of CNT-based gadgets furthermore, circuits. In view of CNTFETs, some cutting edge designs, for example, rationale entryways, fivestage ring oscillator manufactured along a solitary CNT, a capacitive sensor interface circuit, a permeation transport-based decoder, remain solitary circuit components, for example, half-snake whole generators, D-locks and static random get to memory (SRAM) cells have been manufactured. In 2006, IBM exhibited the main IC constructed utilizing SWCNTs. Cao et al. declared that they made medium scale IC utilizing CNTFETs on a thin plastic substrate. Like the first silicon based PC, the CNT PC is a synchronous advanced framework which runs put away projects and is programmable. The working arrangement of this PC accomplishes multitasking by executing an including program and a whole number arranging program simultaneously. In spite of the fact that the working recurrence of the CNT PC is accounted for to be 1 KHz just because of scholarly trial constraints and capacitive stacking presented by the estimation setup, this showing is an imperative turning point in the improvement of complex and exceptionally vitality productive CNT based electronic framework. At display, the major difficulties confronted by CNT innovation are the CNT misalignment and undesirable development of metallic tubes.

The previously mentioned rising gadgets can possibly turn into the successor of SiCMOS in not so distant future. CNTFET and NWFET are 1-D gadgets, graphene nanoribbon FET is a 2-D gadget, and the III-V compound semiconductor FET is a 3-D gadget. 1-D gadgets give ballistic transport operation with no disseminating and in this manner, achieve predominant execution in examination with 2-D and 3-D gadgets. CNTFET gives simple integration of high-k dielectric material because of the nonattendance of dangling bonds, which thus brings about bring down sub-edge slants and lower OFF current. As beforehand said, the mobility of carriers in NWFET, graphene FET, III-V semiconductor FET and CNTFET is higher than Si-MOSFET, which brings about higher carrier speeds and quick exchanging. In CNTFET and graphene transistors, the carrier mobility is in a similar request of size (103 - 104 cm /VS) which makes them promising contender for future rapid circuits. Besides, in light of ITRS 2009 , CNTFET and graphene transistors showed the most elevated plausibility to end up plainly a piece of future gadgets. At the point when this exploration work started, R&D in CNTFET was ahead contrasted with that of graphene transistor. Accordingly, in this proposition, CNTFET-based circuits are focused on.

1.2 Motivation and Objectives

As portrayed before, the scaling of CMOS innovation has been sought after forcefully finished the most recent couple of decades to coordinate more number of transistors on a solitary chip. Nonetheless, material properties are specifically identified with measurement. For conventional Si-based gadgets, as the physical entryway length is come to nanoscale go, numerous gadget level effects, (for example, expanded leakage current, varieties in doping, bigger process varieties and decreased entryway control) are shown with MOSFETs. To conquer these issues, researchers are investigating new choices of Si-CMOS process. CNTFET has turned out to be a promisingelective because of its different unrivaled properties, for example, extraordinary 1-D band structure, ballistictransport operation and low OFF-current together with its similarity to MOSFET as far as characteristic qualities. Accordingly, CNTFET is a promising gadget which empowers high execution and low power designs for the up and coming era of current hardware.

Further, advanced framework design has customarily been related with the binary rationale where advanced calculations are performed on two conceivable rationale esteems that are "0" and "1" in the Boolean space. Since our general surroundings is multi-esteemed, numerous pragmatic applications such as mechanical technology, process control and choice emotionally supportive networks require more than two-esteemed rationale for effective and ideal arrangement. Post showed a meaning of multivalued rationale (MVL) as an extension of customary binary rationale. It declared that the most effective radix for realization of exchanging circuits is a whiz base (e = 2.7183) which demonstrates that the best whole number radix is three instead of two. In 1970's, MVL-based framework executions were accounted for in the specialized literature and eluded as voltage mode ternary circuits.

In the course of the most recent few decades, three-esteemed or ternary rationale has pulled in extensive intrigue as a result of a few points of interest as for the binary rationale in design of computerized VLSI circuits. Figure 1.6 outlines the preferences offered by ternary rationale. This rationale decreases chip region involved by the interconnection wires and useful units in VLSI integration. Ternary signs convey more data on a solitary wire, in this manner decreases number of wires and IC pins required for a similar scope of information. This reductions number of

interconnects and therefore, prompts expanded space between any two wires with no addition of aggregate silicon territory. This additionally diminishes resistance and capacitances related with interconnect and contacts, and as an outcome, ternary rationale accomplishes effortlessness and expanded vitality productivity in computerized design. Besides, other included points of interest are less mind boggling mistake location/blunder amendment code and fast serial/serial-parallel number juggling operation. For instance, 14-bit binary expansion can be acquired by a 9-bit ternary snake which lessens number of swell carriers to around half as for its binary usage and subsequently, increment the speed of electronic circuits around by the factor of two. The exhibition that a proficient MVL usage of a marked 32-bit multiplier can decrease both chip range and power by over half in contrast with its speediest binary partner. In, MVL pieces havebeen added with binary rationale ICs to enhance the general execution of framework. Likewise, the benefits of ternary rationale have been affirmed in some of the applications counting memory, correspondence, machine learning, fluffy rationale, manmade brainpower, mechanical technology, information mining, computerized flag preparing, advanced control frameworks and picture handling and so on.

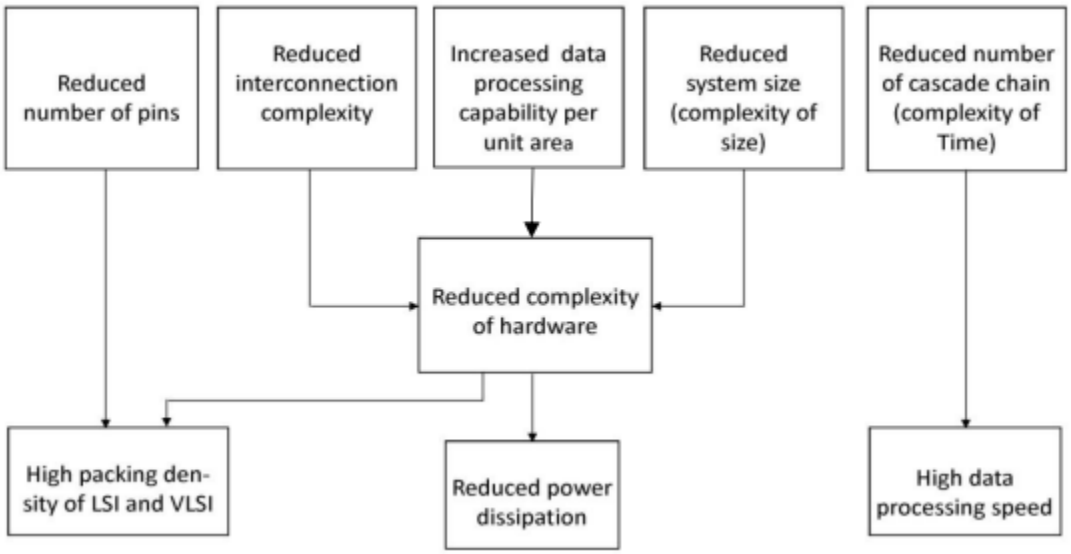


Figure 1.6: Advantages of ternary logic circuit

Voltage-mode MVL circuit forms data in light of voltage levels. The most ideal approach to design and actualize these circuits is utilizing multi-limit technique. In CMOS innovation, multi-

limit design depends on body effects where distinctive inclination voltages are connected to the base or buck terminal of the transistors. To get these inclination voltages, various supply voltages are required which prompts expensive and in addition complex power grid design. On the other hand, ternary rationale has an exquisite relationship with CNTFET gadgets. Specifically, CNTFET gives a remarkable chance of accomplishing two unmistakable edge voltages only by utilizing CNTs with various diameters. Subsequently, a multi-edge design can be refined effortlessly in the CNTFETs.

Previously, the essential worries of VLSI designers were proliferation delay, territory, cost and dependability. Nonetheless, expanding power consumption is being given significance alongside others requirements in the current years, because of expanding levels of integration and longing for portability. There is an astounding achievement and development of portable applications including scratch pad and smart phones, and video based interactive media items, individual remote correspondences frameworks, for example, computerized associates and communicators which requires rapid calculation and endlessly expanded capacities with low power consumption. The consistently expanding market fragment of portable electronic gadgets empowers the execution of dependable battery-worked frameworks. The advance of battery innovation is ease back contrasted with progresses in microelectronics innovation. Hence, it is far-fetched to give a power answer for the versatile frameworks. It has turned out to be basic to create VLSI circuits and frameworks which lessen heat dissipation keeping in mind the end goal to permit a huge thickness of works on a solitary chip. The circumstance has been additionally irritated by the way that the clock rate of microprocessor have just come to at 1 GHz stamp, prompting a huge increment in exchanging power consumption. Moreover, vitality proficient circuits are too required in elite PCs, AC powered frameworks in which sinking extensive measure of heat through bundles is turning into a troublesome issue. Henceforth, designers are confronting with more requirements: little chip zone, high throughput, fast, and at the same time, low-power dissipation.

In the present advanced world, the operations, for example, robotization, process control and numerous other complex calculations are refined by different programmable chips like microprocessors, microcontroller and committed processors and so on. The most essential and

imperative handling unit of these chips is a math and rationale unit (ALU) which is in charge of performing different math and rationale operations, for example, expansion, subtraction, increase, size correlation and XOR and so on. ALU is the core of the guideline execution segment of each processor. For instance, engineering of 8085 microprocessor incorporates 8-bit ALU to process binary information. Some other condition of-craftsmanship binary what's more, ternary ALU designs can be found. The expanding interest of high execution in present day data handling frameworks unmistakably indicates the need of proficient usage of ALU designs as far as hardware, speed and power. In this manner, it is basic to build up a productive ALU utilizing CNTFETs for ternary rationale.

In this proposal, we focus on the realization of CNTFET-based ternary ALU (TALU) for cutting edge electronic frameworks. Novel designs of TALU and additionally its utilitarian modules which incorporate viper, subtractor, multiplier, comparator and elite OR, are presented and analyzed with the current condition of-works of art. These designs are assessed in light of four measurements: gadget number, engendering delay, power dissipation and power-delay-item. As the driving ability is an essential parameter for the advanced circuits, introduced designs are tried under various loading conditions. These designs are additionally broke down at various frequencies to inspect their execution with variety in working frequency. Further, another imperative normal for advanced designs which ought to be considered is their powerlessness to voltage and temperature varieties. For this, the displayed circuits are assessed over a tremendous scope of supply voltage and temperature.

Then again, expanded fascination for transfer speed hungry ongoing applications and more utilization of web have raised an interest for rapid networks. On the web, a message like email or page is exchanged by first breaking it into information parcels, and afterward, sending them towards the goal. Every information bundle contains a header which has the data like information length, information sort, grouping number, source address and goal address, and a payload. In view of the data of the header, information parcel is exchanged to a yield port by the system switch. A router which is a more advanced switch keeps up a steering table and route approaching information bundles from source to goal as indicated by the data put away in the directing table. Routers likewise send data to each other for the refreshing of their steering tables.

All in all, optical fiber based physical medium transport the information parcel from one router to another. Advances in optical fiber innovations like wavelength division multiplexing, have accomplished fast information transportation on optical filaments. To get the advantages offered by optical fiber innovation, routers or system switches ought to be able to meet the expanded information exchange rates. In a system switch, the most tedious undertaking is table queries. New methodologies like strategy based steering, stream investigation and Quality of Service (QoS) are expanding the number and assortment of table queries. The low need bundles, as information are exchanged after the high need bundles, for example, voice and video, to keep up the QoS. These new methodologies require various searches up for every bundle before it is conveyed. For table query errand, programming arrangements like radix tree are moderately moderate and not versatile with the extent of the table. The hash capacity can perform query errand in one memory get to under ordinary conditions, in any case, its most pessimistic scenario look time is extensively higher than that of tree looks. As a result, a number of programming arrangements executing table query undertakings at various system layers are currently being substituted by their hardware partners.

A standout amongst the most productive hardware arrangements is content addressable memories (CAM) which can be incorporated as a co-processor with arrange handling unit to perform table query errand. Further, CAMs are additionally utilized as a part of numerous other key applications incorporating label indexes in affiliated store memory framework , interpretation look-aside cradles in virtual recollections, parametric bend extraction, information pressure, picture coding, real-time design looking in infection (or interruption) discovery frameworks and quality example coordinating in bioinformatics and so forth. Since a large portion of these applications utilize littler CAMs, the ebb and flow look into identified with CAMs is primarily administered by arrange applications which request high thickness CAMs with low power and high hunt speed.

Design of low power and fast CAM structures keeps on being sought after, and ballistic transport operation and low off current qualities of CNTFET make them excellent contender for rapid and expanded integration thickness of CAM design. In this theory, designing of CNTFET-based CAM cells is engaged for quick match operation. Novel CAM structures are given and looked at their current partners.

Objectives Of The Research Are:

1) To create structures and circuits of ternary rationale based ALU (TALU) streamlined in terms of hardware utilizing CNTFETs.

2) To enhance the execution of sub-squares of above hardware proficient TALU for power-delay product (PDP) proficiency utilizing diverse circuit methods.

3) To locate another engineering of TALU and circuits of its sub-squares advanced for low power ternary framework utilizing CNTFETs.

4) To design ternary rationale based CAM cell for quick pursuit operation utilizing CNTFETs.

1.3 Organization of Thesis

This theory is composed as takes after:

CHAPTER2 Manages literature review. To begin with, subtle elements of CNTFET gadget are given, and afterward ternary rationale and number juggling circuits executed in CMOS and CNTFET innovation are assessed. Further, a study of CAM cells acknowledged utilizing CMOS and also CNTFET is included.

CHAPTER 3 Introduces a design of 2-bit hardware improved TALU (HO-TALU) utilizing CNTFETs. Engineering and usefulness of the 2-bit HO-TALU are portrayed. HO-TALU presents snake subtractor (AS) module which takes out a subtractor obstruct from the ordinary design. This segment is trailed by the portrayal of ternary capacity minimization and realization. Design and usage of HO-TALU practical modules and their integration over TALU cut are clarified. HO-TALU modules use binary gates with ternary gates. The last area of this section exhibits comes about for useful test and execution assessment of HO-TALU including its hardware appraisal.

CHAPTER 4 Clarified the execution helped designs of sub-squares of 2-bit HO-TALU utilizing CNTFETs. Initial, three designs of ternary full viper (TFA) which is a critical subblock of AS module, are portrayed. The primary TFA design contains a symmetric draw up and pull-down networks alongside a resistive voltage divider as its essential part, which is configured utilizing

transistors and prompts a fast design. The second TFA is designed in light of complimentary pass transistor rationale style with a specific end goal to accomplish low power consumption. The third TFA is actualized utilizing dynamic rationale style with a specific end goal to get diminished power-delay-product. All new TFA designs are broke down, assessed and thought about with the current snake designs. This segment is trailed by the exhibit of design of new comparator module of 2-bit HO-TALU. This circuit is designed utilizing pass transistor rationale style and limits the quantity of stages to get enhanced execution. It is utilized as a part of execution of 2-bit and N-bit comparators which utilize binary tree design to remedy the voltage levels. New design of comparator is broke down, assessed and contrasted and the existing comparator designs.

CHAPTER 5 Depicts a design of 2-bit power advanced TALU (HO-TALU) utilizing CNTFETs. The design and elements of 2-bit PO-TALU are clarified which is taken after by the exhibition of ternary capacity minimization and realization. PO-TALU utilitarian squares: viper subtractor-selective OR (ASE) and multiplier, are designed utilizing complementary CNTFET-based binary computational unit and a low many-sided quality encoder. ASE dispenses with elite OR and subtractor hinders from the ordinary engineering. Multiplier utilizes another convey include (CA) obstruct set up of ternary half snake. Usage of these squares is indicated which is trailed by the extension of PO-TALU for 2-bit cut. The last area of this part shows reproduction results and correlation with existing CNTFET-based designs.

CHAPTER 6 Presents Binary CAM (BCAM) and ternary CAM (TCAM) cells designed based on low capacitance seek rationale in CNTFET innovation. Another three-esteemed CAM (3CAM) cell is additionally exhibited utilizing CNTFETs. This cell utilizes multi edge voltage structure in execution of low capacitance seek arrange which prompts quick and reduced CAM design. The exhibited CAM cells are mimicked and contrasted and the current memory designs.

CHAPTER 7 Introduces the outline of the work exhibited in this proposal, by counting key discoveries, fundamental contributions and vital perceptions, and furthermore talks about conceivable headings for the future work.

CHAPTER 2

Literature Review

2.1 Introduction

In chapter 1, the capability of CNTFET for superior and low power current designs due to its different excellent properties, for example, novel 1-D band structure, ballistic transport operation

also, low OFF-current, has been illustrated. The importance and inspiration to create CNTFET-based designs of ternary (three-esteemed) number juggling and rationale unit (TALU), and substance addressable memory (CAM) cells, have additionally been examined. Researchers and researchers intrigue in ternary rationale is expanding in the course of recent decades as a result of giving a few focal points for example, decreased chip range and less number of interconnects, less unpredictable blunder recognition/mistake rectification code and rapid serial/serial-parallel number juggling operations and so on. As a result, noteworthy distributed literature is accessible on design and execution of ternary number juggling also, rationale circuits utilizing MOSFETs. Also, because of the one of a kind property of CNTFET for controlling edge voltage by the CNT diameter, various researchers have discovered it as a central gadget for the ternary design. In this part, the literature accessible on the designs and circuit usage of ternary number juggling and rationale circuits in view of CMOS and also CNTFET innovation is surveyed. Further, CAM has been in look into since most recent couple of decades. A few circuit systems and models have been created to diminish the cell territory, delay and power consumption of CAMs. This part gives a concise survey of different designs of CAM cell created in CMOS and CNTFET innovation.

In segment 2.2, gadgets properties of CNTFET which make it extremely focused in future hardware, is given. Ternary rationale and number juggling circuits executed in CMOS and CNTFET innovation are looked into in area 2.3. An audit of CAM designs acknowledged utilizing CMOS and CNTFET is given in area 2.4. This is trailed by the area 2.5 in which holes in the distributed research work have been incorporated alongside the issue articulation of the theory.

2.2 Carbon Nano Tube Field Effect Transistor (CNTFET)

Carbon nanotube (CNT) is an allotrope of carbon with barrel shaped structure, which could be single-walled (SWCNT) or multi walled. A SWCNT is acquired by moving up a sheet of graphite along a wrapping vector Ch = n1a + n2b, where n1 and n2 are certain whole numbers which indicate the hilarity of the tube, and "an" and "b" are grid unit vectors, as appeared in Figure 2.1. Contingent on the estimation of n1 and n2, SWCNT can be either metallic or

semiconducting. On the off chance that n1-n2 is a numerous of 3, SWCNT is metallic or else it is semiconducting. Essentially, SWCNT is additionally arranged into three gatherings as indicated by estimation of n1 and n2: (1) easy chair CNT when n1 = n2 = n, (2) crisscross CNT when n1 = 0 or n2 = 0, and (3) chiral CNT when n1 and n2 are extraordinary and nonzero. All easy chair CNTs act as conductors. Then again, crisscross and chiral CNTs indicate conductor conduct when the distinction between the records (n1-n2) is a number various of 3 else they are semiconducting CNTs, which are utilized as a part of CNTFET

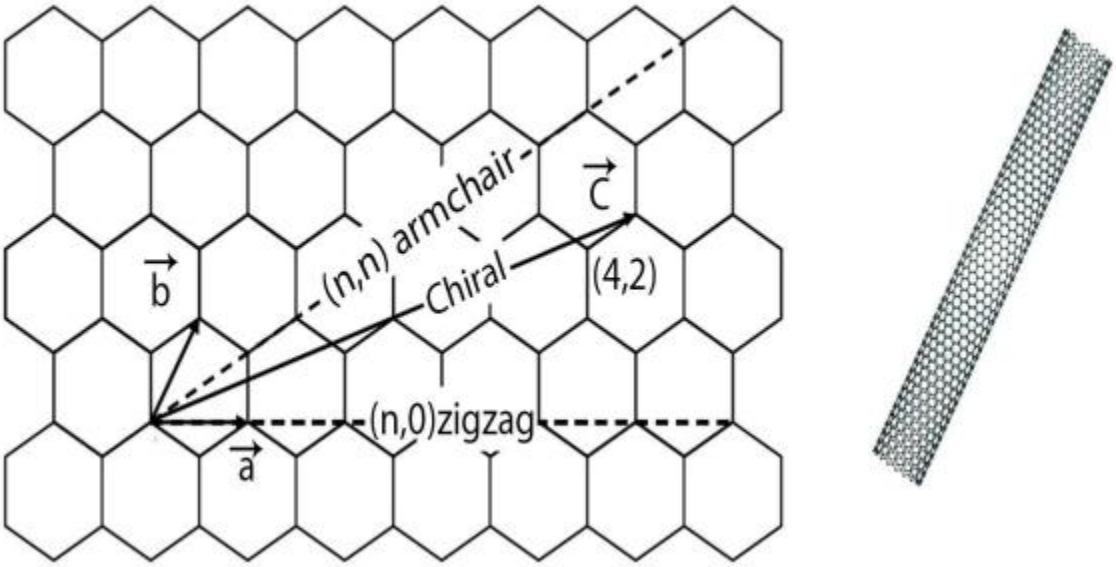


Figure 2.1: Unrolled sheet of graphite and the rolled lattice structure of CNT

CNTFET is a kind of FET that makes utilization of a solitary or a variety of semiconducting SWCNTs as a channel shaped between two metal electrodes going about as a source and depletes contacts. Gadget is turned ON and OFF through the gate electrode put around CNT channel. The schematic perspective of CNTFET is appeared in Figure 2.2 (a). Undoped portions of CNTs fill in as a channel under the gate electrode, while intensely doped CNT portions set between the entryway and the source/deplete electrodes offer low electrical resistance in the ON-

province of CNTFET. Since the electrons are just restricted to the limited CNTs, carrier mobility goes up considerably because of ballistic transport operation, in examination with the mass MOSFET.

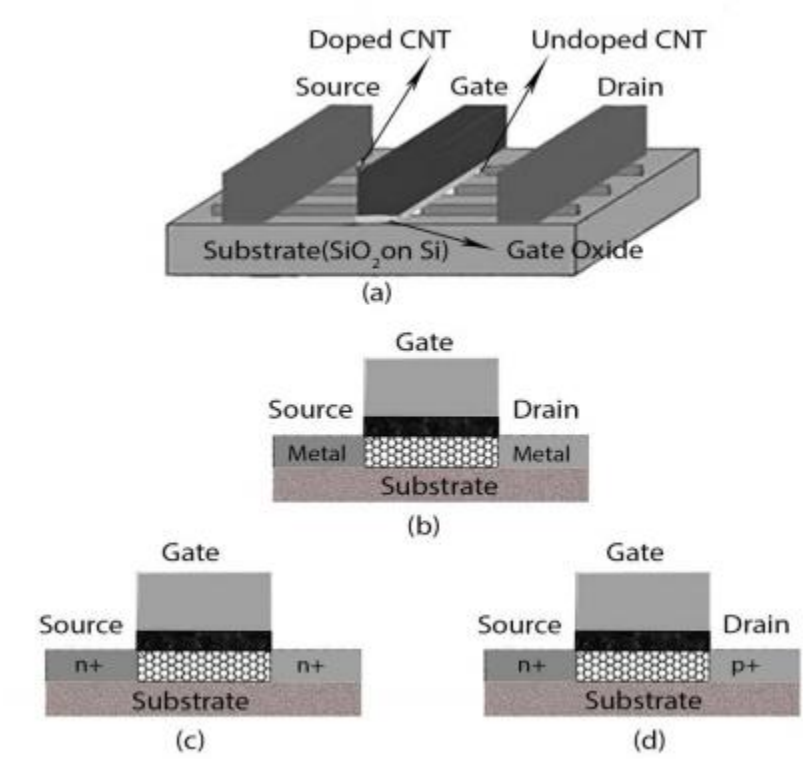


Figure 2.2: Carbon nanotube field effect transistor (CNTFET) (a) Schematic view of a CNTFET device, (b) SB-CNTFET, (c) M-CNTFET, (d) T-CNTFET

Three sorts of CNTFET gadgets have been accounted for in the literature. They are known as schottky barrier CNTFET (SB-CNTFET), MOSFET-like CNTFET (M-CNTFET) and bandto-band tunneling CNTFET (T-CNTFET). SB-CNTFET chips away at the rule of direct tunneling through a schottky barrier (SB) at the source/deplete channel junction. This gadget is created by reaching amongst metal and semiconducting CNT, and appeared in Figure 2.2 (b). The nearness of SB at the CNT-metal junction restricts the trans-conductance of the CNTFET in the ON state and lessening current conveys capacity, which thusly decreases the reasonableness of SB-CNTFET for fast applications. Moreover, SB-CNTFET appears solid ambipolar conduct which constrains the utilization of this gadget in complementary transistors-based circuits.

To wipe out the previously mentioned disadvantage of SB-CNTFET, M-CNTFET has been created and appeared in Figure 2.2 (c). This gadget works like an ordinary MOSFET with fast and low power consumption. It is manufactured utilizing intensely doped source and depletes CNT areas. Because of nonappearance of SB at source/deplete channel junction, M-CNTFET has altogether higher ON current which makes it extremely reasonable for ultra-elite computerized circuits. T-CNTFET which is appeared in Figure 2.2 (c) has low ON present and extremely great cut-off qualities. Thus, this gadget turns out to be a super contender for subthreshold furthermore, ultra-low-power design.

In view of the expressed focal points and in addition similitudes of M-CNTFET with MOSFET in terms of operation and intrinsic qualities, this sort of CNTFET is utilized as a part of this proposal for usage of the displayed circuits.

The gate width of CNTFET can be approximated as:

$$W \approx \min(W_{min}, N \times S) \quad \textbf{(2.1)}$$

Where W_{min} is the base gate width, N is the quantity of tubes and S is the pitch which is the separation between the focuses of two connecting CNTs under a similar entryway. The edge voltage is the voltage expected to turn ON the gadget electro-statically by means of the entryway. For a CNTFET, it can be approximated to the primary request as the half band hole and can be computed as

$$V_{th} \approx \frac{E_g}{2e} = \frac{1}{\sqrt{3}} \frac{aV_\pi}{eD_{CNT}} \approx \frac{0.43}{D_{CNT}(nm)} \quad \textbf{(2.2)}$$

Where Vπ (= 3.033 eV) is the carbon π-π bond energy in the tight bonding model, a (= 0.249 nm) is the carbon-carbon atom distance and e is the unit electron charge. D_{CNT} is the diameter of the CNT, which depends on the chirality vector (n1, n2) and can be calculated as

$$D_{CNT} = \frac{\sqrt{3}a}{\pi}\left(\sqrt{n_1^2 + n_2^2 + n_1 n_2}\right) \approx 0.0783(nm)\left(\sqrt{n_1^2 + n_2^2 + n_1 n_2}\right) \quad (2.3)$$

As per the eq. (2.2) and (2.3), the edge voltage of CNTFET is contrarily proportional to the CNT diameter, and CNT diameter is specifically proportional to chirality vector. For a CNTFET with (19, 0), CNT diameter is 1.487 nm and subsequently, edge voltage is 0.289 V. Thus, for a CNTFET with (13, 0), CNT diameter is 1.02 nm and subsequently, edge voltage is 0.422V. The edge voltage of P-CNTFET is same as that of N-CNTFET with an inverse sign. As the chirality vector expands, edge voltage of CNTFET perishes. Subsequently, CNTFET gives a novel chance to setting edge voltage by differing the chirality vector of CNT. Diverse research bunch have illustrated propels on assembling process for very much controlled CNTs. For instance, Li et al. have utilized discrete synergist nano-particles of different sizes for development of single divider CNTs (SWCNTs) with controlled chirality vectors. Ohno et al. have introduced a plausibility of chirality task of SWCNT by small scale photocurrent spectroscopy. Wang et al. has portrayed an amalgamation procedure utilizing diverse carbon antecedents on Co−Mo impetuses for creating SWCNTs with very much controlled chirality structure. Lin et al. has announced present handling procedures on control the edge voltage of different tube CNTFET.

Other excellent properties which make CNTFET a potential contender for building exceptionally productive electronic framework requiring superior and low power are specified as takes after:

1. Long disseminating mean free way (~1μm) whichprompt bring down delay and less heating which is extremely consequential from IC perspective [97-98].

2. High carrier mobility (10^3– 10^4 cm 2 /V-S) in semiconducting CNTs which gives high ON current (>1mA/μm).

3. Simple integration of high-k dielectric material (other than SiO_2) because of the nonattendance of dangling bonds, bringing about better entryway electrostatics.

.4. Solid synthetic holding, high warm conductivity (1700-3000 W/mK) and synthetic solidness prompt high current densities (~ 10^{10}A/cm^2).

5. Better coordinating of complementary CNTFETs: P and N-sort CNTFETs with same sizes have rise to carrier mobility, along these lines convey same drive streams, which is extremely imperative for transistor measuring of complex circuits.

Other than the specified points of interest of this developing innovation, it additionally confronts some major challenges that must be made plans to make it attainable for business reason. These challenges are said as takes after:

1. CNT pressing thickness

2. CNT diameter and thickness variety

3. CNT misalignment

4. Metallic-CNT (m-CNT) development

Empowering endeavors are being made for settling these difficulties so as to time. CNT blend procedures, for example, wafer-scale CNT exchange alongside wafer-scale-adjusted development , various cycles of synthetic vapor testimony development and CNT exchange through various conciliatory layers and so forth., empower us to pack about 5-50 CNTs/μm. Durkop et al. created CNTFET with top notch ohmic contacts, high-k dielectrics HfO2 movies furthermore, electro statically doped source and deplete districts. Researchers depicted different CNT doping techniques, for example, coordinate synthetic doping [107] and nuclear layer statement. For P-CNTFET, Mann et al. have utilized Palladium (Pd) which prompts ohmic contact between CNT valance band and Pd electrode. Thus, for N-CNTFET, Zhang et al. have used Scandium which prompts ohmic contact between CNT conduction band and Sc electrode. Zhang et al. presented incorporated structure and adjusted dynamic format system to beat the effect of CNT varieties. For the disposal of undesirable m-CNTs, different handling strategies for example, particular compound scratching, current-incited electrical consuming] and VLSI compatible m-CNTs evacuation were depicted. Patil et al. illustrated robotized calculation and design system to execute misaligned CNT-insusceptible rationale structures

Researchers proposed distinctive CNTFET gadget demonstrates in the literature. Stanford demonstrates is utilized as a part of this proposition, to assess CNTFET-based circuits under different test conditions and to perform correlation with their current counterparts, at 32nm

innovation node. The working voltage (V_{dd}) for all proposed designs is picked as 0.9V because of default estimation of the CNTFET Stanford show. This standard model has been designed for MOSFET-like single-walled CNTFET (M-CNTFET), in which every transistor may incorporate at least one CNTs as its channel. This model considers a reasonable, circuit-good CNTFET structure and incorporates pragmatic gadget non-idealities. The demonstrated non-idealities join between CNT charge screening effects, diffusing, schottky-barrier effects at the contacts, parasitic, doped source-deplete extension locales, back-entryway (substrate predisposition) effect furthermore, source/deplete, and entryway resistances and capacitances. The model additionally incorporates a full transcapacitance system to convey more exact transient and dynamic reaction. The innovation parameters of CNTFET alongside their concise portrayal and numeric esteem are given in Table 2.1

Table 2.1: Technology parameters for CNTFET

Parameter	Description	Value
L_{ch}	Physical channel length	32.0 nm
L_{geff}	The mean free path in the intrinsic CNT channel region	100.0 nm
L_{ss}	The length of doped CNT source-side extension region	32.0 nm
L_{dd}	The length of doped CNT drain-side extension region	32.0 nm
E_{fi}	The Fermi level of the doped S/D tube	0.6 eV
K_{gate}	The dielectric constant of high-k top gate dielectric material	16.0
T_{ox}	The thickness of high-k top gate dielectric material	4.0 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	40.0 pF/m
V_{fbn}, V_{fbp}	Flatband voltage for n-CNTFET and p-CNTFET, respectively	0.0 eV, 0.0 eV
L_channel	Physical gate length	32.0 nm
Pitch	The distance between the centers of two adjacent CNTs	20.0 nm
L_{eff}	The mean free path in p+/n+ doped CNT	15.0 nm
phi_M	The work function of Source/Drain metal contact	4.6 eV
phi_S	CNT work function	4.5 eV

2.3 Three-esteemed (Ternary) Arithmetic and Logic Circuits

Ternary arithmetic and rationale circuits designed in MOSFET and additionally CNTFET innovation are talked about in the accompanying sub-segments.

2.3.1 Ternary Circuits in light of MOSFET

A few creators [130-139] have introduced MOSFET-based designs of ternary rationale circuits. In most cases, they utilized power supply voltages higher than gadget limit voltage, bigger offchip resistors and various power sources, which result in high power consumption in the circuits. Hotshot and Antoniou [62] built up a low power ternary rationale family which contains a set of inverters, NAND and NOR entryways. Utilizing these entryways, they executed half and full snake, what's more, 1-trit multiplier, which were additionally used in development of a move enroll, a N-trit viper also, a N-trit multiplier, and cyclic convolution. These circuits were developed utilizing MC 4007 also, MC14011 discrete transistors and tried to investigation their

execution. It was demonstrated that they get huge lessening in power-delay product (PDP) and gadget tally concerning prior ternary designs displayed in Heung and Mouftah exhibited ternary rationale family that does exclude resistors. They created inverters, NAND and NOR gates in light of the utilization of consumption upgrade complementary metal-oxide-semiconductor (DECMOS) innovation, at that point introduced a design of ternary full viper utilizing these gates. These circuits use two power supplies lower than the limit voltage of transistors. They were contemplated utilizing SPICE 2G reproduction bundle. It was demonstrated that they give low power consumption and fast in correlation with their binary partner. Above depicted ternary circuits of require four kind of gadgets in particular the exhaustion PMOS, the exhaustion NMOS, the improvement PMOS and the upgrade NMOS. The standard CMOS process does not bolster exhaustion MOSFETs. In this way, these designs are not perfect with the standard CMOS process.

Srivastava and Venkatapathy created positive ternary inverter (PTI), negative ternary inverter (NTI) and ternary full viper without utilizing exhaustion mode transistors and resistors. They designed these circuits utilizing CMOS inverter and pass transistors (at the yield) in 2 µm n-well standard CMOS procedure to work them underneath + 2V. In these circuits, width/length (W/L) proportions of the transistors were changed in accordance with get ideal execution. It was demonstrated that PTI and NTI get change in transient time, clamor margin and chip zone by the factor of four, half and two, separately, in correlation with their partner of executed in DECMOS innovation.

Notwithstanding, in these designs, the adaptability in process alteration to modify limit voltage of MOSFETs was truant. Srivastava utilized back-entryway inclination strategy furthermore with the W/L proportion of MOSFET to get sought area of transition district (around the halfway between low what's more, high voltage levels) in dc voltage exchange qualities. They were designed STI, NTI and PTI for operation at a low voltage (± 1 V) in 2 µm, n-well standard CMOS innovation, recreated with SPICE 3 and used in the design of CMOS ternary rationale circuits. Wang et al. detailed dynamic ternary rationale circuits in which Yoeli-Rosenfeld polynomial math was actualized. In these circuits, an overlapped four-stage timing plan was utilized and distinctive essential circuit piece were associated by the allowed fan-out outlines. These circuits were reenacted utilizing SPICE program with 2 µm CMOS process parameters. It

was discovered that dynamic circuits indicates diminishment in speed-power-range product by three to four times than static ternary circuits. Be that as it may, these circuits experience the ill effects of dc power dissipation and debased voltage swing due to rationale. Wu and Huang recommended dynamic ternary circuits which utilize two-stage non-overlapped clocks and have full voltage swing with no dc power dissipation. In view of NMOS differential tree, they additionally introduced basic ternary differential rationale (STDL) for dynamic complex circuits to frame a pipeline framework.

These circuits were reproduced utilizing SPICE program with 1.2 µm CMOS process parameters. It was demonstrated that PDP of these circuits is just 23% to that of dynamic designs introduced. These circuits likewise have advantage in term of format region regarding the designs. In any case, power supply voltages utilized as a part of circuits are too low and along these lines, commotion and drive spike can without much of a stretch impact them. Dynamic circuits require edge balanced MOS (non-standard CMOS) handling and four power supplies. Also, the most astounding voltage accessible in the circuit is utilized to drive the precharge transistors and to build the edge voltage of PMOSFETs by methods for body effect where the mass capability of these transistors is being raised over the high voltage level. Subsequently, yield rationale swing accessible is not exactly the greatest voltage and clamor margin is therefore lessened. A. Herrfeld and Hentschke created ternary dynamic differential rationale (TDDL) and exhibited a TDDL-based ternary full snake. This dynamic circuit method needs just a solitary clock flag and its reverse. The TDDL-based circuit utilizes improvement mode MOS transistors with edge voltages (Vth) < ΔV, where ΔV speaks to the differential voltage between two neighboring states bringing about bigger commotion margin. Other good properties are no static power consumption and utilization of standard CMOS process limited to upgrade mode P-sort and N-sort MOS transistors. In any case, these circuits are very intricate (least 15 transistors required for an inverter). Totto and Saletti additionally proposed a dynamic circuit arrangement that permits the usage of ternary circuits utilizing a standard CMOS process, with just three power supplies, most extreme conceivable commotion margin and zero static power dissipation, to the detriment of a somewhat more unpredictable circuit structure (least 9 transistors required for an inverter).

Mateo and Rubio introduced semi adiabatic ternary (QAT) CMOS rationale keeping in mind the end goal to get ternary rationale advantage of diminishing the territory for low-power advanced ICs. They understood fundamental ternary gates and ternary half snake. These circuits were recreated utilizing the level six model of a 1 µm CMOS innovation in HSPICE program. It was exhibited that PDP of QTA based ternary half viper increment by one request of greatness in examination with that of adiabatic binary half viper having non completely adiabatic exchanging, however it diminishes by two requests of greatness contrasted with that of static binary half viper and dynamic ternary half snake QTA based ternary half viper additionally indicates 65% zone sparing as for adiabatic binary rationale. Mateo and Rubio additionally showed a QAT-based 5 x 5 trit multiplier actualized utilizing 0.7 µm CMOS innovation. The announced outcomes demonstrate that PDP of QTA based 5 x 5 multiplier increments by one request of greatness in examination with that of completely adiabatic binary 8 x8 multipliers having non completely adiabatic exchanging and the breakage of reversibility, however it diminishes by one and seven request of greatness contrasted with that of static CMOS binary 8 x 8 multiplier and semi adiabatic binary 8 x 8 multiplier separately.

QTA based multiplier likewise indicates 60% range sparing and advantage in steering concerning completely adiabatic binary. Shivashankar and Shivaprasad displayed a methodical methodology for the disentanglement furthermore, execution of ternary capacities utilizing a 3-to-1 line ternary multiplexer as building piece. Guide technique which decreases number of design steps, was utilized for improvement of ternary capacities. At least one information factors were considered as information select factors in the realization of ternary capacities. As a result, this realization requires less multiplex in examination with the designs. A calculation for lessening unary administrators and ternary gates required in the information ways was likewise examined. Creators considered single level and multi-level multiplexing procedures, and created designs of a ternary snake, sub tractor and ternary to simple converter.

Sipos et al.depicted a design technique for ternary multiplexers with any number of data sources. They utilized 3-to-1-line ternary multiplexer as an essential circuit to design those multiplexers having higher number of information sources. This fundamental multiplexer was constructed utilizing least and most extreme ternary capacities, and the control circuit was constructing utilizing ternary circuits named as pointers of rationale levels. Designs of multiplexer were

actualized utilizing supplementary symmetrical rationale circuit (SUS-LOC) structure, and recreated in ORCAD condition utilizing transistors from Breakout library to approve their operation.

Sathish et al.exhibited a technique for characterizing, implementing, analyzing, testing ternary circuits with VHDL Simulator. They exhibited VHDL displaying of ternary circuits, for example, 9-to-1-line and 27-to-1-line multiplexers, half snake, half subs tractor, full viper, full subs tractor, 1- bit multiplier, 1-bit and 2-bit comparator, swell convey snake and convey spare viper, 1-bit and 2-bit position shifter and barrel shifter, where all circuits were actualized utilizing 3-to-1-line multiplexers. Every one of the designs were recreated utilizing VHDL test system with the assistance of innovation subordinate bundle called 9-state StdLogic_1164 bundle to check their usefulness and timing determinations.

Gundersen et al. conveys free adjusted ternary snake (BTA) actualized utilizing revived CMOS semi skimming entryway (RSFG) devices. They additionally understood an adjusted ternary subs tractor by applying transformed contributions to BTA. This snake contains RSFG ternary inverter squares, auto zero circuit which change over an info flag to a legitimate energize flag, and metal plate capacitors. BTA offers convey free expansion and hence, can be used as a fundamental piece in figuring it out quick multiplier circuits. Creators likewise depicted a design of ternary counter in light of RSFG devices. This counter uses adjusted ternary documentation and reasonable for usage of quick viper structure which can include both positive and negative operands. They likewise introduced a comparator structure in view of RSFG ternary inverter pieces and metal plate capacitors. RSFG based designs were reenacted by utilizing Cadence with simple design condition in 90 μm CMOS process. These circuits work at a clock frequency of 1 GHz with power supply voltage of 1.0 V as it were.

Zeng et al.exhibited a design of ternary full snake in light of multi-esteemed switch-level hypothesis. Utilizing this ternary full snake, they designed a ternary swell convey viper which has the characters of low power and fast. These designs utilize complementary pass-transistor rationale (CPL) which prompts straightforward, consistent and symmetry structure as for entryway level designs. The creators depicted low power design of ternary extent comparator (TMC) in light of switch-level design method. This circuit has full-swing yield flag which enhances commotion margin, and less number of transistors guaranteeing a straightforward

circuit and littler zone than entryway level TMC. Designs were mimicked in PSPICE, utilizing TSMC 0.25 µm CMOS gadget parameters. Recreation comes about demonstrate that they devour less vitality (roughly by a factor of two) in examination with gate level designs.

Dhande et al.displayed the engineering, design and usage of 2 bit ternary arithmetic and rationale unit (TALU). This design performs operations on 2-bit operands and can be reached out for N-bit operands by falling N/2 TALU cuts. It utilizes ternary translates and ternary gates. These CMOS ternary gates were acknowledged in upgrade and consumption MOS innovation making them appropriate for VLSI execution. TALU sub-pieces were reenacted in PSPICE program. It was discovered that sub-pieces of TALU get noteworthy decrease in power consumption, delay and hardware multifaceted nature in correlation with that. For example, TALU sub-square, for example, full viper (FA) utilizes 56 ternary gates just while FA utilizes 108, 115, 83 and 120 binary gates with an expansion encoder, separately.

Aline et al.exhibited the design of regular pieces of a ternary DSP utilizing SUS-LOC structure. SUS-LOC utilizes improvement and exhaustion sort MOSFETs due to their extraordinary edge voltages. The creators designed a library of fundamental ternary rationale components, memory and arithmetic cells, and utilized VHDL to get execution displaying and engineering level reproduction. Every single revealed result were extricated in 0.25 µm CMOS innovation with transistor demonstrate cards gotten from level 3 of SPICE. It was demonstrated that DSP sub-modules, for example, viper, enroll and shifter and so forth get points of interest in delay and vitality consumption contrasted with binary CMOS circuits. Chen and Rajashekhara exhibited a multiplier design utilizing ternary rationale and excess binary marked digit (RBSD) numbers. Bit match recoding was utilized for era of halfway products in RBSD shape utilizing two's supplement (TC) of multiplier and multiplicand operands.

At that point RBSD adders were utilized for including incomplete products. The resultant RBSD product was changed over once more into TC frame by using a RBSD to TC converter designed in view of get think back system introduced. RBSD number framework permits convey free expansion of halfway products which prompts fast multiplier design. Likewise, since every ternary piece underpins a RBSD digit, the utilization of ternary rationale in RBSD adders lessens circuit intricacy and number of interconnects in correlation with the designs where two bits for every RBSE digit are utilized because of binary rationale. Every utilitarian unit and whole design

of 4 x 4 multiplier was reenacted utilizing SPICE program to affirm the accuracy of rationale. Designs of RBSE snake and incomplete product generator were delivered utilizing MAGIC programming on SUN work station.

Wang et al.presented the guideline of vitality recuperation and switch level design system for the design of ternary circuits. They exhibited a design of 4 x 4 ternary adiabatic multiplier. In this design, twofold power clocks were utilized for charging and releasing of the yield node capacitances in adiabatic way through bootstrapped NMOS transistors and cross-memory structure. This design was recreated in PSPICE with TSMC 0.25 μm CMOS gadget. The announced outcomes demonstrated that it devours 91% less vitality as for that of twofold passtransistor rationale based ternary multiplier.

2.3.2 Ternary Circuits in view of CNTFET

In the current years, CNTFET has been widely contemplated as a potential contrasting option to the ordinary MOSFET for implementing two esteemed and multi esteemed circuits. In any case, the execution of various esteemed circuit could be of more intrigue in CNTFET innovation. Since the most ideal approach to design voltage-mode multi-esteemed circuit is the various edge strategy, and coveted limit voltage can be acquired simply by utilizing distinctive diameter of CNT in CNTFET gadget.

Roychowdhury et al.built up a practically entire arrangement of ternary administrators based on CNTFET. This set contains exacting and its supplement, cycle and its supplement, min, and tsum administrators. In design of these administrators, all rationale levels are communicated as far as voltage values considering adequate clamor margin to stay away from mistake in calculation. Utilizing these ternary administrators, multiplexers, half adders, and swell convey full adders were produced and reenacted utilizing HSPICE with circuit-perfect model of CNTFET exhibited. Notwithstanding, these ternary circuits require vast ohmic resistive burdens (no less than 100 Mω esteems) which result in territory overhead and bigger power dissipation. Moreover, resistive load is hard to be incorporated into CNTFET innovation.

Lin et al.displayed a design of CNTFET-based ternary inverter in which resistive load was supplanted by P-CNTFET dynamic load. In light of a similar design method, they created ternary NAND and NOR gates in [67]. These entryways were recreated utilizing HSPICE with Stanford

CNTFET model. The announced outcomes showed that PDP of this ternary inverter is lessened by 300% in correlation with its partner. Also, these gates find less chip range, bigger noise margin and better integration in correlation with CNTFET based ternary designs. Creators additionally introduced a design system which utilizes both ternary rationale entryways and binary rationale gates to exploit both rationale design styles' benefits. It was appeared that this design method prompts 90% decrease in PDPs of ternary half viper and 1-bit multiplier regarding their counterparts designed utilizing CNTFET based ternary entryways as it were.

Nan et al.showed CNTFET-based ternary structures without bigger off chip resistor that utilization a mix of various back biasing voltages and diameter of CNTFET for low power consumption. These circuits were reproduced utilizing HSPICE with CNTFET model. It was discovered that the displayed STI design gets no less than 1000 times diminishment in PDP with regard to STI designs. Thus, it indicates decrease in leakage current by five also, nine requests in correlation with STI, individually. Furthermore, it utilizes four transistors rather than six transistors utilized as a part of STI.

Liang et al. designed pseudo-complementary CNTFET-based ternary circuits by considering an exchange off between static power consumption and territory cost. They supplanted resistors utilized as a part of [64] by P-CNTFET (with gates are associated with ground) and finished edge voltage control by altering chirality vector in CNTFET. HSPICE reproduction comes about were confirmed the accuracy of pseudo complementary approach. Creator additionally portrayed a reasonable structure through transistor-level investigation to evaluate blunder rate of ternary gates. They created stochastic computational models for dependability assessment of ternary gates.

Moaiyeri et al. showed CNTFET-based ternary circuits which execute all sort of ternary rationale including positive, negative and standard, in a solitary structure. They introduced designs of ternary inverters, NAND and NOR entryways, half viper and 1-bit multiplier. These circuits were recreated utilizing HSPICE with 32nm CNTFET model. Recreation comes about shown lessening in vitality consumption by 53% and 40% by and large for ternary rationale what's more, arithmetic circuits in examination with their relating designs. In expansion, these circuits indicate high driving capacity, bigger noise margin and safety to process varieties as for ternary rationale and arithmetic circuit.

Vudadha et al.exhibited a ternary multiplexer based design technique for realization of CNTFET-based ternary circuits. By utilizing transmission gate based ternary 3:1 multiplexer, they created ternary half snake and 1-bit comparator circuits. These designs were recreated in HSPICE with CNTFET model. It was discovered that ternary half viper gets lessening in delay and PDP by 27% and 23%, individually, in correlation with its partner introduced. **Vudadha et al.** exhibited a design of encoder streamlined at transistor level for execution of ternary capacities. Using this encoder, they actualized ternary half snake.

Results got from HSPICE showed change in delay, power and PDP by 22%, 20% and 39% in correlation with that of ternary half viper. **Vudadha et al.**built up a CNTFET-based ternary comparator that utilizations binary rationale alongside ternary rationale for streamlined usage. 1-bit comparator design was expanded for N-bit operand length by utilizing gathering procedure in view of prefix structure. This comparator design with various operant lengths was reenacted in HSPICE with CNTFET model.

Reproduction comes about were demonstrated power dissipation of 0.65 µW and delay of 21 pS for 1-bit design. The creators revealed an alternate execution of ternary comparator that diminishes the unpredictability of design by taking out the need of complex ternary decoder. HSPICE recreation comes about exhibited that 1-bit comparator design indicates diminishment in power consumption and delay by 81% and 41.6%, individually, as for its partner figured it out in view of the design procedure.

Nepal K. exhibited CNTFET-construct dynamic ternary structure situated in light of finish display approach. Utilizing this procedure, they exhibited design of ternary inverter, cushion furthermore, MIN gate. These designs utilize two power supply voltages (V_{dd} and $V_{dd}/2$) and single diameter CNTFETs. HSPICE reenactment comes about demonstrated that ternary inverter indicates diminishment in PDP by

One request of size as for that of inverter design introduced**. Moaiyeri et al. [209]** introduced two designs of CNTFET-based ternary full snake. These designs use capacitor-based scaled simple summer alongside a ternary support. In the primary design, ternary cradle contains two fell ternary inverters in which initial one act as a limit locator and the second one work as a

standard inverter to get output from its supplement. In the second design, ternary cradle contains edge locator just to create Sum flag. The first design utilizes 5 capacitors and 24 transistors, and the second one contains 18 transistors and 5 capacitors, while ternary full snake designed utilizing falling of two half viper utilizes more than 200 transistors with one additional power supply. Be that as it may, in the primary design, there exist a long way between the info and output, and furthermore because of utilized capacitors, delay and power consumption are expanded. Albeit second design has all the more driving ability and less delay, it has more static power consumption contrasted with initial one. Aside from this, the two designs endure from low noise margin because of parasitic effect caused by utilized capacitors.

Ebrahimi et al.displayed a CNTFET-based ternary full viper which contains two fell half snake squares to create output Sum. The purported half snake does not create last output Convey. A different sub-circuit is utilized to produce Carry. The displayed design uses 106 transistors including ternary inverters which give complementary info signals. HSPICE reproduction comes about showed lessening in PDP of introduced circuit by 61% and 85% contrasted with first and second designs of at 3 fF output stack. Be that as it may, this ternary full snake has low driving power because of its long basic way comprising of a few pass-transistors in arrangement.

Display Scenario

In 2013-2015, a few researchers exhibited ternary rationale based advanced circuits utilizing CNTFETs. For example, **Moaiyeri et al** built up a universal approach for implementing CNTFETbased ternary circuits with no static power dissipation. In this technique, the way from power supply (V_{dd}) to ground is killed in the static condition of the circuit which prompts impressive improvement in power consumption and vitality effectiveness. HSPICE reenactment comes about with 32 nm CNTFET model exhibited that these circuits get 82% decrease in static power consumption in correlation with that of ternary designs.

Vudadha et al.designed ternary half viper utilizing a blend of binary 2:1 multiplexer what's more, ternary 3:1 multiplexer. Reproduction comes about demonstrated 58% decrease in power and 64% lessening in PDP regarding ternary multiplexer based design. **Sridevi et al.**acknowledged ternary combinational circuits including half snake, half subtractor, full snake, full subtractor and 2-bit comparator, in light of invalidation of literals procedure. These circuits

were assessed utilizing HSPICE test system with CNTFET model. The revealed comes about managed 5–145 times improvement in PDP with less gate tally as for ternary– binary combinational gate designs.

Mirzaee et al.executed a ternary full snake on the premise of falling two half viper squares to create Sum and, a convey generator to deliver Carry. In this design, resistors and capacitors, which were executed utilizing transistors, were used for voltage division. Creators likewise exhibited designs of ternary half viper and 4-bit ternary swell snake. HSPICE reenactment comes about showed improvement in delay and power consumption by 66% and 45%, separately, for ternary full snake in examination with its partner introduced at 0.7 V power supply voltage. Furthermore, it utilizes 46 fewer transistors contrasted with ternary full snake. Be that as it may, it experiences high power dissipation because of utilized resistors, and low noise margin due to utilized capacitors.

Keshavarzian et al.exhibited a CNTFET-based ternary full snake executed utilizing a Aggregate generator and a Carry generator. Each of these generators contain two draw up networks, two draw down networks and one resistive voltage divider configured utilizing transistors. This TFA uses 106 transistors in its realization. A ternary cradle was utilized for high driving capacity of TFA. HSPICE reproduction comes about demonstrated decrease in PDP by 82%, 93%, and 53%, contrasted with the first and second TFA designs and TFA, separately. **Sridharan et al.**showed CNTFET-based designs for single-trit and multi-trit adders. They introduced single-trit viper design with less intricate encoder and convey era unit (in correlation with designs. This design utilizes 142 transistors in its execution. For multi-trit design, creator's utilized single-trit viper hinders with lessened number of encoder and decoder obstructs (in examination with coordinate falling of single-trit adders). The introduced snake designs were reproduced in HSPICE with CNTFET model and gadget parameters. The announced outcomes showed 79% decrease in PDP for 3-trit viper what's more, 88% diminishment in PDP for 9-trit snake, in correlation with the entryway level designs. Be that as it may these designs contain an immediate way amongst Vdd and ground for some info mixes which brings about high static power consumption.

Next, **Panahi et al.** created two designs of ternary half subs tractor in view of CNTFETs. The main design depends on complementary CNTFET design style with resistive voltage divider configured utilizing transistors. It utilizes 42 transistors including ternary inverters for

supplements of inputs. The second design utilizes transmission gates and decreases number of transistors to 18. These designs were recreated in HSPICE with CNTFET model. It was demonstrated that the second design gets 400% improvement in PDP as for that of first design.

2.4 Content Addressable Memory (CAM) Cell

A substance addressable memory (CAM) is an application particular memory that thinks about info look information against put away information, and returns the address of coordinating information, inside one single clock cycle which makes it quicker than other programming and hardware look frameworks. There are two sorts of CAMs: binary CAM (BCAM) and ternary CAM (TCAM). Binary CAM (BCAM) stores rationale 0 and rationale 1. It performs correct match looks and subsequently, it is valuable for tag correlation in store memory. Ternary CAM (TCAM) gives an additional adaptability of example coordinating with the utilization of couldn't care less (X). It stores and scans for a X esteem alongside rationale 0 also, rationale 1. This X esteem gives special case passage where memory cell demonstrate a match independent of information bits. This element makes TCAMs mainstream for acknowledging organizing applications, for example, bundle sending and parcel grouping in arrange routers.

2.4.1 CAM Cell in view of MOSFET

The main BCAM cell alluded as PMOS-commanded diode cell was depicted by Koo in 1970. This cell contains two NMOS transistors and seven PMOS transistors including one diode associated PMOS for coordinate line pull up. In this cell, bit-line stack is information subordinate which leads to flighty read and compose delays. Also, the diode based match-line pull up prompts slower seek operation, and draw up current gave by bit lines instead of a hard supply makes buffering and electro movement concerns. **Kadota et al.** introduced a 10T dynamic pulldown cell. This cell contains eight NMOS transistors and two PMOS transistors. It settle the troubles confronted by diode-based cell: bit-line stack is information free and the match line pull-down happens through a dynamic system associated with a hard supply. In this cell, bit line state amid coordinate line precharge has the inverse extremity from that of read/compose precharge, which brings about expanded pursuit process duration. This cell likewise experiences charge-sharing issue. Enhanced 10T dynamic draw down cell was shown by **Uvieghara et al.** This cell settle charge sharing issue by swapping of transistors in its XOR based correlation rationale

parcel however the issue of contrariness with bit line states still remains. Bergh et al. gave a 9T cell committed inquiry lines in triple-metal process. These additional lines offer a few points of interest. Bit line loads are information autonomous. The conditions of match line are autonomous from perused/compose movement. Bit lines and inquiry lines have decreased load in correlation with them where a solitary combine is utilized. As a result, the introduced cell prompts rapid and low power consumption regarding that of above portrayed cells. Also, read and inquiry operations can be completed in parallel, which brings about expanded handling throughput by a factor of two. In any case, this cell requires more extensive draw down transistor.

Miyatake et al.displayed a 9T CAM cell with PMOS as a bit-coordinate gadget. This match gadget causes lessened voltage swing in pulling down the match line, in correlation with NMOS pull-down. As an outcome, the introduced cell finds littler match line charging and releasing streams, lessened noise level, and lower power consumption (all roughly by 40%) in examination with traditional 9T cell. In any case, the PMOS-based coordinate line pull-down driver is powerless in driving down the word coordinate line for befuddle case in correlation with NMOS-based driver.

Liu et al. built up a low-voltage 12T CAM cell with a quick tag-analyze ability, based on in part exhausted SOI CMOS dynamic edge methods. Notwithstanding ten transistors utilized as a part of customary cell, this cell utilizes two additional pass transistors for powerfully controlling of the collections of transistors in think about system. As per comes about acquired by MEDICI test system program, it is 45% speedier than that of traditional 10T cell, at supply voltage of 0.7 V.

Thirugnanam et al.presented a 9T flipping match line CAM. They utilized one extra wire called as dynamic high/dynamic low flag (AHAL) which is shared between two neighboring columns, contrasted with an essential cell. The displayed cell interchanges between dynamic high and dynamic low output in each entrance with AHAL flag which is turned ON in substitute cycle to locate the dynamic state of the match line. Reenactments were performed in HSPICE utilizing 0.25 µm CMOS innovation.The announced outcomes exhibited that the introduced cell demonstrates 40% lessening in power consumption over read misses because of decreased

exchanging movement in coordinate lines significantly, in correlation with particular precharge CAM cell and altered CAM cell.

Mundy et al.showed the principal dynamic 5T BCAM cell in light of PMOS devices in1972. This cell contains two 3T dynamic random get to memory (DRAM) cells associated back to back with one regular read get to gadget. In this cell, adequate charge stockpiling is not accomplished because of low estimation of entryway capacitance which contains an arrangement association of gate oxide capacitance and exhaustion layer capacitance.

Yamagata et al.displayed a dynamic 5T cell with DRAM-sort capacitors. This cell employments NMOS devices and plays out all operations with complementary signs with reference to PMOS based cell. It accomplishes genuine differential charge stockpiling however the related DRAMtype capacitors are hard to create and infrequently accessible to ASIC designer. Swim and Sodini showed a dynamic 5T cell which does not require progressed Measure fabrication strategies for settling charge stockpiling issue. This cell uses crosscoupled association of bit lines. At the point when composes are played out, the capacity gadget is turned OFF; there is no arrangement association between the exhaustion capacitance and entryway capacitance, and adequate charge stockpiling is acquired. The exhibited cell performs quick read and inquiry operation as for its partner introduced. Dynamic cells need invigorate operation, and have information reliance of bit line loads. Jones introduced an 8T dynamic lock cell in light of 4T-DRAM. Despite the fact that this cell require more range contrasted with the 3T-DRAM based cells, its realization and operation system are considerably more straightforward. This cell accomplishes completely differential information stockpiling with positive input hooking, and good with standard SRAM read/compose peripherals. Be that as it may, it experiences coordinate line charge sharing issue.

Pagiamtzis et al.depicted a 16T TCAM cell with NOR-based examination rationale. This cell utilizes two 6T SRAM cells for information stockpiling and four NMOS transistors for bit examination. It gives a full swing voltage at the gates of examination transistors and prompts quick match operation. Roth et al. introduced an altered variant of this cell. They have utilized PMOS devices rather than NMOS devices for examination circuitry, which empowers a more minimal design by lessening the quantity of dividing of n-dissemination to p-dispersion in the cell. Furthermore, the altered cell diminishes wiring capacitance and in this manner prompts low

power consumption. Yet, the cell has eased back inquiry operation because of high identical resistance related with correlation transistors.

Arsovski et al.announced a 12T TCAM cell with NAND-sort look at rationale. These cell employments deviated 4T static cells for information stockpiling and four NMOS transistors for think about system. A topsy-turvy game plan of capacity cell contains a hard node which stores full rail voltage signals. The recorded cell range is 17.54 μm2 which is practically identical with that of customary BCAM cell; thusly the displayed cell gives ternary execution with no cost. **Choi et al.** introduced a 16T TCAM cell with NAND-sort look at organize. This cell uses two 6T SRAM stockpiling cells and four NMOS think about transistors. This cell demonstrates low power attributes yet experiences high inquiry delay in correlation with TCAM.**Sultan et al.**showed a 12T TCAM cell. This cell contains two lopsided 4T information capacity cells and one correlation circuit in light of low capacitance look rationale. This examination rationale decreases coordinate line capacitance (by half or 75% relying upon all inclusive conceal bits in seek information) in correlation with that of NOR examination rationale based TCAM cell. The format of introduced cell, which was attracted Cadence Virtuoso with UMC 0.13 μm innovation, involves 12.93 μm2. **Mohan et al.** showed the appropriateness of 5T-SRAM cells for regular TCAM cells to diminish leakage and cell range. They likewise proposed NMOS coupled 14T TCAM and PMOS coupled 14T TCAM, which utilize unused condition of regular TCAM for further lessening in cell leakage by eliminating one of the sub-edge leakage ways. PTM recreation comes about exhibited that the displayed cells indicate 40% diminishment in leakage with littler degradation (< 8%) in static noise margin (SNM) over the ordinary TCAM cell. The

Detailed outcomes likewise exhibited that these cells takes 3.6 nS (most extreme) for read and compose operations.

Kumar et al.revealed a 16T-TCAM cell with coordinate line testing circuitry in 180 nm innovations. In this cell, a system which contains a transmission gate and a capacitor, neither is included with the current ternary NOR cell to check the veiling condition amid the inquiry operation. It is demonstrated that match line conditions have been tried effectively and the resultant outputs are in agreement with fancied ones.

Fries et al.gave a dynamic TCAM coupled match line. This cell utilizes four Ntype transistors, and plays out each of the three essential operations: match, read and compose. The match line in the cell is combined with one of the cell transistor bringing about long coordinating delays. Creators moreover exhibited a match line slice off plan to manage the coupling effects. Valerie et al. detailed a dynamic TCAM cell which utilizes six NMOS transistors and two DRAM-sort capacitors. In this cell, coordinate line pull down gadget which is controlled by the cell node, was secluded from coupling of match line with a specific end goal to expand the speed of match line release. Noda et al. proposed a planer dynamic TCAM created in 130 nm CMOS innovation. This cell contains eight NMOS transistors and four planer capacitors. These capacitors are masterminded in two complementary sets which enhances steadiness of TCAM. Likewise, this planer dynamic idea prompts a little cell zone of 4.79 µm2 which is roughly 50% of the SRAM based TCAM cell executed in a similar innovation. Noda et al. additionally proposed a cost-effective dynamic TCAM actualized in 130 nm implanted DRAM innovation. This cell comprises of six NMOS transistors and two capacitors. It utilizes double oxide process for the dependability of information maintenance and quick inquiry operation. The exhibited cell prompts little zone of 3.59 µm2 , which is 47% not as much as that of ordinary static TCAM and 25% not as much as that of dynamic TCAM introduced in [240], both created in 130 nm CMOS innovation, Additionally, it prompts low power consumption and littler noise level because of low capacitance of inquiry lines what's more, coordinate lines. Alongside these favorable circumstances, bigger capacity node capacitance (30fF) increments its delicate blunder resistance level and power.

Frias et al.presented five decoupled dynamic TCAM cells. They arranged these cells in light of the quantity of transistors utilized. The exhibited cells contain six, six-and-a-half, seven also, a-half, and ten-and-a-half transistors (one transistor is shared between two adjoining cells).These cells prompt shorter coordinating delay because of decoupling of match lines from cell transistors. For assessment, they were recreated utilizing 0.25 µm CMOS innovation and thought about with the dynamic cells introduced. Among all cells, 7.5-T DDCAM accomplishes shorter coordinate delay (89.7 pS). So also, 6-T DDCAM cell gets the littlest match delay-current product which is 33% of that of different cells.

2.4.2 CAM Cell in view of CNTFET

Design of quick and smaller CAM structure is of most noteworthy need and ballistic transport operation what's more, low off current make CNTFET a reasonable gadget for elite and expanded integration thickness of CAM design. This memory performs parallel information examination with information capacity. It comprises of SRAM cells for information stockpiling and a look at arrange for information correlation. Utilizing CNTFETs, diverse designs of SRAM cell have been proposed in the literature for binary also, ternary stockpiling. **Bachtold et al.**introduced a resistive-stack CNTFET-based SRAM cell. Be that as it may, this cell needs huge off-chip resistors (100 Mω) which bring about high power dissipation and expanded cell territory. To address this issue, **Lin et al**.built up a resistor-less CNTFET-based SRAM cell which utilizes P-CNTFET as dynamic load. This design utilizes two unique diameters for P-CNTFET and N-CNTFET. Creators additionally presented a metric called as "SPR" (static power-noise margin product to power-delay-product proportion) to catch diverse figures of legitimacy including dependability, power consumption and compose time. The exhibited cell was mimicked in HSPICE utilizing the Stanford CNTFET model and the Berkeley Prescient 32 nm CMOS model to perform correlation with its CMOS partner.

Recreation comes about demonstrated that SPR of the cell is four times higher than its CMOS partner having a similar design. The detailed outcomes likewise showed safety to process, voltage and temperature varieties concerning CMOS SRAM cell. Kim et al exhibited a CNTFET-based 8T SRAM cell. This design separates the criticism circle of the two consecutive inverters of 6T SRAM structure amid compose operation what's more, isolates the compose and read bits with 8T design. Amid compose operation, the exhibited strategy decreases number of release and limits dynamic power consumption.

HSPICE reenactments were performed with the Stanford CNTFET model and the Berkeley Predictive 32 nm CMOS model. Contrasted with 6T CMOS SRAM cell, the exhibited 8T cell demonstrates 48% decrease in unique power consumption with 56% more extensive SNM at the cost of 2% and 3% expansion in leakage power and compose delay, separately. You and Nepal announced two design of ternary SRAM cell; one uses 14 transistors and different uses 8 transistors. The main design utilizes six-transistor based ternary inverters, and the second design utilizes three-transistor based ternary inverters with one additional power supply ($V_{dd}/2$). In these

designs, CNTFETs with various diameters are used. Flavor recreations demonstrated that 8T ternary cell has more power consumption than 14T ternary cell. It was likewise illustrated that the delay of the two designs is equivalent, and there exist an exchange off amongst power and territory for settling on a decision in the middle of these two designs.

Lin et al.introduced a CNTFET-based ternary memory cell. This cell utilizes a transmission entryway for compose operation, and a cushion alongside another transmission gate for read operation. Two consecutive six transistors-based ternary inverters were utilized for ternary information stockpiling. The exhibited cell disposes of the need of additional power supply voltage by making the utilization of CNTFET chirality vectors for edge voltage control. This cell gets high SNM because of independent read andcomposes operations, and 90% lower standby power consumption as for customary binary CMOS cell. The revealed cell additionally demonstrates 41.6% range sparing contrasted with that of its CMOS ternary partner at 32 nm.

Das et al.assessed the execution of a CNTFET-based 4-bit binary CAM (BCAM) cluster. They put four 8T NOR-sort BCAM cells in parallel to shape this exhibit. Recreations were performed in HSPICE with Stanford CNTFET model. Creators utilized current race coordinate line detecting intensifier to show coordinate line conditions. The announced outcomes exhibited that the introduced CAM cluster demonstrates 2-4 times speed improvement with 17.4% power sparing with regard to its CMOS partner.

Nepal and You built up a substitute design of CNTFET-based TCAM cell (i.e. 3CAM) utilizing genuine three esteemed structures. To start with, they showed CNTFET-based 8T NOR-sort BCAM cell. This cell utilizes 6T SRAM cell for information stockpiling and, four N-CNTFETs shaping match pull-down system for analyze rationale. Besides, they neither portrayed CNTFET-based 16T TCAM cell with NOR based look at rationale. This cell contains two 6T SRAM cells furthermore, four think about transistors. It needs extra territory because of utilization of two stockpiling cells. To address this issue, creators detailed a 3CAM cell which has an indistinguishable ease of use from TCAM. The exhibited 3CAM cell utilizes a ternary memory cell for information stockpiling and does not require a second binary SRAM which is utilized as a part of TCAM structure. HSPICE reenactment comes about shown that 3CAM cell has 1.61 nS look delay which is tantamount to that of TCAM cell, and 2.29 µW power consumption which is

higher than TCAM cell having power consumption of 1.26 µW. The exhibited 3CAM cell demonstrates 25% zone sparing over TCAM cell.

2.5 Research Gaps and Scope of the Presented Work

In view of the literature survey done in past area, the accompanying issues have been considered and tended to:

1. Research work in the territory of advancement of ternary rationale and arithmetic circuits utilizing CNTFETs is insignificant for reduced VLSI sub-framework. Hardware advancement of such designs at architecture and circuit level is one of the issues tended to in this theory.

2. Investigation of the utilization of CNTFET for vitality productive ternary sub-framework is constrained. Design space of speed and power enhanced ternary circuit in view of CNTFET has been taken up in the displayed work.

3. Less work has been done in the range of building CAM structures utilizing CNTFETs for constant applications. There is a requirement for designing of CAM circuits in light of CNTFET.

Chapter 3

Design of 2-bit Hardware Optimized Ternary ALU (HO-TALU) utilizing CNTFETs

3.1 Introduction

An ALU is one of the primary parts inside focal preparing unit (CPU) of a computerized PC, and even it is found inside the most straightforward microprocessors additionally, where it is in

charge of performing arithmetic and rationale operations. The expanding interest for profoundly enhanced current data handling framework obviously indicates the need of proficient usage of ALU as far as power, speed and hardware. This part shows design of 2-bit hardware enhanced ternary ALU (HO-TALU) utilizing CNTFETs. 2-bit HO-TALU gets minimization in required hardware at both engineering as well as at circuit level. At architecture level, HO-TALU has another viper subtractor (AS) module which performs both expansion and subtraction operations utilizing a snake module as it were with the assistance of multiplexers. Therefore, it kills a subtractor module from the customary architecture. At circuit level, HO-TALU limits ternary capacity articulations in examination with work minimization proposed. Moreover, it uses binary entryways alongside ternary gates in realization of utilitarian modules: AS, multiplier, comparator and selective OR. HSPICE reproduction comes about demonstrate that multiplier, comparator and selective OR have advantage in power-delay product (PDP) yet AS has a minor misfortune in PDP. As a result, HO-TALU gets noteworthy decrease in gadget include with marginally increment PDP for expansion and subtraction operations just in examination with CNTFET-based ternary designs accessible in the literature. Design of 2-bit HO-TALU is changed to build up a 2-bit HO-TALU cut which could be effectively fell to develop N-bit HO-TALU.

In area 3.2, designs of ternary gates are illustrated. Architecture and elements of HOTALU are exhibited in area 3.3. Segment 3.4 gives ternary capacity minimization and realization, and area 3.5 and 3.6 clarify design of HO-TALU useful modules and their integration over TALU cut, separately. In area 3.7, transient recreation comes about for useful test and execution assessment are given hardware assessment, trailed by the conclusion in Section 3.8.

3.2 Design of Ternary Logic Gates

Ternary rationale is a sort of multi-esteemed rationale, which increases the value of the ordinary binary rationale. Table 3.1 demonstrates the meaning of ternary rationale states signified by 0, 1 and 2 and their proportionate voltage levels. A variable ternary capacity f (a1, a2… an) is a rationale work which is mapped on {0, 1, 2} n to {0, 1, 2}. The essential ternary operations (AND, OR and NOT) are characterized as takes after

$$a_1.a_2.a_3 \ldots\ldots\ldots a_n = \min(a_1, a_2, a_3 \ldots\ldots\ldots a_n)$$

$$a_1 + a_2 + a_3 \ldots\ldots\ldots a_n = \max(a_1, a_2, a_3 \ldots\ldots\ldots a_n)$$

$$\bar{a}_n = 2 - a_n \qquad \textbf{(3.1)}$$

Where a1, a2, a3 …an = {0, 1, 2}, - denotes arithmetic subtraction and operators ·, +, ¯, denotes ternary AND, OR and NOT operations, respectively. The most fundamental building blocks of ternary system are NOT (or inverter), NAND and NOR gates. These gates operate according to their respective convention provided by eq. (3.1).

Table 3.1: Definition of logic states in ternary logic

Logic states	Voltage Level (V)
0	0
1	0.45 (V_{dd}/2)
2	0.9 (V_{dd})

There are three types of inverters, namely positive ternary inverter (PTI), negative ternary inverter (NTI) and standard ternary inverter (STI), which are defined as follows.

$$NOT_k(a) = \begin{cases} 2 - a & \text{if } a \neq 1 \\ k & \text{if } a = 1 \end{cases} \qquad \textbf{(3.2)}$$

In eq. (3.2), "a" will be a ternary info flag; variable k is 0 for NTI, 1 for STI, and 2 for PTI. The truth table of ternary inverters is appeared in Table 3.2. Like ternary inverters, there could be three sorts of ternary NAND and NOR entryways.

Table 3.2: Truth Table of ternary inverters

a	NTI	PTI	STI
0	2	2	2
1	0	2	1
2	0	0	0

A two-input ternary NAND and NOR gate having inputs ‘a’ and ‘b’ are defined as follows.

$$NAND_k(a,b) = \begin{cases} 2 - \min(a,b) & \text{if } \min(a,b) \neq 1 \\ k & \text{if } \min(a,b) = 1 \end{cases} \quad \textbf{(3.3)}$$

$$NOR_k(a,b) = \begin{cases} 2 - \max(a,b) & \text{if } \max(a,b) \neq 1 \\ k & \text{if } \max(a,b) = 1 \end{cases} \quad \textbf{(3.4)}$$

According to eq. (3.3) and (3.4), depending upon the logic value of variable k i.e. 0, 1 and 2, a ternary NAND/NOR gate will operate as a negative ternary NAND/NOR (NTNAND/NTNOR) gate, standard ternary NAND/NOR (STNAND/STNOR) gate and positive ternary NAND/NOR (PTNAND/PTNOR) gate, respectively. Table 3.3 gives truth table of ternary NAND and NOR gates. Further, designs of ternary logic gates presented are used in this work. These gates use complementary CNTFET logic style and unique feature of CNTFET for threshold voltage adjustment without using multiple power supply voltages.

Table 3.3: Truth Table of ternary NAND and NOR gates

a	b	NTNAND	PTNAND	STNAND	NTNOR	PTNOR	STNOR
0	0	2	2	2	2	2	2
0	1	2	2	2	0	2	1
0	2	2	2	2	0	0	0
1	0	2	2	2	0	2	1
1	1	0	2	1	0	2	1
1	2	0	2	1	0	0	0
2	0	2	2	2	0	0	0
2	1	0	2	1	0	0	0
2	2	0	0	0	0	0	0

Figure 3.1 shows schematic outline and image of NTI, where D speaks to diameter of CNTFET. Design of NTI utilizes low edge N-CNTFET (T1) and high edge P-CNTFET (T2). At the point when input voltage (V_a) is 0 V, T1 is killed and T2 is turned ON, and output is pulled up to 0.9 V. As V_a changes to 0.45 V or 0.9 V, T1 is turned ON and T2 is killed, what's more, output is released to 0 V. The operation of NTI affirms its entrances of Table 3.2.

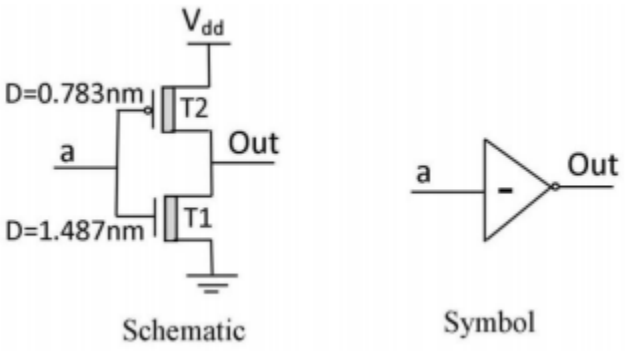


Figure 3.1: Negative ternary inverter (NTI)

Figure 3.2 shows schematic graph and image of PTI. This design of PTI utilizes high limit N-CNTFET (T3) and low edge P-CNTFET (T4). At the point when input voltage (Va) is 0 V or 0.45 V, T3 is killed and T4 is turned ON, and output is pulled up to 0.9 V. As Va changes to 0.9 V, T3 is turned ON and T4 is killed, and output is released to 0 V. The operation of PTI affirms its entrances given in Table 3.2.

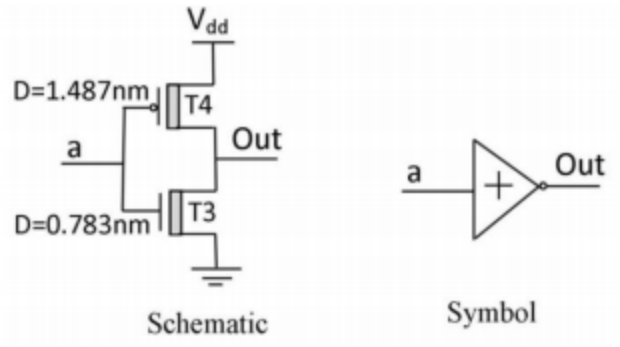


Figure 3.2: Positive ternary inverter (PTI)

Figure 3.3 shows schematic diagram and symbol of STI. STI is realized by combining NTI and PTI circuits through a network which contains one P-CNTFET (T5) and one N-CNTFET (T6) having same geometries. Consequently, output voltage (Vout) is obtained as the average value of output voltage of NTI (V_{out_N}) and PTI (V_{out_P}), which is represented as follows

$$V_{out} = \frac{(V_{out\_N} + V_{out\_P})}{2} \quad \textbf{(3.5)}$$

When the input voltage (V_a) is 0 V, both Vo_{ut_N} and V_{out_P} are 0.9 V and consequently V_{out} is 0.9 V. Similarly, when V_a = 0.9 V, both V_{out_N} and V_{out_P} are 0 V and consequently V_{out} is 0 V. Finally, when Va = 0.45 V, V_{out_P} and V_{out_N} are 0.9 V and 0 V, respectively and consequently, V_{out} is 0.45 V. Further, based on eq. (3.3), (3.4) and described method of designing ternary inverters, CNTFET-based STNAND/STNOR gates are implemented. Figure 3.4 and 3.5 show the schematic diagram and symbol of these gates, respectively.

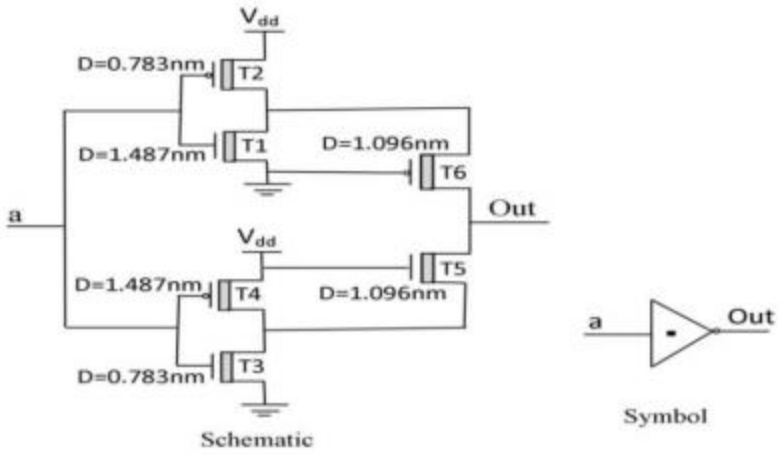


Figure 3.3: Standard ternary inverter (STI)

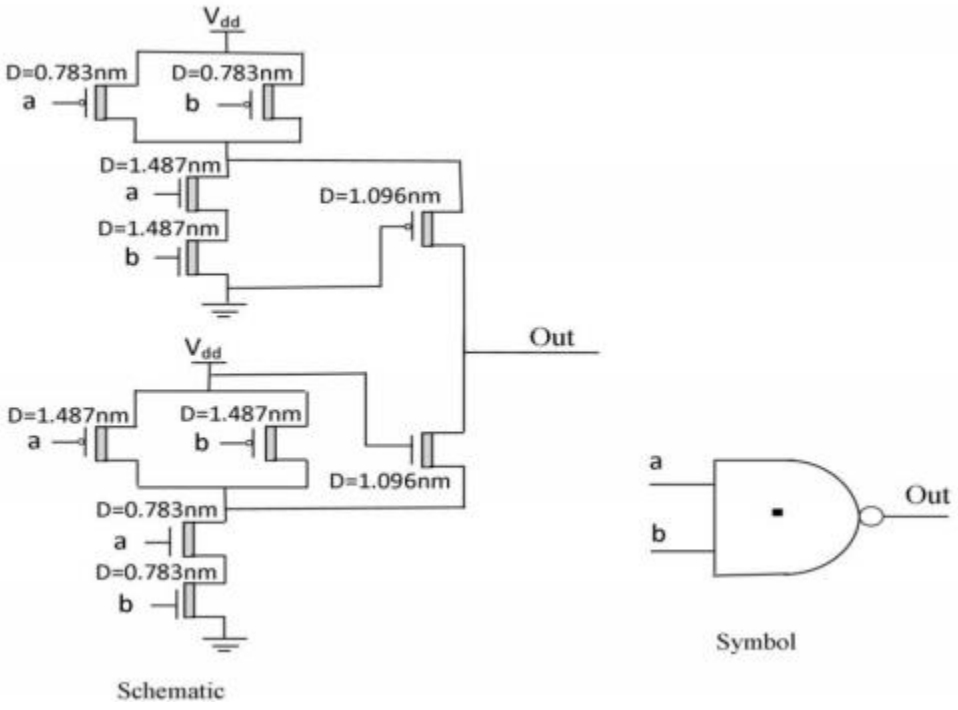


Figure 3.4: Standard ternary NAND (STNAND) gate

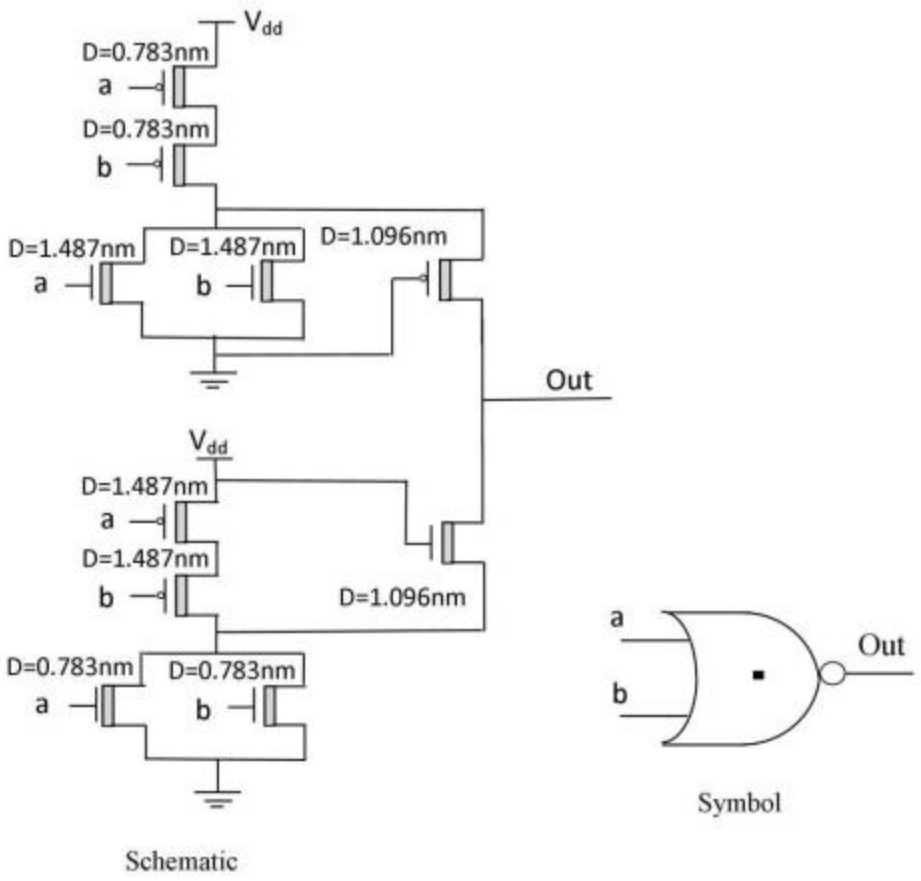


Figure 3.5: Standard ternary NOR (STNOR) gat

3.3 Architecture and Functions of 2-bit HO-TALU

Figure 3.6 demonstrates the stick graph and architecture of 2-bit HO-TALU. There are two ternary information inputs An (A_1 A_0) and B (B_1 B_0), and different outputs: Sum/Difference and Carry/Borrow, Product and C_{out}, GR, EQ and LE, and diverse rationale outputs, for example, A+B, $\bar{}$A+B, and A.B$\bar{}\bar{}$. Two select sources of info (S1 and S0) select craved rationale and arithmetic operation, as portrayed in Table 3.4. HO-TALU is equipped for giving four arithmetic operations and five rationale operations. The arithmetic operations incorporate expansion, subtraction, duplication and examination. The rationale operations incorporate AND, NAND, OR, NOR and XOR. The architecture of HO-TALU comprises of the accompanying fundamental segments: 1-to-3-line decoder, work selection rationale obstruct with dynamic high outputs (FSB-AHO), transmission gate hinder with dynamic high empower (TGB-AHE) and

distinctive useful squares (alluded as modules) which incorporate AS, multiplier, comparator, restrictive OR, T-OR, T-NOR, T and T-NAND. Terms "Bi" and "T" are utilized to demonstrate binary and ternary nature of rationale entryways, separately.

Table 3.4: Function Table of 2-bit HO-TALU

S_1	S_0	Function
0	0	Addition
0	1	Subtraction
0	2	Multiplication
1	0	Comparison
1	1	OR
1	2	NOR
2	0	AND
2	1	NAND
2	2	XOR

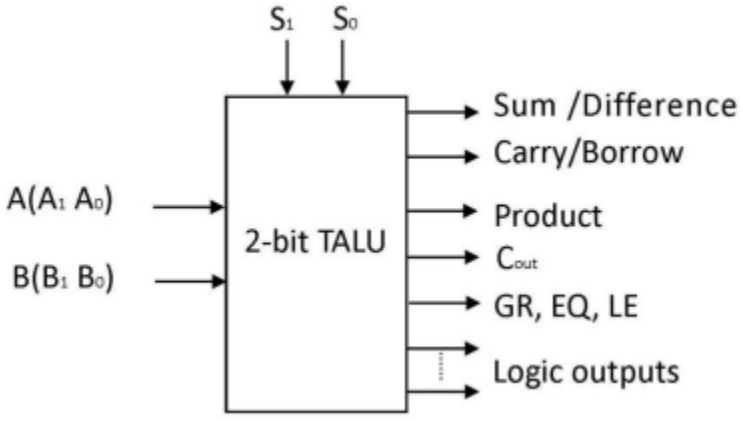


Fig. 3.6a: Pin out diagram of 2-bit HO-TALU

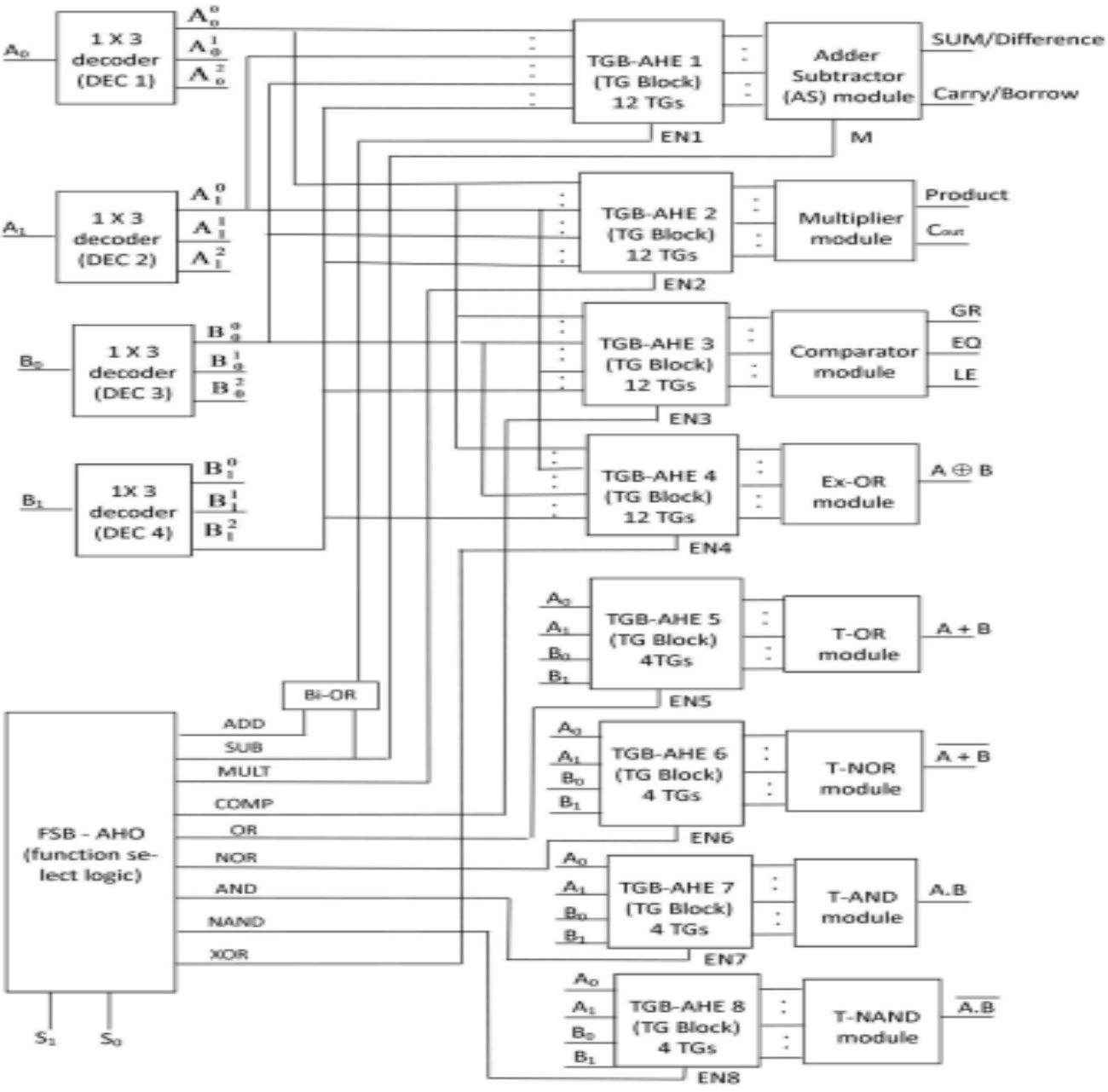


Fig. 3.6b: Architecture of 2-bit HO-TALU

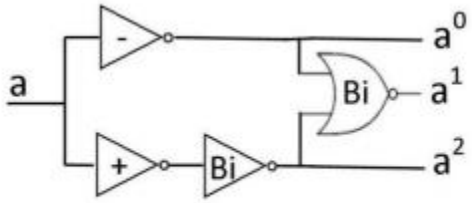
1-to-3-line Ternary Decoder

Figure 3.7 shows logic diagram of 1-to-3-line ternary decoder and its truth table. It is a one-input, three-output combinational circuit that generates three unary functions for an input 'a' as a^0, a^1 and a^2. This design uses NTI to produce a 0, PTI followed by a binary inverter to neither

generate a ^{2}, and a binary NOR gate having inputs a ^{0} and a ^{2} to produce a $^{1.}$ The logic response of a decoder is given as:

$$a^{c} = \begin{cases} 2 & \text{if } a = c \\ 0 & \text{if } a \neq c \end{cases} \qquad \textbf{(3.6)}$$

Where variable c takes 0, 1 and 2. In Figure 3.6 (b), decoder (DEC1) generates unary functions A_0^0, A_0^1 and A_0^2 for A_0, DEC2 generates A_1^0, A_1^1 and A_1^2 for A_1. Similarly, decoder DEC3 generates B_0^0, B_0^1 and B_0^2 for B_0, and DEC4 generates B_1^0, B_1^1 and B_1^2 for B_1. These unary functions are fed to functional modules for desired outputs.



(a)

a	a^0	a^1	a^2
0	2	0	0
1	0	2	0
2	0	0	2

(b)

Figure 3.7: 1-to-3-line ternary decoder (a) logic level diagram (b) truth table

Capacity Select Logic Block with Active High Outputs (FSB-AHO) Figure 3.8 shows rationale chart of capacity select rationale hinder with dynamic high outputs (FSBAHO). It has two information sources S_0 and S_1, and nine outputs ADD, SUB, MULT, COMP, OR, NOR, Also, NAND and XOR. It contains a variety of nine binary AND entryways with two 1-to-3-line decoders (DEC1 and DEC2). DEC1 creates unary capacities S_0^0, S_0^1 and S_0^2 for S_0 Similarly, DEC2 generates unary functions S_1^0, S_1^1 and S_1^2 for S_1 these capacities are connected to AND entryways for a coveted output. FSB-AHO chooses one specific TALU work contingent upon the bit blend of S0 and S1, as depicted in Table 3.4.

Consider the case when

$S_1S_0 = 02$. S_1^0, S_1^1 and S_1^2 are 2, 0 and 0, respectively. Similarly, S_0^0, S_0^1 respectively.

Similarly

S_0^0, S_0^1 and S_0^2 are 0, 0 and 2, respectively.The third AND gate of the array having inputs S_1^0 and S_0^2 makes its output MULT high, while all other AND gates have one (or more) input equal to 0 which makes their outputs low. The high MULT further enables TGB-AHE2 for multiplication operation, as shown in Figure 3.6 (b). Thus, depending upon the logic state of S_0 and S_1, only one particular output of FSB-AHO block is active (high) for desired TALU function.

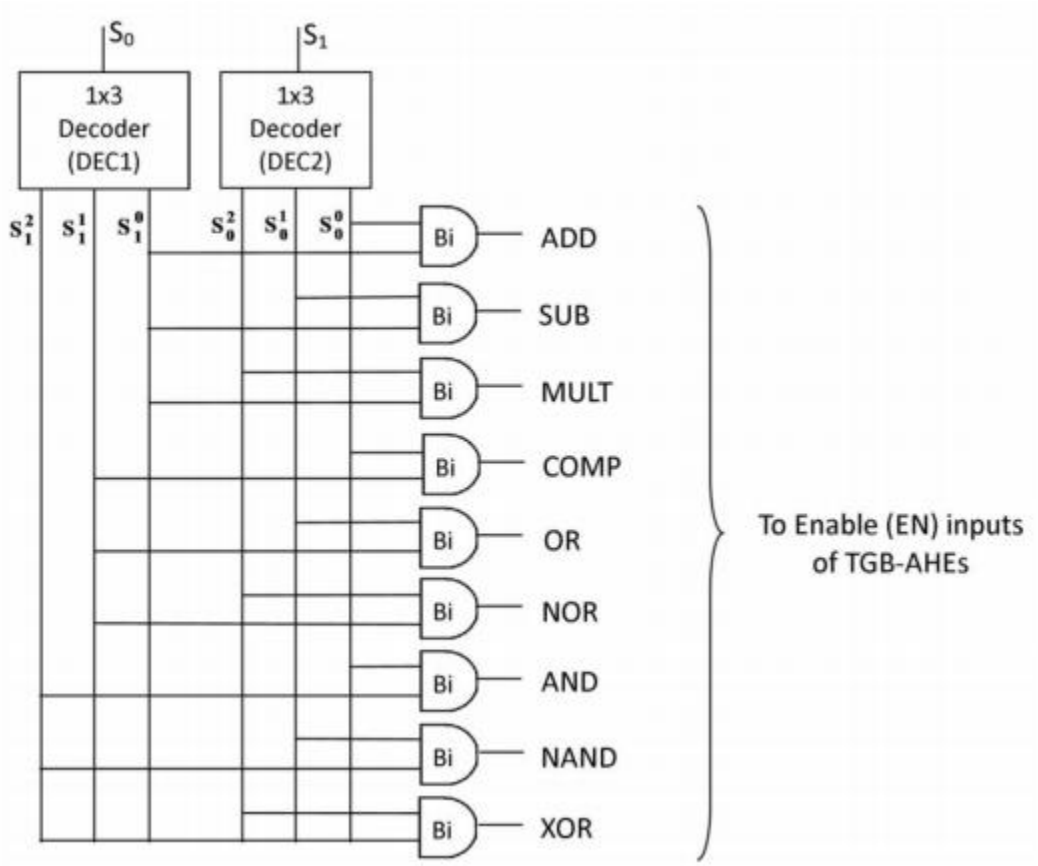


Figure 3.8: Logic level diagram of function selection logic block with active high outputs (FSB AHO)

Transmissions Gate Block with Active High Enable (TGB-AHE)

Figure 3.9 shows rationale level chart of transmission entryway obstructs with dynamic high empower (TGBAHE). It contains a variety of transmission entryways (TGs) which interface

decoder output lines to the information contributions of practical modules. This cluster is initiated when input empower (EN) is high. In Figure 3.6(b), the quantity of TGs utilized as a part of the cluster is specified with every individual TGBAHE. Further, TG is actualized utilizing the parallel association of P-CNTFET and N-CNTFET. In a TG cluster, N-CNTFET gate of all TGs is associated with EN and the entryway of all P-CNTFETs is associated with EN which is made by utilizing a binary inverter. At the point when EN is 2 (high), the N- CNTFET entryway is 0.9 V and the P-CNTFET gate is at 0 V, as an outcome, the two transistors direct and there is a shut way between input (I/P) and output (O/P). Likewise, when EN is 0 (low), the N-CNTFET gate is at 0 V and the P-CNTFET entryway is at 0.9 V, therefore both transistors are OFF and there is an open circuit between I/P and O/P. TGB-AHE gets estimation of EN from at least one outputs of FSB-AHO through either some rationale or, then again straightforwardly, as appeared in Figure 3.6(b). FSB-AHO outputs MULT, COMP, AND, NAND, OR, NOR and XOR are associated specifically to EN of the TGB-AHE2, TGB-AHE3, TGB-AHE4, TGB-AHE5 and TGB-AHE6, TGB-AHE7 and TGB-AHE8, individually. Since TGB-AHE1 is related with the AS practical module which performs expansion and subtraction, its empower input (EN1) must be high at whatever point one of these operations is craved. For this, a binary OR entryway is included with FSB-AHO. FSB-AHO outputs ADD and SUB are connected to this gate which produces EN1.

To exhibit the working of TGB-AHE, expansion operation is accepted. FSB-AHO makes its output ADD to high. Thusly binary OR entryway set EN1 to 0.9 V, which empowers TGBAHE1. This empowered square supplies decoder created unary elements of the contributions, to the AS module. This module performs expansion operation and produces SUM/Difference and Convey/Borrow outputs. Different modules stay segregated from information contributions because of low estimation of empower flag (EN) of their TGB-AHE.

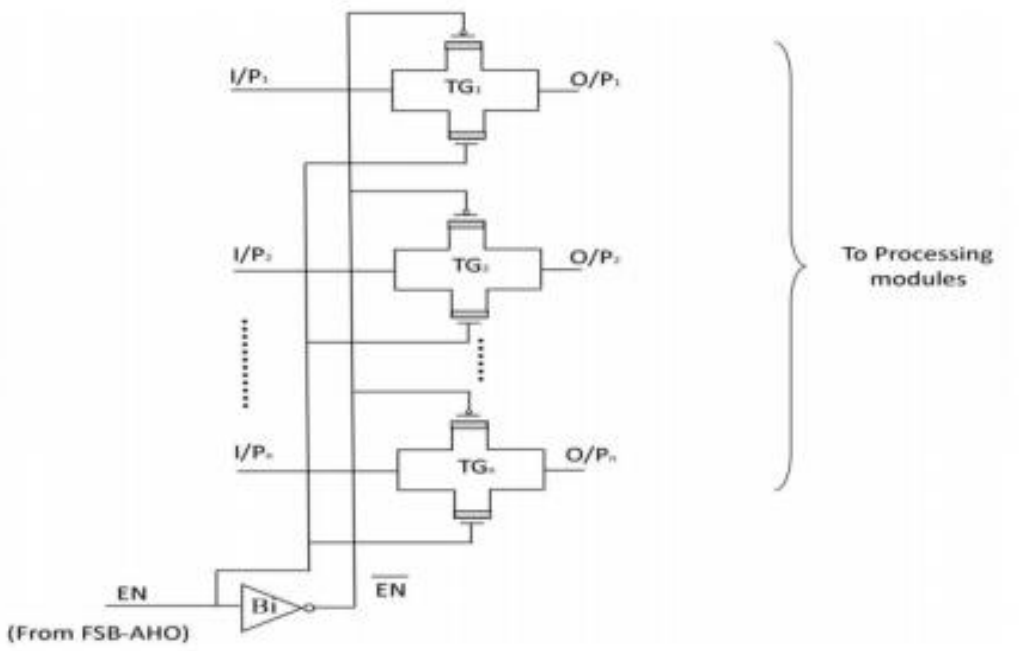


Figure 3.9: Logic level diagram of transmission gate block with active high enable (TGB-AHE)

3.4 Synthesis, Minimization and Realization of 2-bit HO-TALU Function

A ternary n-variable function F (a1, a2…an) is expressed in its canonical sum form as follows, based on theorem 1.

$$F(a_1,a_2.....a_n) = F_1(a_1,a_2,.....a_n)+1.\ F_2(a_1,a_2.....a_n) \quad \textbf{(3.7)}$$

Where F1 is a capacity which contains terms of 2's and F2 is a capacity which contains terms of 1's. As needs be, a ternary capacity can be orchestrated from its fact table. For the minimization of ternary capacities, there are three essential techniques:

1. Algebraic method

2. Tabular method

3. Ternary K-map method

In this work, ternary K-outline is utilized for work minimization. Further, the realization of limited ternary capacities is appeared in Figure 3.10. This usage strategy utilizes 1-to-3-line

ternary decoders for changing over ternary info signals (0, 1 and 2) into binary signals (0 and 2). These signs are prepared by a calculation unit containing binary rationale gates, and after that binary outputs are changed over once again into ternary outputs utilizing an encoder in light of ternary rationale gates.

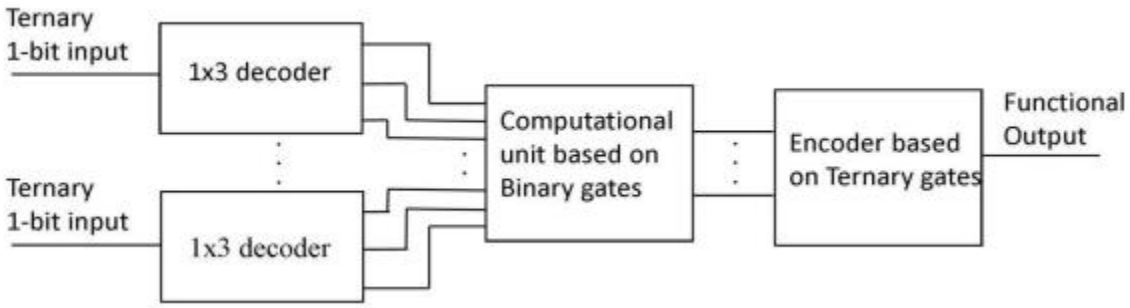


Figure 3.10: Ternary function implementation for 2-bit HO-TALU

The design methodology is as per the following:

1. Develop truth table and draw K-outline output factors.

2. Discover the exhibits (i.e. cell gathering) of 3 x 1, 3 x 2 and 3 x 3 cells with 2's terms and 1's terms. Cells with 2's term can be considered as couldn't care less for the development of exhibits with 1's terms. Create and limit the ternary capacity.

3. Understand the limited ternary capacity.

To expound synthesis, minimization and realization of ternary capacities, designing of a ternary half viper (THA) is clarified as takes after. Reality table of the THA is given in Table 3.5. The K-guide of outputs S0 (Sum) and C0 (Carry) are appeared in Figure 3.11.

Table 3.5: Truth table of ternary half adder (THA)

A	B	S_0 (Sum)	C_0 (Carry)
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

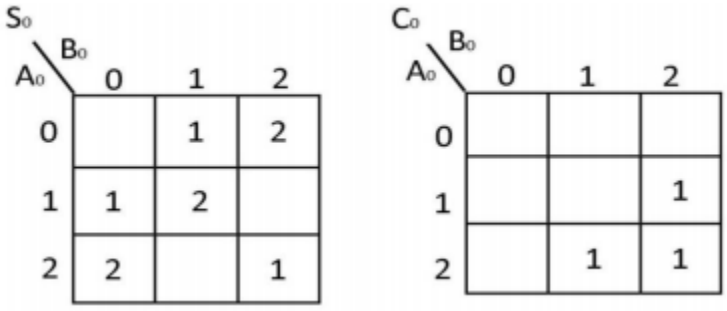


Figure 3.11: K-map of ternary half adder (THA)

From the K-maps, functions F1 and F2 are derived for S0 and C0. The simplified expressions of these variables are expressed as:

$$S_0(\text{Sum}) = F_1 + 1.F_2 = A_0^2B_0^0 + A_0^1B_0^1 + A_0^0B_0^2 + 1.(A_0^1B_0^0 + A_0^0B_0^1 + A_0^2B_0^2) \quad \textbf{(3.8)}$$

$$C_0(\text{Carry}) = F_3 + 1.F_4 = 0 + 1.(A_0^2B_0^1 + A_0^2B_0^2 + A_0^1B_0^2) \quad \textbf{(3.9)}$$

In case of THA, minimization by grouping of cells is not possible. Based on eq. (3.8) and (3.9), THA is implemented and shown in Figure 3.12. This implementation is taken from and used for this work.

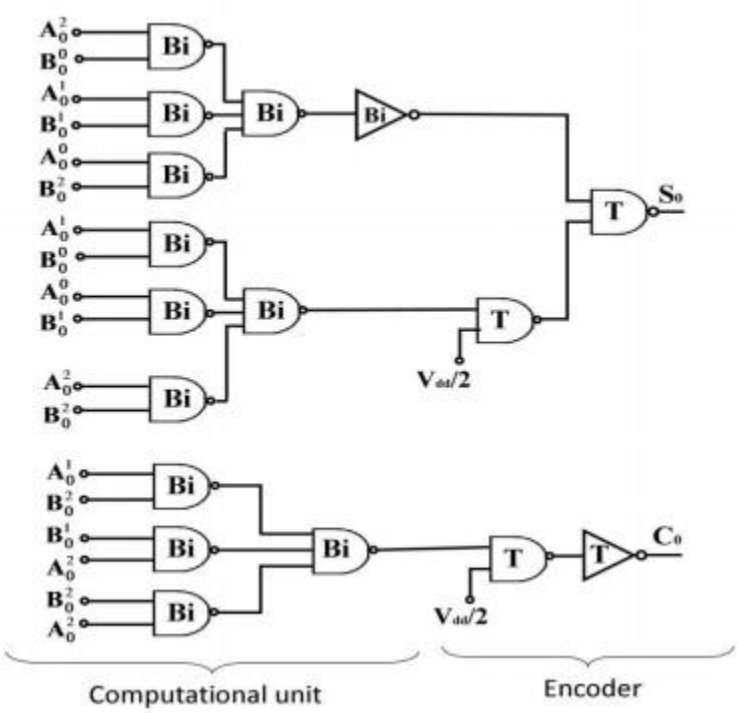


Figure 3.12: Logic level diagram of ternary half adder (THA)

3.5 Design and Implementation of 2-bit HO-TALU useful module

Design and usage of 2-bit HO-TALU useful modules including AS, comparator, multiplier, select OR, T-OR, T-NOR, T and T-NAND are portrayed in the accompanying sub-segments.

3.5.1 Adder-Subtractor (AS) Module

Figure 3.13 demonstrates the piece outline of the proposed AS module. It performs expansion and subtraction operations on An (A_1A_0) and (B_1B_0), which are spoken to by A+B and A-B, separately. AS module comprises of one half viper subtractor (HAS) piece and one full adder - subtractor (FAS) piece. A_0 and B_0 are included or subtracted utilizing HAS which produces outputs S_0/D_0 and C_0/B_0. This C_0/B_0 is gone through a 1-to-3-line decoder to create its unary capacities. At that point, these capacities are provided to FAS that includes or subtracts A1, B1

and C_0/B_0, and produces outputs S_1/D_1 and C_1/B_1. S_0/D_0 and S_1/D_1 speak to slightest noteworthy piece (LSB) and most huge piece (MSB) of Sum/Difference TALU output, and C_1/B_1 speaks to the Carry/Borrow TALU output. M is mode input which chooses the operation amongst expansion and subtraction. It is provided by SUB output line of FSB-AHO. Accordingly, when M = 0, AS performs expansion and for M = 2, it performs subtraction. Design of HAS and FAS squares are exhibited in the following sub-areas.

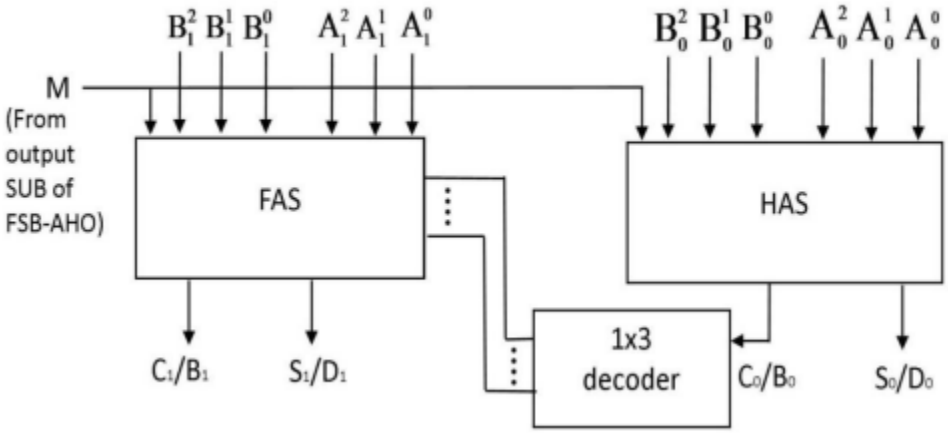


Figure 3.13: Logic level diagram of 2-bit ternary adder-subtractor (AS)

Half Adder-Subtractor (HAS) Block

The schematic outline of HAS square is appeared in Figure 3.14. It performs both expansion and subtraction operations utilizing one THA just with three multiplexers (MUXs), in view of the similitude in realization of THA and ternary half subtractor (THS). The execution of THA is exhibited in past (segment 3.4). For THS, utilizing its fact table given in Table 3.6, K-outline attracted and demonstrated Figure 3.15. From this K-outline, articulations of outputs

D_0 (Difference)andB0(Borrow)areinferredas:

$$D_0(\text{Difference}) = A_0^2 B_0^0 + A_0^1 B_0^2 + A_0^0 B_0^1 + 1.\ (A_0^1 B_0^0 + A_0^0 B_0^2 + A_0^2 B_0^1) \quad \textbf{(3.10)}$$

$$B_0(\text{Borrow}) = 1.\ (A_0^0 B_0^1 + A_0^0 B_0^2 + A_0^1 B_0^2) \quad \textbf{(3.11)}$$

Minimized expressions of output factors S_0 (Sum) and C_0 (Carry) of THA are given in eq. (3.8) and (3.9) in segment 3.4. In light of the eq. (3.8) and (3.10), articulation for D0 will be same as that of S0 if variable $B^1_0$is supplanted by B^2_0, and B^2_0 is supplanted by B^1_0. Likewise, as indicated by eq. (3.9) and (3.11), articulation for B_0 will be same as that of C_0 if variable A^0_0 is supplanted with A^2_0 Henceforth, a THA can deliver D_0 and B_0 likewise; having appropriate selection of information factors which is fulfilled utilizing MUXs as appeared in Figure 3.14. At the point when M = 0, MUX1, MUX2 and MUX3 select B^1_0, B^2_0 furthermore, A^2_0, separately, and HAS process the capacities given by eq. (3.8) and (3.9) for expansion operation. Essentially, when M = 2, MUX1, MUX2, MUX3 select B^2_0, B^1_0 what's more, A^0_0, individually, and HAS figures the capacities given by eq. (3.10) and (3.11) for subtraction operation. 51 Figure 3.14: Logic level outline

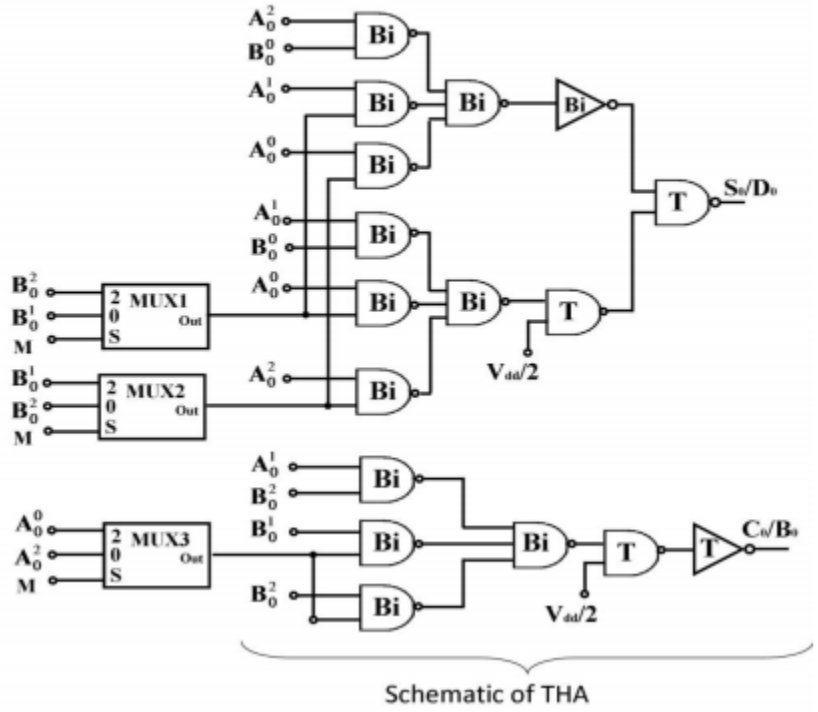


Figure 3.14: Logic level diagram of ternary half adder-subtractor (HAS)

Table 3.6: Truth Table of ternary half subtractor (THS)

A_0	B_0	D_0 (Difference)	B_0 (Borrow)
0	0	0	0
0	1	2	1
0	2	1	1
1	0	1	0
1	1	0	0
1	2	2	1
2	0	2	0
2	1	1	0
2	2	0	0

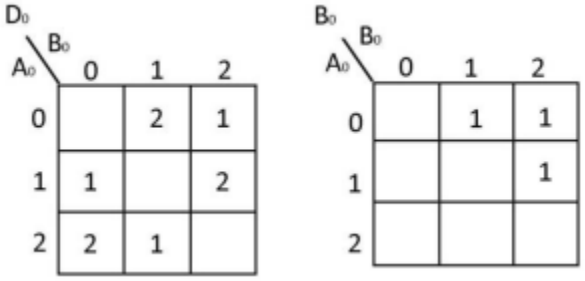


Figure 3.15: K-map of ternary half subtractor (THS)

In figure 3.16 It performs both addition and subtraction operations utilizing one ternary full viper (TFA) just with six MUXs, in view of the comparability in realization of TFA and ternary full subtractor (TFS). For TFA, utilizing its fact table given in Table 3.7, K-outline attracted and demonstrated Figure 3.17. From this K-outline, articulations of outputs S1 (Sum) and C1 (Carry) are inferred as takes after.

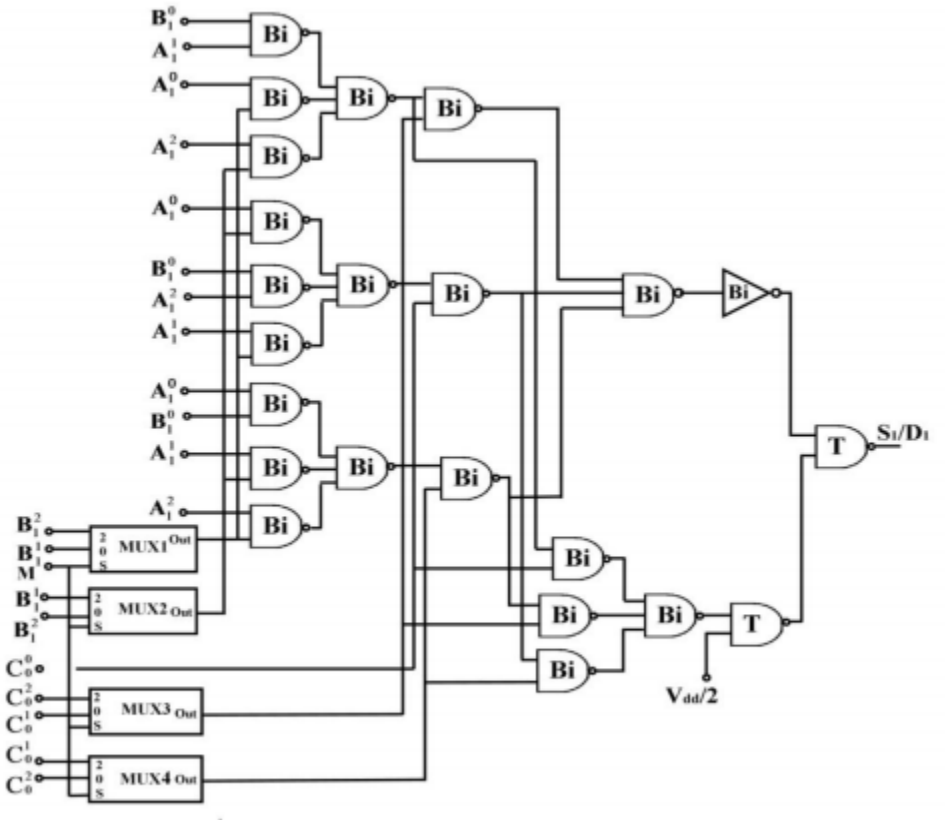
$$S_1(\text{Sum}) = C_0^0(A_1^0B_2^0 + A_1^1B_1^1 + A_1^2B_1^0) + C_0^1(A_1^1B_1^0 + A_1^0B_1^1 + A_1^2B_1^2) + C_0^2(A_1^0B_1^0 + A_1^1B_1^2 + A_1^2B_1^1) + 1.\{C_0^0(A_1^1B_1^0 + A_1^0B_1^1 + A_1^2B_1^2) + C_0^1(A_1^0B_1^0 + A_1^1B_1^2 + A_1^2B_1^1) + C_0^2.(A_1^2B_1^2 + A_1^1B_1^1) + C_0^2A_1^0B_1^0)\} \quad \textbf{(3.12)}$$

$$C_1\,(\text{Carry}) = A_1^2B_1^2 + C_0^2 + 1.\{C_0^0(A_1^1B_1^2 + A_1^2B_1^1 + A_1^2B_1^2 + C_0^1.(A_1^2B_1^2 + A_1^1B_1^1) + C_0^2\ \overline{A_1^0B_1^0}\}$$ **(3.13)**

Similarly, for THS, using its truth table given in Table 3.7, K-map is drawn and shown in Figure 3.18. From this K-map, simplified expressions of outputs D1 (Difference) and B1 (Borrow) are derived as:

$$D_1\,(\text{Difference}) = C_0^0(A_1^0B_1^1 + A_1^1B_1^2 + A_1^2B_1^0) + C_1^2\ (A_1^1B_1^0 + A_1^0B_1^2 + A_1^{21}B_1^1) + C_0^1(A_1^0B_1^0 + A_1^1B_1^1 + A_1^2B_1^2) + 1.\{C_0^0(A_1^1B_1^0 + A_1^0B_1^2 + A_1^2B_1^1) + C_0^2(A_1^0B_1^0 + A_1^1B_1^1 + A_1^2B_1^2) + C_0^1(A_1^0B_1^1 + A_1^1B_1^2 + A_1^2B_1^0)\}$$ **(3.14)**

$$B_1\,(\text{Borrow}) = A_1^0B_1^2 + C_0^2 + 1.\{C_0^0(A_1^1B_1^2 + A_1^0B_1^1 + A_1^0B_1^2 + C_0^1.(A_1^0B_1^2 + A_1^1B_1^1) + C_0^2\ \overline{A_1^2B_1^0}\}$$ **(3.15)**



Schematic of S1(Sum) generator of TFA

Figure 3.16 (a): Logic diagram of S1/D1 generator of ternary full adder-subtractor (FAS)

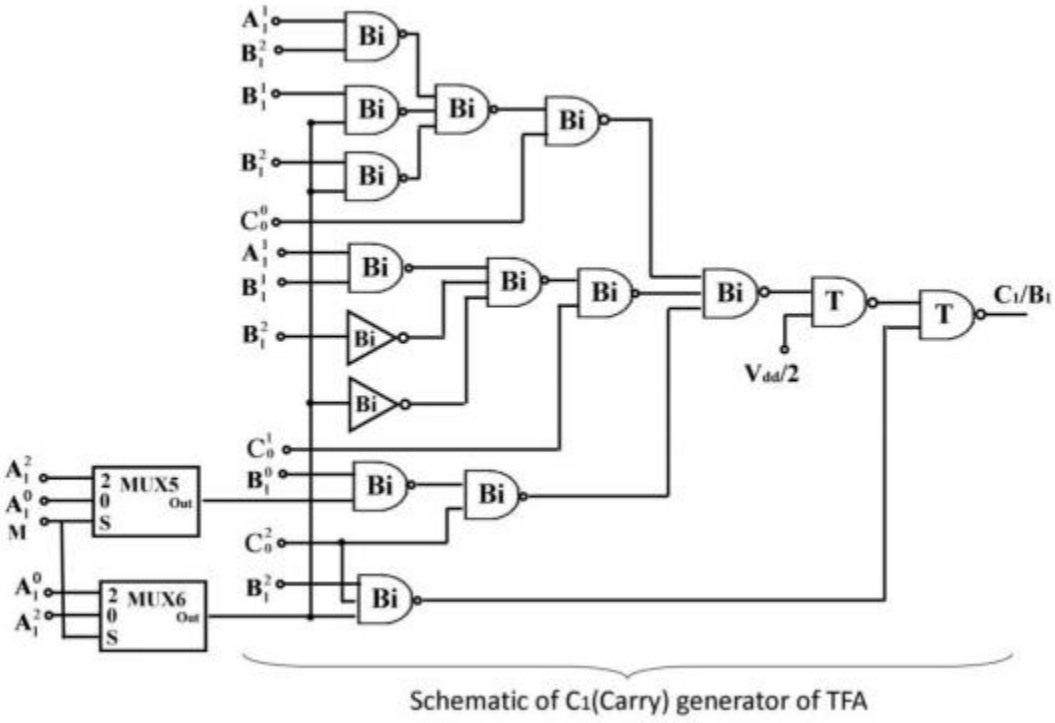


Figure 3.16 (b): Logic diagram of C1/B1 generator of ternary full adder-subtractor (FAS)

Table 3.7: Truth Table of ternary full adder (TFA) and full subtractor (TFS)

A_1	B_1	C_0	S_1(Sum)	C_1(Carry)	D_1(Difference)	B_1(Borrow)
0	0	0	0	0	0	0
0	0	1	1	0	2	1
0	0	2	2	0	1	1
0	1	0	1	0	2	1
0	1	1	2	0	1	1
0	1	2	0	1	0	1
0	2	0	2	0	1	1
0	2	1	0	1	0	1
0	2	2	1	1	2	2
1	0	0	1	0	1	0
1	0	1	2	0	0	0
1	0	2	0	1	2	1
1	1	0	2	0	0	0
1	1	1	0	1	2	1
1	1	2	1	1	1	1
1	2	0	0	1	2	1
1	2	1	1	1	1	1
1	2	2	2	1	0	1
2	0	0	2	0	2	0
2	0	1	0	1	1	0
2	0	2	1	1	0	0
2	1	0	0	1	1	0
2	1	1	1	1	0	0
2	1	2	2	1	2	1
2	2	0	1	1	0	0
2	2	1	2	1	2	1
2	2	2	0	2	1	1

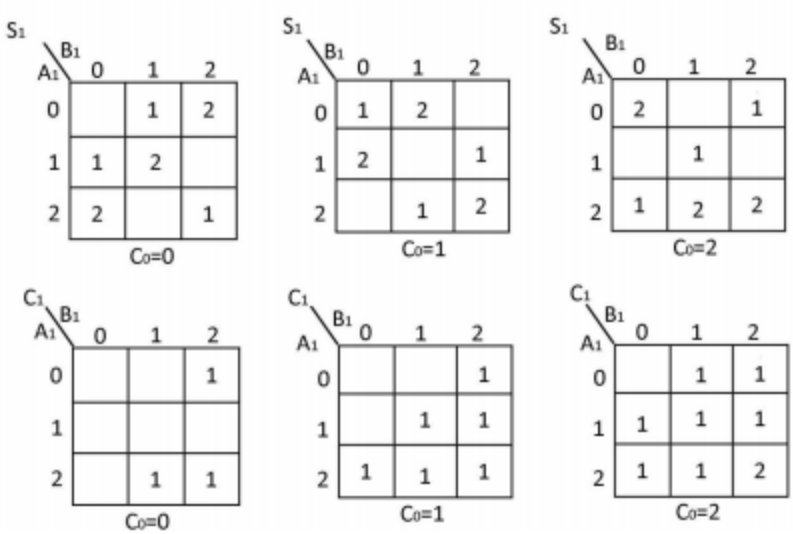


Figure 3.17: K-map for ternary full adder (TFA)

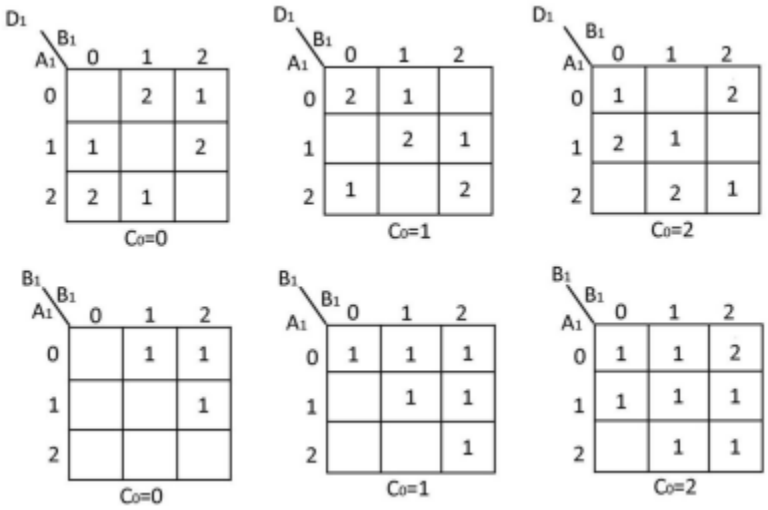


Figure 3.18: K-map for ternary full subtractor (TFS)

In light of the eq. (3.12) and (3.14), work for D_1 will be same as that of S_1 If B^1_1 is supplanted by B^2_1 , B^2_1 is supplanted by B^1_1 , C^1_0 is supplanted by C^2_0 , and C^2_0 is supplanted by C^1_0 . Likewise, agreeing to eq. (3.12) and (3.14), work for B1 will be same as that of C_1 if variable 0 A1 is supplanted by A^2_1 , and $A^2_1$is supplanted by A^0_1 . Thus, a TFA can produce D_1 and B_1 additionally, alongside S_1 and C_1, having appropriate selection of info factors. For this, MUXs are utilized as a part of FAS piece. Whenever M = 0, MUX1, MUX2 MUX3, MUX4, MUX5

and MUX6 select B^1_1, B^2_1, C^1_0, C^2_0, A^0_1 also, A^2_1 individually, and TFA processes the capacities given by eq. (3.12) and (3.13) for expansion operation. So also, when M = 2, MUX1, MUX2 MUX3, MUX4, MUX5 and MUX6 select 2 B1 , 1 B1 , 2 C0 , 1 C0 , A^2_1 what's more, A^0_1 separately, and TFA processes the capacities given by eq. (3.14) and (3.15) for subtraction operation.

It merits saying that by performing expansion and subtraction operations utilizing AS module, HO-TALU architecture accomplishes productive hardware execution of these two operations in examination with the current TALU architecture which contains isolate snake and subtractor modules.

3.5.2 Comparator Module

A comparator module performs correlation of An (A1A0) and B (B1B0), and decides their relative sizes. The reaction of examination is indicated by three output factors GR, EQ what's more, LE that indicate whether A is more prominent than B (A>B), An is not as much as B (A<B), or An is equivalent to B (A=B). Reality table of comparator is given in Table 3.8. As indicated by Table 3.8, after rationale is fulfilled:

1. One of output factors GR, EQ and LE is 2 then the staying two factors are dependably 0.

2. Two of GR, EQ and LE are 0 then the staying third one is dependably 2.

3. Two of GR, EQ and LE are never equivalent to 2 in the meantime.

4. GR, EQ and LE have just two rationale esteems 2 and 0, and they never can be 1.

Table 3.8: Truth Table of 2-bit ternary comparator

A_1	A_0	B_1	B_0	EQ	LE	GR
0	0	0	0	2	0	0
0	0	0	1	0	2	0
0	0	1	2	0	2	0
0	1	1	0	0	2	0

A_1	A_0	B_1	B_0	EQ	LE	GR
0	1	2	1	0	2	0
0	1	2	2	0	2	0
0	2	0	0	0	0	2
0	2	1	1	0	2	0
0	2	2	2	0	2	0
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	0	0	0	0	0	2
1	0	0	1	0	0	2
1	0	1	2	0	2	0
1	1	1	0	0	0	2
1	1	2	1	0	2	0
1	1	2	2	1	2	0
1	2	0	0	0	0	2
1	2	1	1	0	0	2
1	2	2	2	0	2	0
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
2	0	0	0	0	0	2
2	0	0	1	0	0	2
2	0	1	2	0	0	2
2	1	1	0	0	0	2
2	1	2	1	2	0	0
2	1	2	2	0	2	0
2	2	0	0	0	0	2
2	2	1	1	0	0	2
2	2	2	2	2	0	0

Based on first three observations, GR is expressed in terms of EQ and LE as follows.

$$GR = \overline{EQ + LE} \quad \textbf{(3.16)}$$

To derive EQ and LE, K-map is drawn as shown in Figure 3.19. From this K-map, simplified expressions for EQ and LE are derived and expressed as:

$$EQ = (A_1^0 B_1^0 + A_1^1 B_1^1 + A_1^2 B_1^2)\,(A_0^0 B_0^0 + A_0^1 B_0^1 + A_0^2 B_0^0) \quad \textbf{(3.17)}$$

$$LE = (A_1^0 B_1^0 + A_1^2 B_1^2 + \overline{A}_1^2 B_1^2) + (A_0^0 B_0^1 + \overline{A}_0^0 B_0^2 + A_0^2 B_0^0)(A_1^0 + B_1^0 + A_1^1 B_1^1) \quad \textbf{(3.18)}$$

In view of above forward perception, the comparator is actualized utilizing binary gate just in request to accomplish enhanced execution. The rationale graph of the comparator module is appeared in Figure 3.20. The circuits appeared in Figure 3.20 (an) and (b) process the capacities given by eq. (3.17) and (3.18) and as needs be, create EQ and LE, separately. At that point these output factors are gone through one NOR gate to produce GR in light of eq. (3.16) and appeared in Figure 3.20 (b).

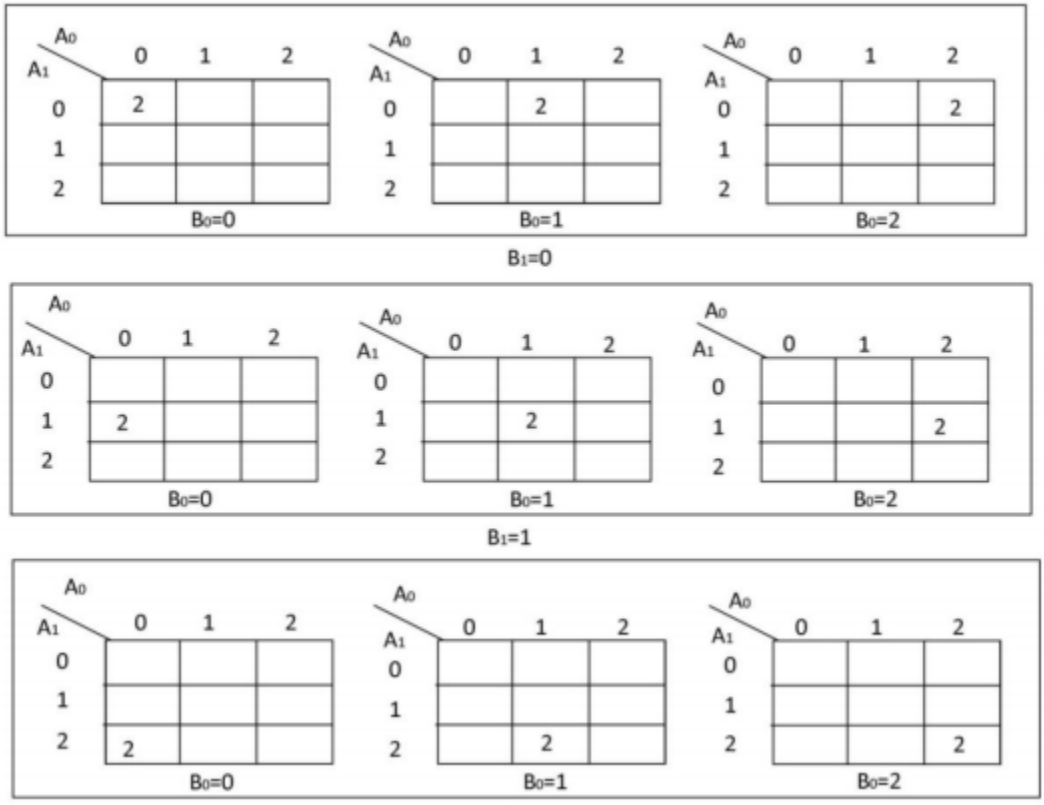


Figure 3.19(a): Ternary K-map for EQ of comparator module

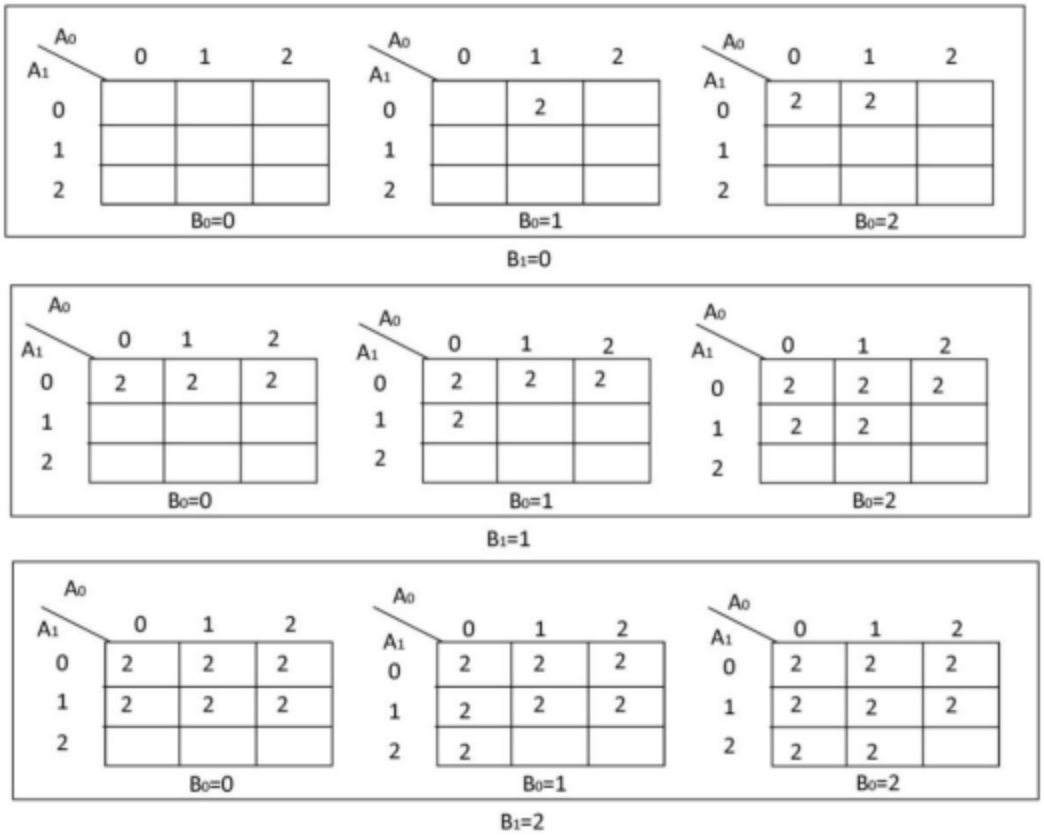


Figure 3.19(b): Ternary K-map for LE of comparator module

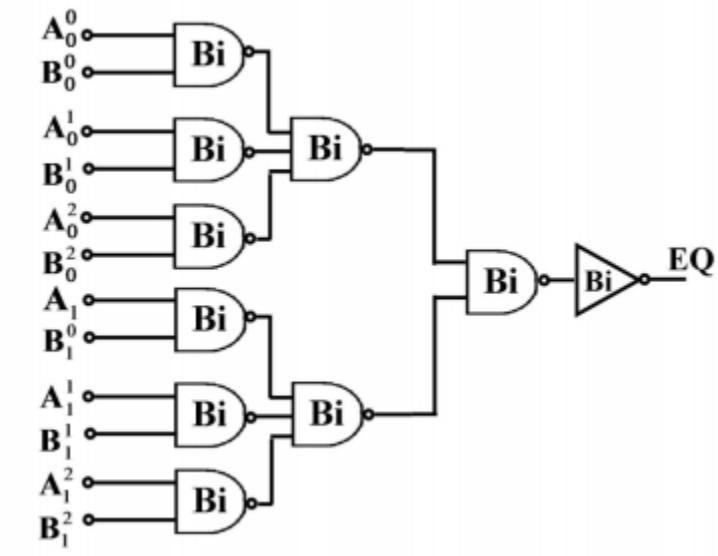


Figure 3.20 (a): Logic level diagram for EQ generator of comparator Module

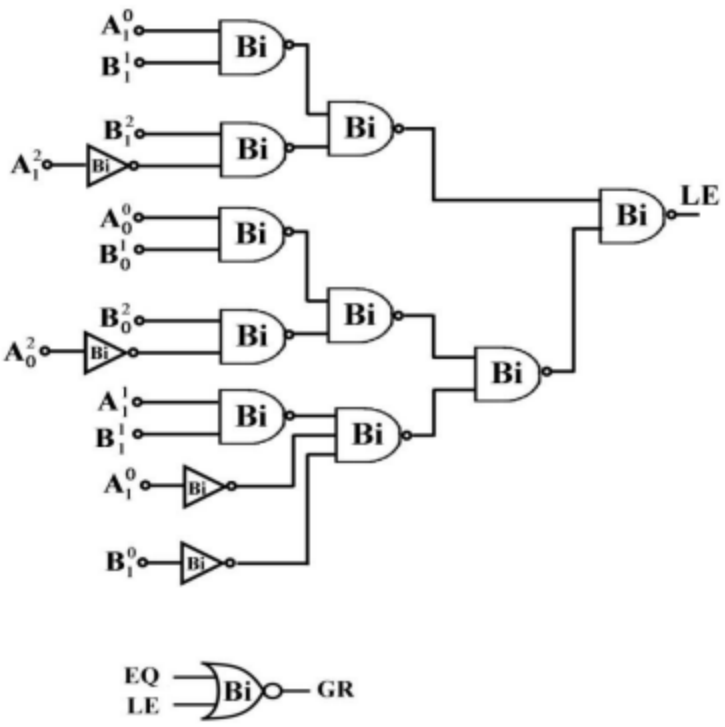


Figure 3.20(b): Logic level diagram for LE and GR generator of comparator module

The comparator design accomplishes hardware advancement at three levels. At first level, it actualizes GR utilizing just a single NOR gate. At second level, disentangled rationale articulations are utilized for EQ and LE. At third level, these capacities are executed utilizing binary gate just rather than ternary gate .Therefore, for examination operation, HO-TALU diminishes number of rationale entryways around to one fourth as for its partner.

3.5.3 Exclusive-OR Module

The square graph of restrictive OR module is appeared in Figure 3.21. It performs XOR operation on An (A_1A_0) and B (B_1B_0), and produces two outputs $A_0 \oplus B_0$ and $A_1 \oplus B_1$. The ternary XOR operation is done utilizing mod-3 expansion where convey bit produced from ternary expansion is overlooked. As an outcome, restrictive OR module is executed utilizing whole generation circuitry of THA, which is spoken to by THA_SUM square. This module comprises of two THA_SUM pieces where each square performs 1-bit XOR operation. Reality table of 1-bit XOR operation for A_0 and B_0 is given in Table 3.9. The schematic chart of

THA_SUM piece is appeared in Figure 3.22 where eight binary NAND gate, two ternary NAND entryways and an inverter deliver XOR work which is characterized as takes after.

$$A_0 \oplus B_0 = A_0^2 B_0^0 + A_0^1 B_0^1 + A_0^0 B_0^2 + 1.(A_0^1 B_0^0 + A_0^0 B_0^1 + A_0^2 B_0^2) \quad \textbf{(3.19)}$$

The proposed exclusive-OR module leads to compact structure with respect to its counterpart presented which utilizes both sum and carry generator of THA block.

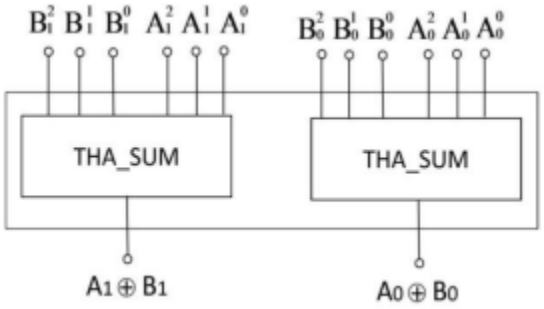


Figure 3.21: Block diagram of the exclusive-OR module

Table 3.9: Truth table of 1-bit ternary XOR

A_0	B_0	$A_0 \oplus B_0$
0	0	0
0	1	1
0	2	2
1	0	1
1	1	2
1	2	0
2	0	2
2	1	0
2	2	1

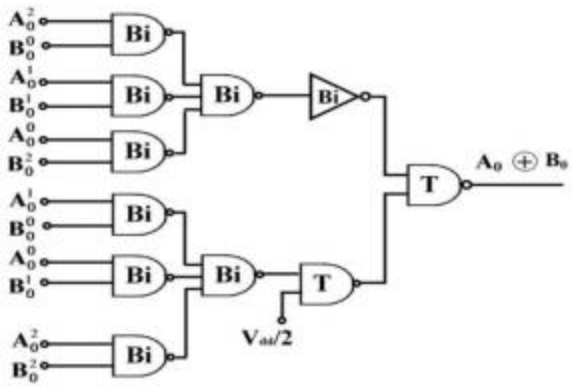


Figure 3.22: Logic level diagram of THA_SUM block of exclusive-OR module

3.5.4 Multiplier Module

Duplication of ternary numbers is performed similarly as increase of decimal or binary numbers. The multiplicand is duplicated by each piece of the multiplier, beginning from the minimum critical position and each such increase frames an incomplete product. Progressive fractional products are moved one position to one side and the last product is acquired from the entirety of the fractional products. Figure 3.23 demonstrates the square graph of the multiplier module (decoded unary capacities for input information are not appeared). The architecture of multiplier displayed is utilized,here. It performs duplication of A_1A_0 and B_1B_0, and produces product of four bits $M_3M_2M_1M_0$ with $C_{out.}$

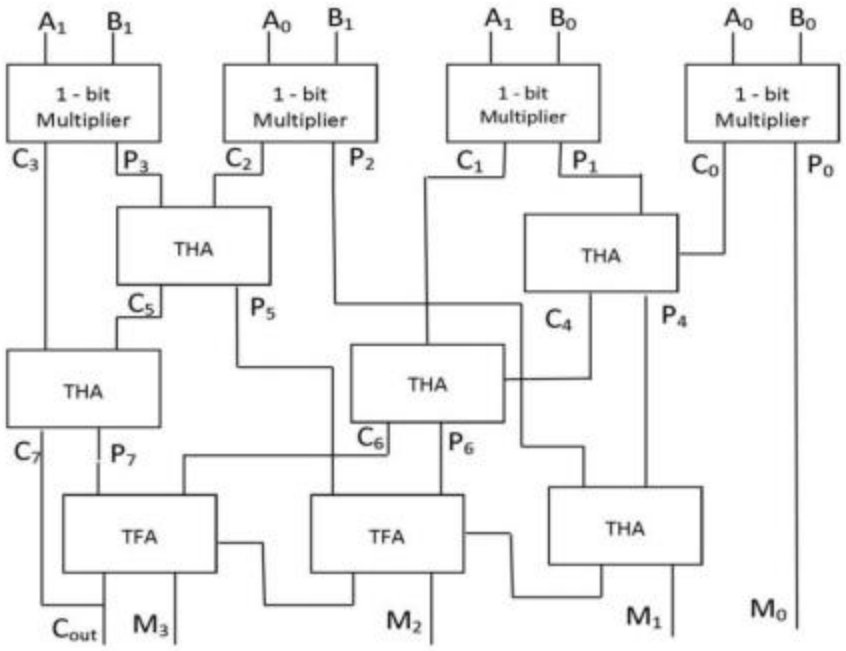


Figure 3.23: Block diagram of multiplier module

Multiplier module contains 1-bit multipliers, ternary half adders (THAs) and ternary full adders (TFAs) for the generation of incomplete products, moving and last expansion of halfway products. Table 3.10 gives reality table of 1-bit multiplier which performs duplication of A0 and B_0, furthermore, produces outputs P_0 and C_0. Figure 3.24 demonstrates the K-outline the same. From the K-delineate, disentangled articulations of P_0 and C_0 are determined and communicated as:

$$P_0 = (A_0^2 B_0^1 + A_0^1 B_0^2) + 1.(A_0^1 B_0^1 + A_0^2 B_0^2) \quad \textbf{(3.20)}$$

$$C_0 = 1.(A_0^2 + B_0^2) \quad \textbf{(3.21)}$$

Table 3.10: Truth table of 1-bit ternary multiplier

A_0	B_0	P_0 (Product)	C_0 (Carry)
0	0	0	0
0	1	0	0
0	2	0	0
1	1	1	0
1	2	2	0
2	2	1	1

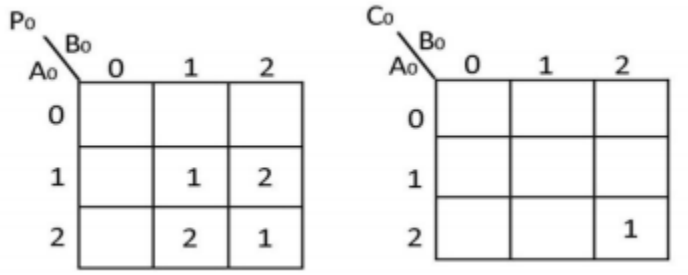


Figure 3.24: K-map of 1-bit ternary multiplier

Figure 3.25 gives the rationale outline of 1-bit ternary multiplier which processes the capacities given by eq. (3.20) and (3.21). A 1-bit multiplier is executed utilizing design approach exhibited. The usage of THA is as of now talked about in area 3.4 and appeared in Figure3.12. FAS Square examined in segment 3.5.1 and appeared in Figure 3.16, barring MUXs. The mix of binary and ternary rationale entryways utilized as a part of subblocks of multiplier prompts a hardware productive design as for the multiplier design introduced.

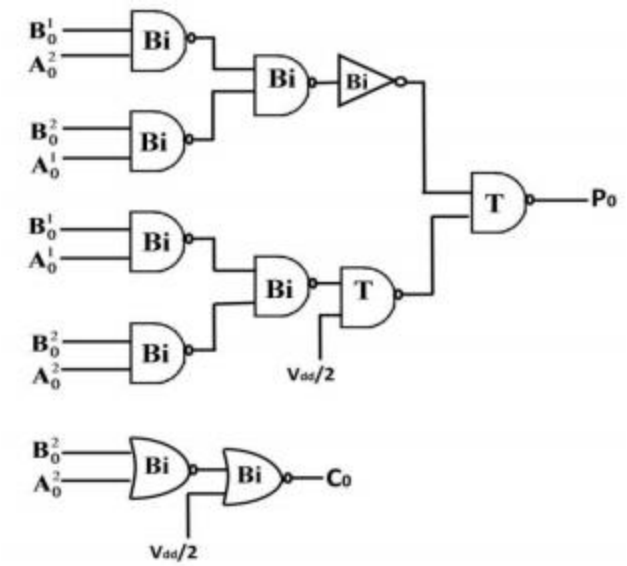


Figure 3.25: Logic level diagram of 1-bit ternary multiplier

3.5.5 T-OR/T-NOR/T-AND/T-NAND Module

Figure 3.26 shows the logic diagram of T-OR/T-NOR/T-AND/T-NAND modules. They perform logic operations on A (A_1A_0) and B (B_1B_0) using ternary gates which are discussed in section 3.2. Since logic operations manipulate the bits of the operands separately and treat each bit as a ternary variable, each type of ternary gate is repeated two times to get 2-bit logic outputs.

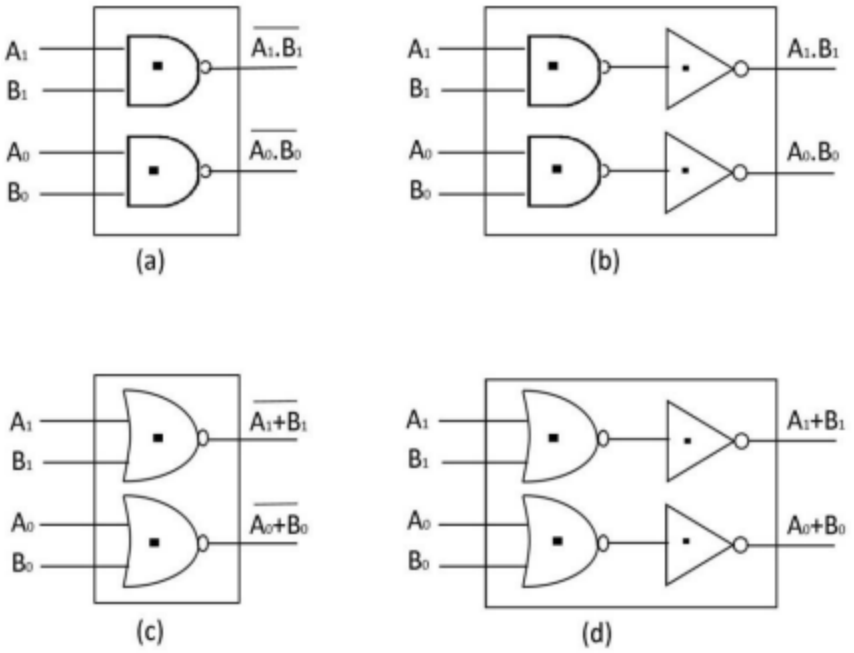


Figure 3.26: Logic level diagram of (a) T-NAND (b) T-AND (c) T-NOR (d) T-OR modules

3.6 2-bit HO-TALU Slice for N-bit HO-TALU

Design of 2-bit HO-TALU is extended to implement a 2-bit HO-TALU slice which can be duplicated for n/2 times to build an N-bit TALU. The pin diagram of the 2-bit HO-TALU slice is shown in Figure 3.27. Compared to design of 2-bit HO-TALU, this slice has new input signals which are named as cascaded signals: $Carry_c$/$Borrow_c$, GR_c, EQ_c and LE_c

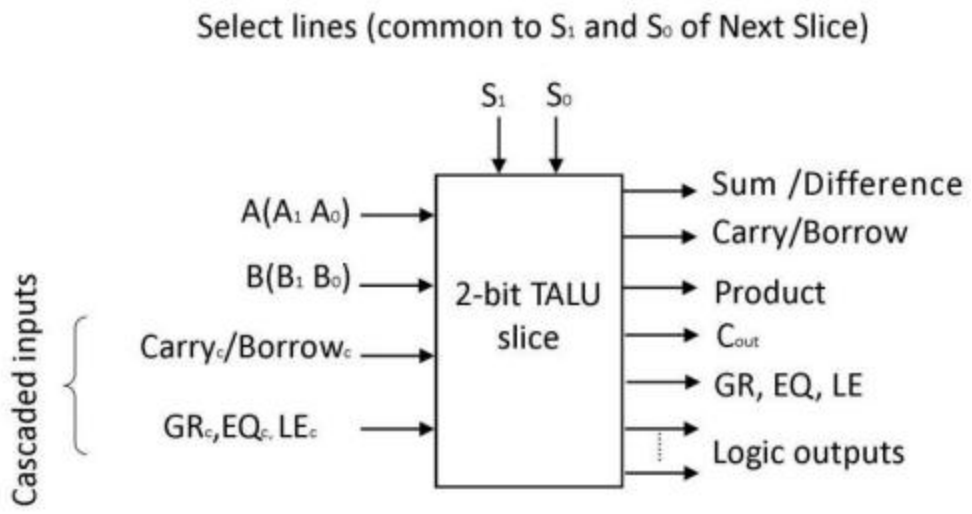


Figure 3.27: Block diagram of 2-bit HO-TALU slice

To join these signs for execution of 2-bit TALU cut, a few alterations are required in 2-bit HO-TALU design. Adjustment in the AS module is appeared in Figure 3.28 (decoded unary capacities for input information are not appeared). The adjusted AS (MAS) module employments FAS hinder set up of HAS to manage fell contribution of convey/borrow flag i.e. Carryc/Borrowc (C_c/B_c). For N-bit HO-TALU, the fell arrangement of this module is appeared in Figure 3.29 where input Cc_0/B_{c0} of MAS1 is associated with ground (rationale 0). Info C_{c1}/B_{c1} of MAS2 is associated with output C1/B1 of MAS1. Correspondingly, for different MAS module, input C_c/B_c originates from output C/B of their individual past square, accordingly the created conveys or, on the other hand borrows propagates in a chain through the MAS modules. When the past carrier or borrow are accessible, the right Sum/Difference and Carry/Borrow rise up out of the output S/D what's more, C/B of MAS modules.

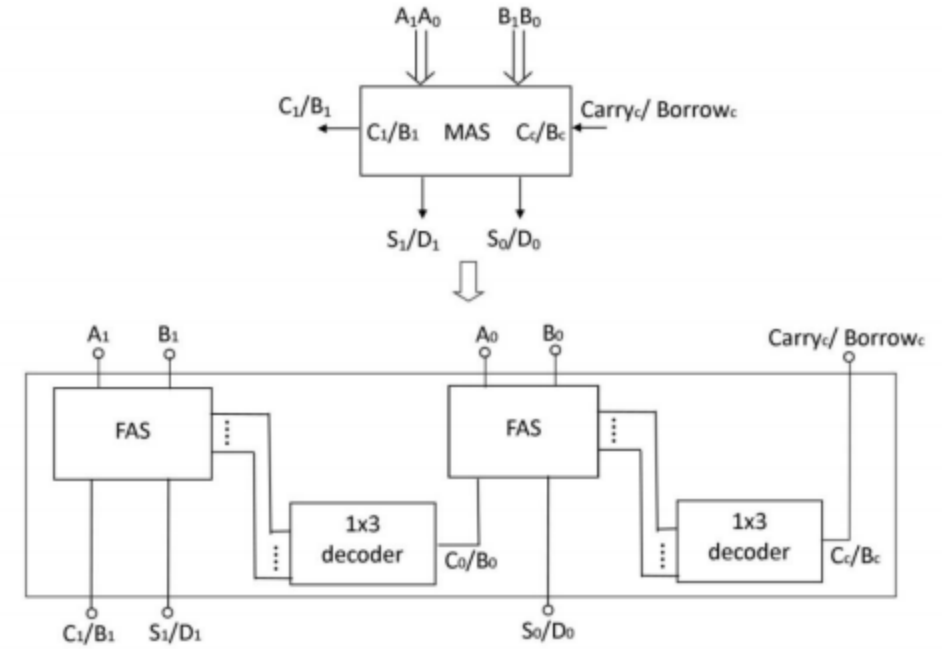


Figure 3.28: Block Diagram for modified adder-subtractor (MAS)

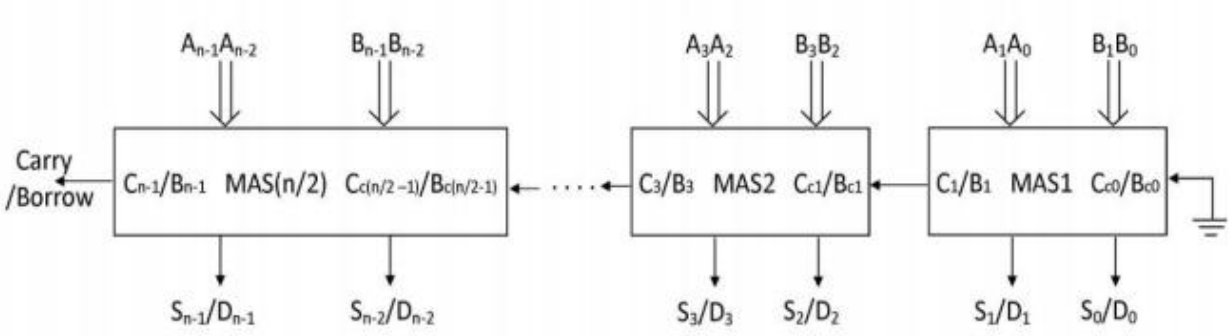


Figure 3.29: Cascaded configuration of modified adder-subtractor (MAS) for N-bit HOTALU

The modified comparator (MCOMP) module of 2-bit cut is appeared in Figure 3.30. MCOMP contains 2-bit HO-TALU comparator module which is named as COMP_Pre obstruct, here and one little included circuitry. In this module, falling comparator inputs GR_c, EQ_c and LE_c, and signals GR_i , EQ_i and LE_i produced by COMP_Pre square, are connected to included circuit which produces three outputs EQ, LE and GR. This additional circuit is executed in view of the following perceptions:

1. For EQ to be 2, both EQ_c and EQ_i ought to be 2.

2. For LE to be 2, either LE_i ought to be 2 or both EQ_i and LE_c ought to be 2.

3. For GR to be 2, either GR_i ought to be 2 or both EQ_i and GR_c ought to be 2.

Likewise, EQ, LE and GR are acquired and communicated as takes after.

$$EQ = \overline{EQ_c \cdot EQ_i} \quad \textbf{(3.22)}$$

$$LE = LE_i + LE_c \cdot EQ_i \quad \textbf{(3.23)}$$

$$GR = GR_i + GR_c \cdot EQ_i \quad \textbf{(3.24)}$$

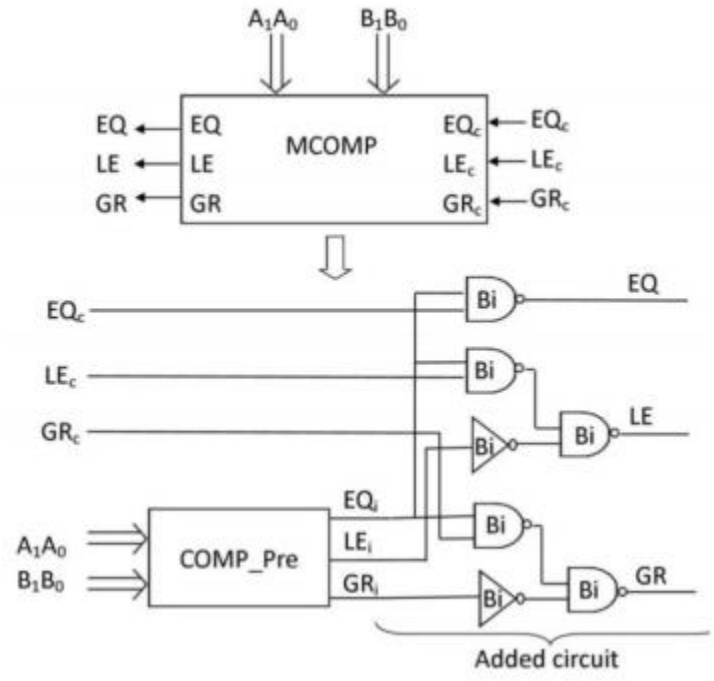


Figure 3.30: Logic diagram for modified comparator (MCOMP)

For N-bit TALU, the cascaded configuration of MCOMP module is shown in Figure 3.31, where cascading comparator inputs EQc0, GRc0 and LEc0 of MCOMP1 is connected to Vdd, 0, and 0 respectively. Inputs EQc1, GRc1 and LEc1 of MCOMP2 are connected to outputs EQ1, GR1 and LE1 of MCOMP1. Similarly, for other MCOMP block, inputs EQc, GRc and LEc come from outputs EQ, GR and LE of their respective previous block, thus the comparator outputs are connected in a chain through the MCOMP blocks. The final N-bit comparison result emerges from MCOMPN/2 block where $A_{N-1}A_{N-2}$ and B_{N-1} B_{N-2} of N-bit ternary numbers (A and B) are applied. For 2-bit HO-TALU slice, logic operation modules of HO-TALU are used without any modification. Further, as the number of bits increases, multiplication becomes more complex. For N-bit multiplication, the multiplier block presented in [62] is used where parallel N-bit design requires N2 one-bit ternary multipliers, (N - 1) THAs, and N (N - 1) TFAs.

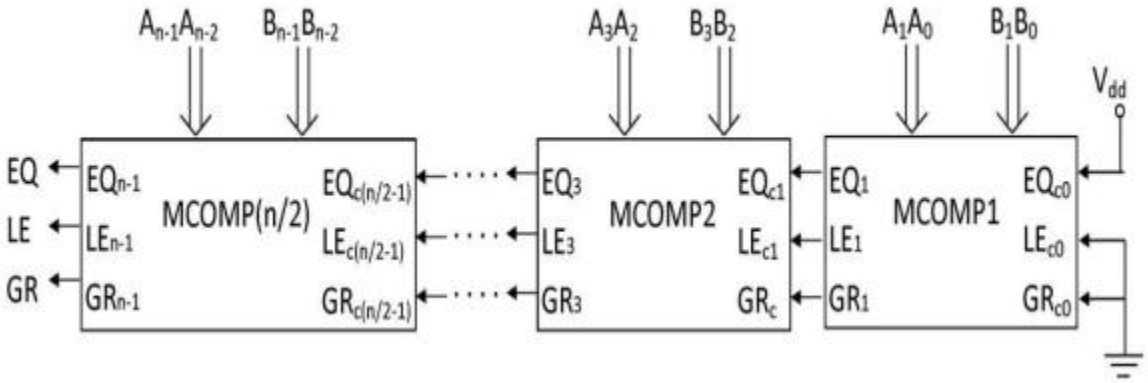


Figure 3.31: Cascaded configuration of modified comparator (MCOMP) for N-bit HO-TALU

3.7 Results and Discussion

Design of proposed 2-bit HO-TALU is broke down and assessed utilizing Synopsys HSPICE test system with the Stanford model of 32 nm CNTFET which incorporates non-idealities of CNTFET. Points of interest of the Stanford display have been shown in area 2.2 of section 2. The chirality vector of CNTFETs utilized as a part of binary gate and TG square is (19, 0). The edge voltage of these transistors is 0.289V with the diameter of 1.487 nm. The diameter of CNTFETs used in ternary gate is given in area 3.2 of this part. Other innovation parameters of CNTFET have same esteems as said in segment 2.2 of section 2.

To perform correlation of proposed ternary designs in CNTFET innovation, TALU design introduced in [73] is recreated. For this, circuits of TALU modules displayed are taken also, executed utilizing CNTFET-based ternary gate as these rationale entryways beat other existing CNTFET-based entryways. Design of THA exhibited prompts vitality productive also, smaller design as for other CNTFET-based THA circuits. As a result, THS, TFA and TFS are likewise actualized utilizing the design approach of and alluded as CNTFET-based circuits of [199], for examination of HAS and FAS. Further, keeping in mind the end goal to perform examination with 32 nm CMOS innovation, proposed circuits are executed utilizing CMOSbased binary and ternary rationale gate introduced. The CMOS-based ternary gate utilizes numerous voltages for limit voltage change and depends on multi-edge strategy for ternary operation. Berkeley Predictive 32nm CMOS demonstrate is utilized to reenact CMOSbased designs. For duplicated designs, viewpoint proportions of MOSFETs, diameter of CNTFETs and estimation of different parameters, are picked by the data given in the particular papers from the literature.

3.7.1 Functional Verification of 2-bit HO-TALU

To check the functionality of 2-bit HO-TALU, its sub-circuits and also whole design are tried through transient reproductions. For moment, the transient waveform of FAS cell is appeared in Figure 3.32. The initial three waveforms speak to inputs A_1, B_1 and C_0 (input Carry/Borrow). At the point when mode input M = 0, FAS performs expansion (A_1+B_1+C_0) and creates outputs S1 (Sum) and C_1 (Convey). These signs are appeared in the fourth and fifth waveforms individually. Likewise, when M = 2, FAS performs subtraction (A_1-B_1-C_0) and produces two outputs D_1 (Difference) and B_1 (Borrow). These signs are appeared in the 6th and seventh waveforms, separately. Depending upon the estimation of mode input M, FAS performs adjust ternary expansion and subtraction operation and in this way, the functionality of FAS is checked. Thus, transient waveforms of proposed HAS, multiplier, comparator, exclusive-OR and rationale operation modules (just T-AND is incorporated) are appeared in Appendix which affirm their right operations.

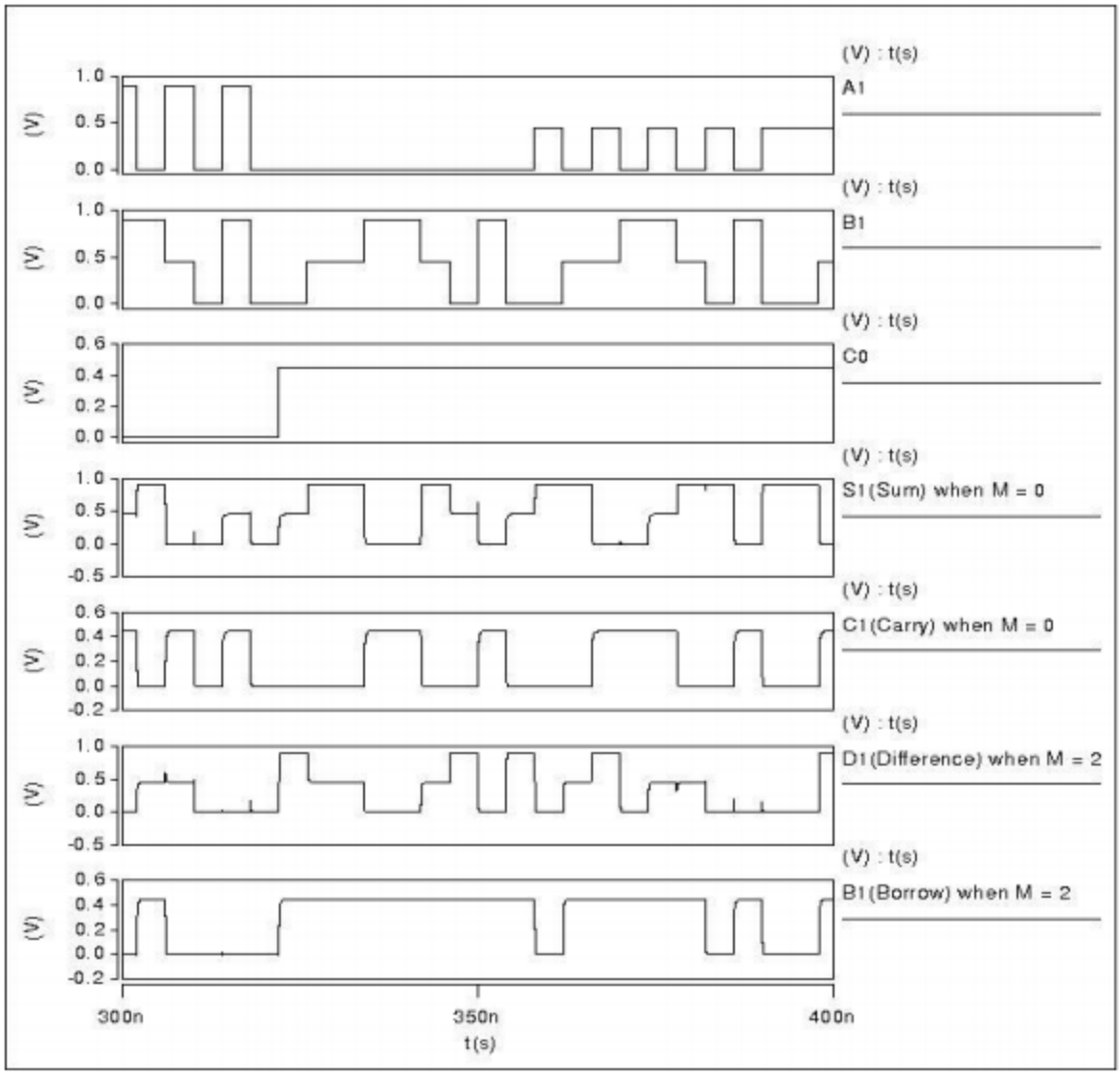


Figure 3.32: Transient waveform of full adder-subtractor (FAS)

3.7.2. Hardware Efficiency Evaluation of 2-bit HO-TALU

Design of 2-bit HO-TALU is assessed on the premise of hardware effectiveness. For expansion and subtraction operations, HO-TALU design presents an AS module while the current TALU designs contain isolate snake and subtractor module. The sub-squares of AS are HAS and FAS. HAS is contrasted and its partner which are considered as a blend of THA and THS. Essentially, FAS is contrasted and its partner which are considered as a mix of TFA and TFS. Designs of 2-bit multiplier, 2-bit comparator and 2-bit exclusive-OR are contrasted and their counterparts introduced. Examination of proposed ternary circuits in light of gadget include is given Table

3.11 and appeared in Figure 3.33. HAS square reduces number of transistors by 34% and 76% contrasted with the designs introduced individually. Likewise, FAS square reduces number of transistors by 41% and 82% contrasted with the designs introduced individually. Designs of 2-bit multiplier, 2-bit comparator and 2-bit exclusive-OR accomplish lessening in gadget tally by 64%, 82% and 76% separately, in examination with their counterparts.

Table 3.11: Comparison of ternary circuits based on device count

S. No.	Circuits	Device Count	% improvement in Device count
i	Combination of HA and HS designs of [199]	184	
ii	Combination of HA and HS circuits of [73] using CNTFETs	504	
iii	**Proposed** HAS	122	34 wrt (i), 76 wrt (ii)
iv	Combination of FA and FS designs of [199]	428	
v	Combination of FA and FS circuits of [73] using CNTFETs	1448	
vi	**Proposed** FAS	250	41 wrt (iv), 82 wrt (v)
vii	2-bit multiplier circuit of [73] using CNTFETs	3532	
viii	**Proposed** 2 bit multiplier	1256	64 wrt (vii)
ix	2-bit comparator circuit of [73] using CNTFETs	600	
x	**Proposed** 2-bit comparator	104	82 wrt (ix)
xi	2-bit exclusive-OR circuit of [73] using CNTFETs	504	
xii	**Proposed** 2-bit exclusive-OR	116	76 wrt (xi)

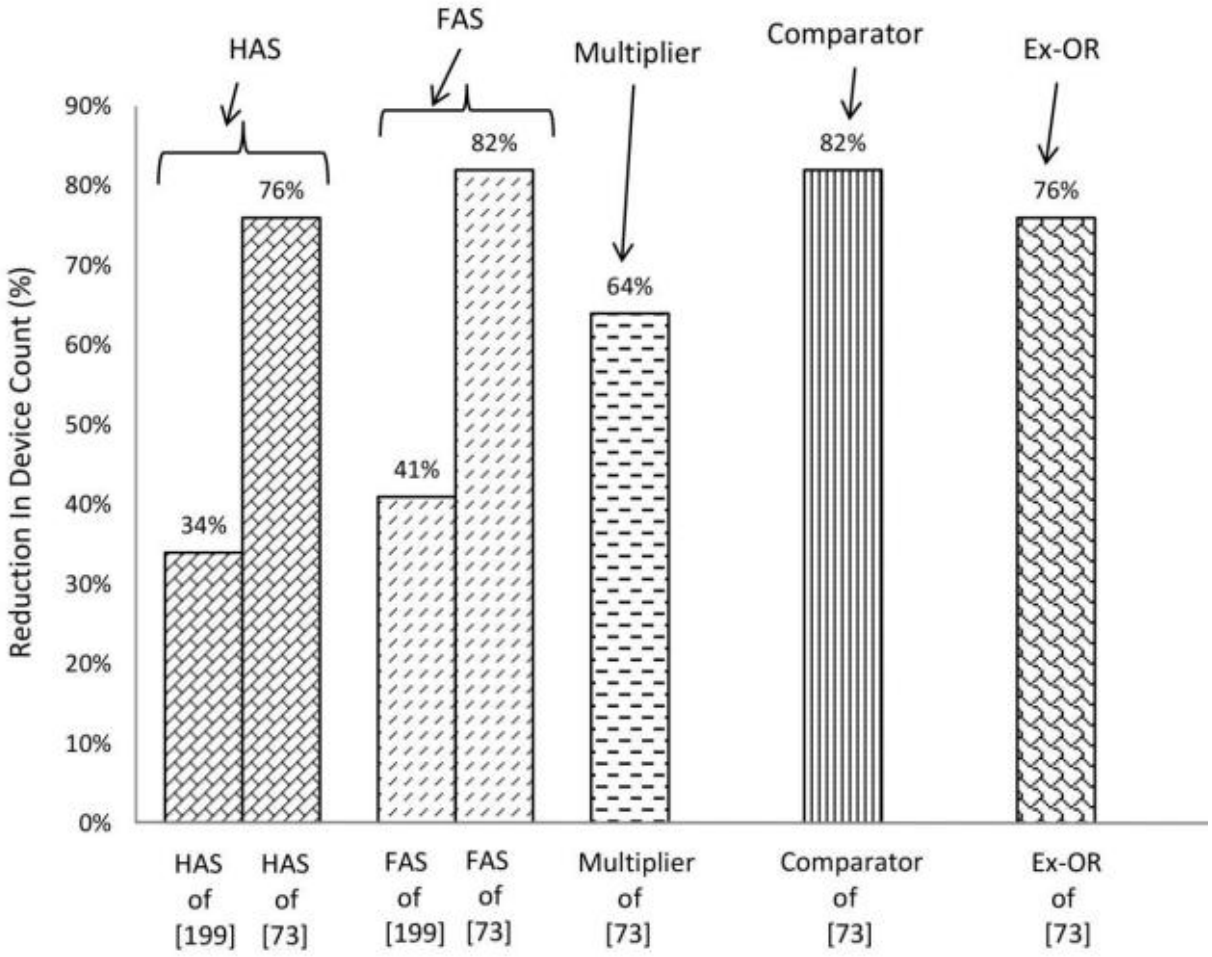


Figure 3.33: Comparison of ternary circuits based on device count

3.7.3 Performance Evaluation of 2-bit HO-TALU

To assess performance of proposed ternary circuits, speed and power are separated from transient simulations. The normal power consumption is measured over a drawn out stretch of time. For most pessimistic scenario delay determination, all conceivable output transition delays are measured. Further, because of the expanded interest for fast, high-throughput calculation and complex functionality in versatile situations, diminishment of delay and power consumption is exceptionally testing. By virtue of the exchange off between power consumption and delay, the productivity of the circuits is assessed by figuring PDP, which is the increase of the normal power consumption and the greatest delay. Delay, power and PDP of ternary circuits in both 32 nm CNTFET and 32 nm MOSFET advancements, at 0.9 V supply voltage with room

temperature, 2.1 fF output stack and 250 MHz working frequency, are recorded in Table 3.12. Ternary circuits are additionally mimicked at 1 GHz working frequency with 3 fF output stacks and at three distinctive supply voltages. Results acquired from these simulations are recorded in. To assess performance at architecture level, diverse HO-TALU information ways containing decoder, FSB-AHO, TGB-AHEfurthermore, isolate sub piece, have been reproduced. Delay, power and PDP comes about are separated and appeared in Table 1 of Appendix II. Correlation of CNTFET-construct ternary designs based with respect to PDP is appeared in Figure 3.34. Table 3.12 demonstrate that the proposed CNTFET-based circuits accomplish around two hundred times lower PDP in examination with that of their CMOS counterparts, which checks the potential advantage of CNTFET circuits. In examination with circuits of executed utilizing CNTFET-based doors, proposed multiplier, comparator and exclusive-OR get diminishment in PDP by 75%, 65% what's more, 28%, separately. In any case, PDP of sub-modules HAS and FAS has marginally expanded by 2% what's more, 5%, separately, in examination with their CNTFET-based counterparts. Hence, every one of the 2-bit HO-TALU modules accomplish great hardware proficiency with a minor loss of PDP for expansion and subtraction operations just, as for CNTFET circuits accessible in the literature.

Table 3.12: Simulation results of ternary circuits

Circuits	Delay ($\times 10^{-10}$ S)	Power ($\times 10^{-6}$ W)	PDP ($\times 10^{-16}$ J)
CNTFET-based THA of [199]	0.69	1.01	0.69
CNTFET-based HAS for addition operation **(proposed)**	0.71	1.02	0.72
HAS based on CMOS logic gates of [141] for addition operation	1.77	81.35	144
CNTFET-based TFA of [199]	0.80	1.45	1.16
CNTFET-based FAS for addition operation **(proposed)**	0.82	1.49	1.22
FAS based on CMOS logic gates of [141] for addition operation	2.45	145	355
2-bit multiplier of [73] using CNTFETs	1.96	23.3	45.67
CNTFET-based 2-bit multiplier **(proposed)**	1.45	7.82	11.34
2-bit comparator of [73] using CNTFETs	0.81	0.99	0.80
CNTFET-based 2-bit comparator **(proposed)**	0.48	0.63	0.30
1-bit exclusive-OR of [73] using CNTFETs	0.69	1.01	0.69
CNTFET-based 1-bit exclusive-OR **(proposed)**	0.69	0.60	0.41

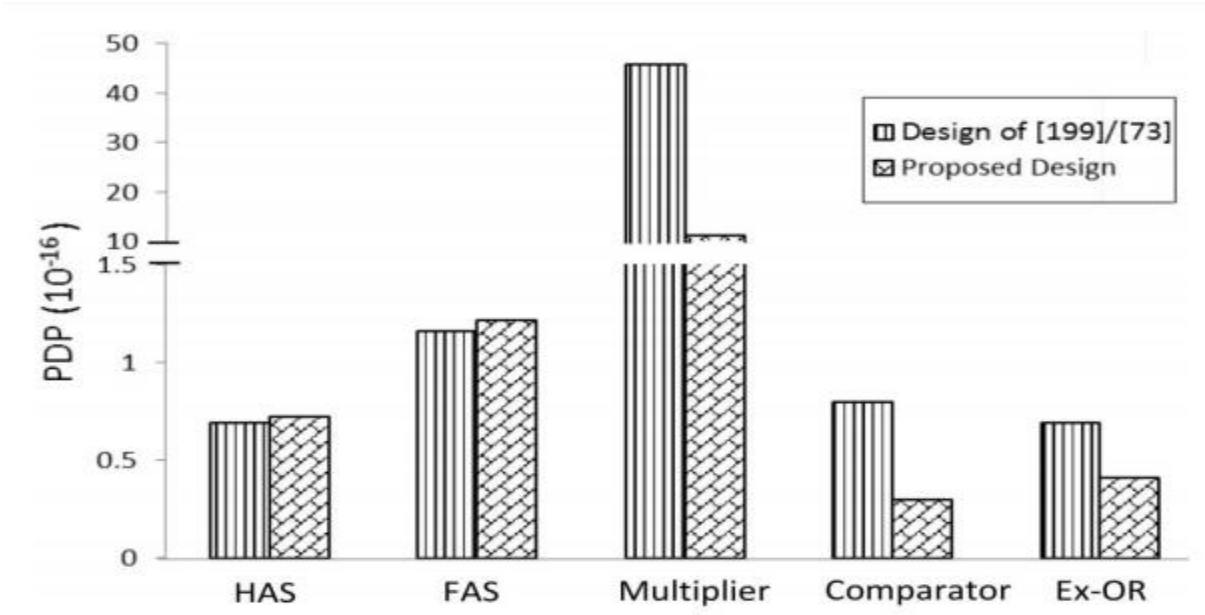


Figure 3.34: Comparison of ternary circuits based on PDP

3.8 Conclusion

In this part, design of 2-bit HO-TALU utilizing CNTFETs has been exhibited. 2-bit HOTALU has another AS module which performs both expansion and subtraction operations utilizing a viper module just with the assistance of MUXs. In this manner, it dispenses with a subtractor module from the customary architecture. HO-TALU limits ternary capacity articulations and uses binary entryways alongside ternary doors in realization of practical modules: AS, multiplier, comparator and exclusive-OR. As a result, the sub-pieces of AS: HAS and FAS utilize about 76% and 82% less transistors, separately, than regular designs which contain isolate viper and subtractor squares. Multiplier, comparator and exclusive-OR show lessening in gadget number by 64%, 82% and 76%, individually, regarding their current counterparts. Results got from HSPICE test system with Stanford model of 32nm CNTFET have appeared that all HO-TALU modules accomplish extraordinary improvement (about two hundred times) in PDP with regard to their CMOS-based partner, which checks the potential advantage of CNTFET circuits. In examination with existing CNTFET-based designs, proposed multiplier, comparator what's more, exclusive-OR get decrease in PDP by 75%, 65% and 28%, separately. Be that as it may, PDP of sub modules HAS and FAS has marginally expanded by 2% and 5%, individually. Accordingly, all HOTALU modules accomplish great hardware productivity with a minor loss of PDP for expansion and subtraction operations just, regarding CNTFET circuits accessible in the literature. Additionally, design of 2-bit HO-TALU is stretched out to build up a 2-bit HO-TALU cut which could be effortlessly fell to build a N-bit HO-TALU.

In the following part, TFA which is an essential sub-piece of AS, is modified utilizing diverse circuit methods to enhance its effectiveness as far as PDP. Three TFA designs named as high speed ternary full viper (HS-TFA), low power ternary full snake (LP-TFA), dynamic ternary full viper (DTFA) are displayed. What's more, a modified comparator with enhanced PDP is moreover displayed for present day hardware with CNTFETs.

Chapter 4

Performance Boosted Designs of Sub-Blocks of 2-bit Hardware Optimized Ternary ALU (HO-TALU) using CNTFETs

4.1 Introduction

In part 3, design of a 2-bit hardware optimized ternary ALU (HO-TALU) has been displayed utilizing CNTFETs. This part introduces performance helped designs of sub-squares of CNTFET-based 2-bit HO-TALU utilizing diverse circuit systems. Three new designs of ternary full viper (TFA) which is an essential sub-square of snake subtractor (AS) are proposed. These designs are optimized as far as speed, power lastly power-delay product (PDP). The main TFA design named as rapid TFA (HS-TFA) utilizes a symmetric pull-up and pull-down networks alongside a resistive voltage divider as its fundamental part,which is configured utilizing transistors. Contrasted with as of late created TFA accessible in literature, HS-TFA gets enhanced speed yet high power dissipation. Keeping in mind the end goal to lessen power consumption, a moment TFA named as low power TFA (LP-TFA) is proposed. LPTFA makes utilization of complimentary pass transistor rationale style and accomplishes low power consumption with marginal lessening in PDP. To get enhanced PDP further, a third TFA is actualized in unique rationale. This TFA is named as unique TFA (DTFA) which utilizes a manager designed for ternary esteems to reduce charge sharing issue. The realization of each of the three TFA takes the benefits of innate binary nature (0 and 1) of information convey prompting straightforwardness in designs.

Next, another design of comparator module of 2-bit HO-TALU is exhibited. Initial, 1-bit comparator is created utilizing pass transistor rationale with diminished number of stages in basic delay way. At that point, 1-bit design is used to make 2-bit and N-bit comparator where a static binary tree arrangement is utilized to redress the voltage levels. The proposed 2-bit comparator accomplishes better PDP in correlation with that of accessible counterparts. This comparator, HSTFA also, DTFA have high driving capacity. In addition, all new TFAs and 2-bit comparator are less touchy to voltage and temperature varieties as for existing designs.

In area 4.2, designs of TFA which incorporate HS-TFA, LP-TFA and DTFA, alongside their reenactment results and examination, are exhibited. Area 4.3 depicts design of ternary comparator with its evaluation, trailed by conclusion in segment 4.4.

4.2 Designs of Ternary Full Adder (TFA)

A TFA includes three bits (A, B and C_{in}) in which A and B are critical bits (1-bit ternary numbers) and C_{in} is convey bit produced by the past piece expansion amid N-bit operation. In this, the greatest aggregate of A and B is 4 in any event noteworthy position and 5 at other positions, which gives most extreme estimation of C_{in} i.e. rationale 1. In this manner, C_{in} never gets rationale 2 in N-bit ternary expansion. By utilizing this idea, TFA is designed in light of the binary nature (0 also, 1) of Cin with ternary nature of A and B.

4.2.1 High Speed TFA (HS-TFA)

The stick chart and piece outline of the primary proposed TFA named as HS-TFA are appeared in Figure 4.1. Reality table of TFA is given in Table 4.1, where Aand B are ternary in nature, and C_{in} is binary in nature (0 and 1). HS-TFA has three information sources A, B and C_{in}, and two outputs Sum and Carry. Sources of info A, B and C_{in} are gone through 1-to-6-line ternary decoders DEC1, DEC2 and DEC3, separately, to create their unary capacities. HS-TFA comprises of a Sum generator and a Carry generator to deliver Sum and Carry signals. Entirety generator contains symmetrical pull-up organize (PUN) and pull-down system (PDN) alongside resistive voltage divider which is actualized utilizing two always exchanged ON transistors T1 and T2. A square set apart as 'Joke for Σin =1, 2, 4 and 5' speaks to a system that will exchanged ON when $\sum (A+B+C_{in}) = 1, 2, 4$ and 5. Thus, a square set apart as 'PDN for Σin =0, 1, 3 and 4' speaks to a system that will exchanged ON when $\sum (A+B+C_{in}) = 0, 1, 3$ and 4. These squares are designed in light of their changing exercises required to create Aggregate. The nitty gritty schematic of Sum generator is appeared in Figure 4.3 (a). Further, T1 (PCNTFET) furthermore, T2 (N-CNTFET) having same geometry achieve a similar resistance and perform voltage division to get rationale 1 for Sum. Table 4.2 abridges how the ON condition of relating PUN and PDN associate Sum to suitable voltage source (Vdd or ground) for every conceivable blend of A, B and C_{in}. Whenever $\sum (A+B+C_{in}) = 0$, PDN is turned ON which interfaces Sum to ground through T2. In spite of the fact that T1 is additionally ON, the PUN is OFF. At the point when

$\sum(A+B+C_{in}) = 1$, both PUN and PDN are accordingly ON, nodes X2 and X1 are charged to Vdd and 0, individually, and T1 and T2 perform voltage division between node voltages of X1 and X2, and create Sum as (X1+X2)/2 = Vdd/2 (i.e. voltage level of rationale 1). Whenever $\sum (A+B+C_{in}) = 2$, PUN is exchanged ON and associates Sum to Vdd through T1. Also, for different estimations of $\sum (A+B+C_{in})$, Sum gets the best possible incentive through PUN, PDN or both, as appeared in Table 4.2

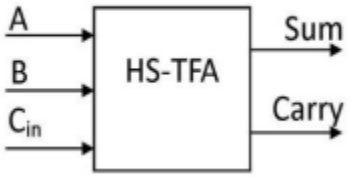


Figure 4.1 (a): Pin diagram of high speed ternary full adder (HS-TFA)

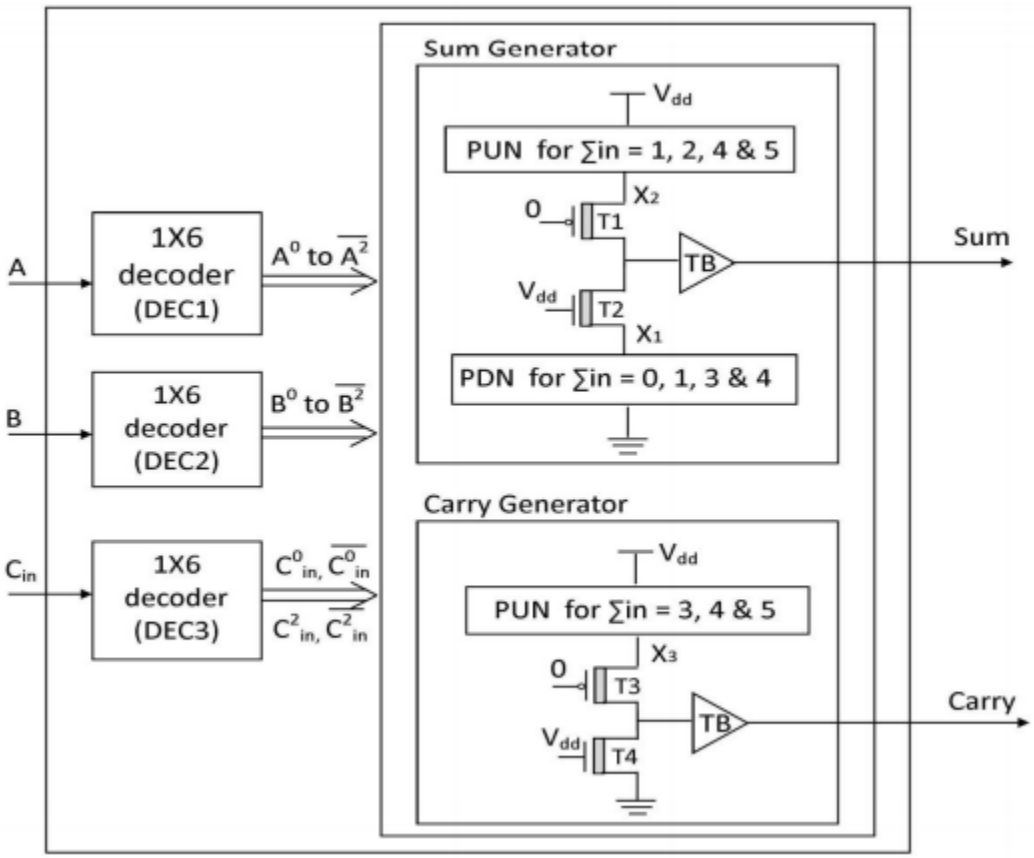


Figure 4.1(b): Block Diagram of high speed ternary full adder (HS-TFA)

Table 4.1: Truth table of ternary full adder (TFA)

A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	2	0
0	2	0	2	0
0	2	1	0	1
1	0	0	1	0
1	0	1	2	0
1	1	0	2	0
1	1	1	0	1
1	2	0	0	1
1	2	1	1	1
2	0	0	2	0
2	0	1	0	1
2	1	0	0	1
2	1	1	1	1
2	2	0	1	1
2	2	1	2	1

Table 4.2: Switching activity for Sum and Carry generator of HS-TFA

$\sum(A+B+C_{in})$			For Sum Generator				For Carry Generator	
	PUN	PDN	X_1	X_2	Sum	PUN	X_3	Carry
0	OFF	ON	0	-	0	OFF	-	0
1	ON	ON	0	2	1	OFF	-	0
2	ON	OFF	-	2	2	OFF	-	0
3	OFF	ON	0	-	0	ON	2	1
4	ON	ON	0	2	1	ON	2	1
5	ON	OFF	-	2	2	ON	2	1

The Carry generator contains a square set apart as 'Play on words for Σin = 3, 4 and 5' which speaks to organize that will exchanged ON when $\sum (A+B+C_{in}) = 3, 4$ and 5. This piece is designed based on its switching exercises required to create Carry. The nitty gritty schematic of Carry generator is appeared in Figure 4.3 (b). Convey generator likewise contains two transistors T3 and T4, which are constantly exchanged ON. They perform voltage division between node voltages X3 what's more, ground, and create Carry as X3/2. Switching of PUN which interfaces carry to V_{dd} for diverse mix of A, B and C_{in}, is additionally given in Table 4.2. Whenever $\sum (A+B+C_{in})$ is more than 2, PUN is exchanged ON and X3 is charged to Vdd, at that point T3 and T4 make Carry equivalent to rationale 1. In the event that $\sum (A+B+C_{in})$ is 0 or 1, Carry is associated with ground just through T4. Further, a ternary buffer (TB) is utilized at the two outputs Sum and Carry to decouple next stage entryway inputs with introduce stage outputs. Additionally, it gives elite without giving up the general vitality effectiveness of TFA.

In light of switching exercises given in Table 4.2 and reality table of TFA given in Table 4.1, X_1, X_2 and X_3 signals are inferred and communicated as:

$$X_1 = 0 * \{A^0(B^0\overline{C_{in}^2} + B^1C_{in}^0 + B^2\overline{C_{in}^0}) + A^1(B^0C_{in}^0 + B^1\overline{C_{in}^0} + B^2\overline{C_{in}^2}) + A^2(B^0C_{in}^0 + B^1\overline{C_{in}^2} + B^2\overline{C_{in}^0})\} \quad \textbf{(4.1)}$$

$$X_2 = 2 * \{\overline{A^0}(\overline{B^0}C_{in}^0 + \overline{B^1}C_{in}^2 + \overline{B^2} * \overline{C_{in}^0}) + \overline{A^1}(\overline{B^0}C_{in}^2 + \overline{B^1}\overline{C_{in}^0} + \overline{B^2}C_{in}^0) + \overline{A^2}(\overline{B^0}\overline{C_{in}^0} + B^1C_{in}^0 + \overline{B^2}C_{in}^2)\} \quad \textbf{(4.2)}$$

$$X_3 = 2 * \{\overline{A^0}\overline{B^2}C_{in}^0 + \overline{A^1}(\overline{B^2}\overline{C_{in}^0} + B^0C_{in}^0) + \overline{A^2}(B^0\overline{C_{in}^0} + C_{in}^0)\} \quad \textbf{(4.3)}$$

Where $A^0, A^2, \overline{A^0}, \overline{A^1}$ and $\overline{A^2}$ are the unary functions of A generated by a 1-to-6-line decoder DEC1; $B^0, B^1, B^2, \overline{B^0}, \overline{B^1}$ and $\overline{B^2}$ are the unary functions of B generated by DEC2; and $C_{in}^0, C_{in}^2, \overline{C_{in}^0}$ and $\overline{C_{in}^2}$ are the unary functions of C_{in} generated by DEC3. Figure 4.2 shows the logic diagram of 1-to-6-line ternary decoder which utilizes design concept. The decoder has one input 'a' and six outputs $a^0, a^1, a^2, \overline{a^0}, \overline{a^1}$ and $\overline{a^2}$ which are known as unary functions. It contains a negative ternary inverter (NTI) followed by a binary inverter to generate a^0 and $\overline{a^0}$, a positive ternary inverter (PTI) followed by a binary inverter to produce 2_a and 2_a, finally a binary NOR gate having inputs as 0_a and 2^a, followed by a binary inverter to get 1_a and 1_a. Table 4.3 shows the unary functions generated by the decoder for input 'a'.

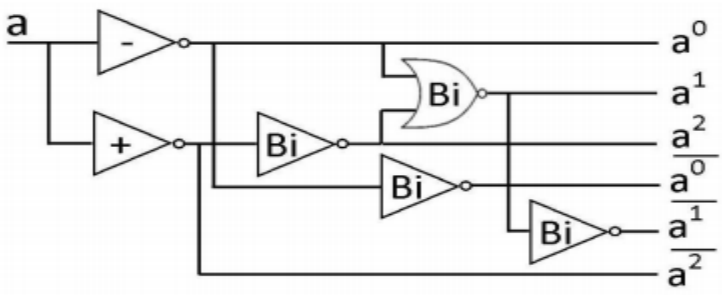


Figure 4.2: Logic level diagram of 1-to-6-line ternary decoder

Table 4.3: Truth table of 1-to-6 ternary decoder

a	a^0	a^1	a^2	$\overline{a^0}$	$\overline{a^1}$	$\overline{a^2}$
0	2	0	0	0	2	2
1	0	2	0	2	0	2
2	0	0	2	2	2	0

The schematic chart of Sum generator and Carry generator of HS-TFA are appeared in Figure 4.3. Play on words of Sum and Carry generator are acknowledged in light of eq. (4.2) and (4.3) utilizing P-CNTFETs. PDN of the Sum generator is built in view of eq. (4.1) utilizing NCNTFETs. For every conceivable mix of A, B and C_{in}, HS-TFA gives a reasonable way for the coveted output rationale esteems. For example, when A = 2, B = 2 and Cin = 0, at that point A2 = B2 = C_{in}^0 = 2, and all other genuine unary capacities are 0. In the circuitry of Sum generator, NCNTFETs whose door are associated with A^2 , B^2 what's more, C_{in}^0 switch ON and make a PD way which makes X1 equivalent to 0. So also, P-CNTFETs whose entryway is associated with $\bar{}A^2$,$\bar{}B^2$what's more, C_{in}^2 turn ON and make a PU way to make X^2 equivalent to 2. T1 and T2 perform voltage division and create rationale 1 at Sum. Presently, in PUN of Carry generator, transistors whose entryways are associated with 0 in $\overline{A^2}, B^2$ and $\overline{C_{in}^0}$ turn ON and make a PU way to create X3 equivalent to 2. At that point T3 and T4 perform voltage division and produces rationale 1 at Carry. Further, the schematic chart of TB is appeared in Figure 4.4, which contains one NTI, one PTI, two binary inverters and two transistors T5 and T6

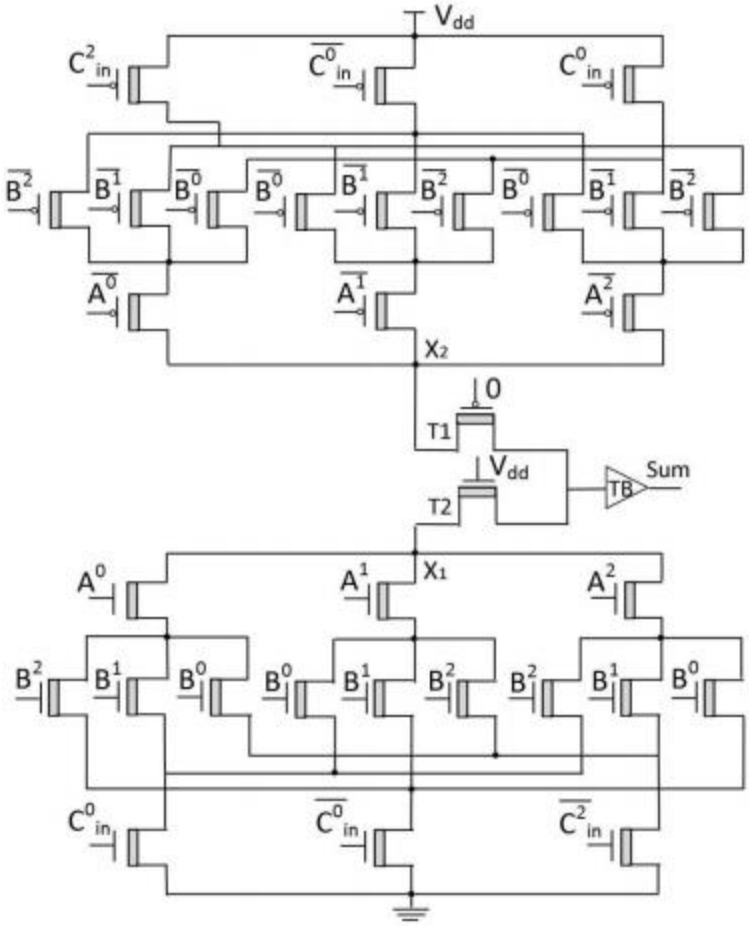


Figure 4.3 (a): Schematic diagram for Sum generator of high speed ternary full adder (HSTFA)

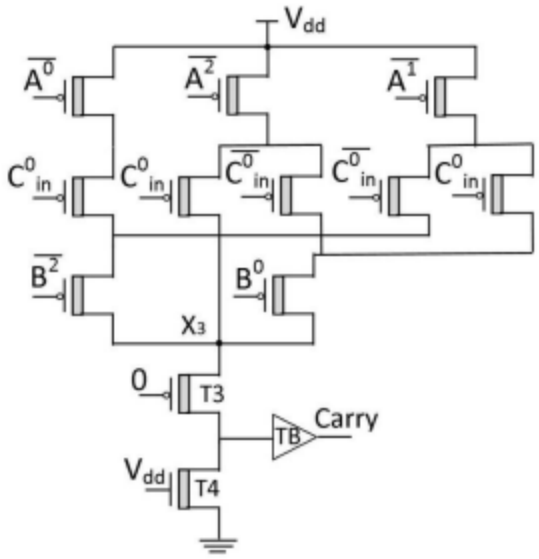


Figure 4.3(b): Schematic diagram for Carry generator of high speed ternary full adder (HSTFA)

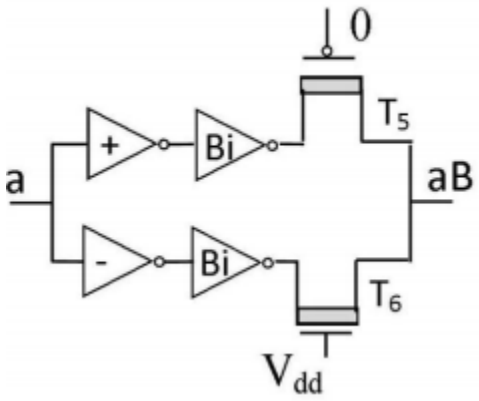


Figure 4.4: Schematic diagram of ternary buffer (TB)

4.2.2 Low Power TFA (LP-TFA)

The stick graph and piece outline of the second proposed TFA are appeared in Figure 4.5. This TFA is designed for pass transistor rationale style keeping in mind the end goal to accomplish low power and named as low power TFA (LP-TFA). Sources of info A and B are gone through 1-to-5-line decoders (DEC1 and DEC2) to create their unary capacities. Info C_{in} is gone through a NTI and a binary inverter. LP-TFA contains a Sum generator to create Sum and ¯Sum signals, and a Convey generator to create Carry flag. The Sum generator is designed in light of complementary pass-transistor rationale (CPL) style. It comprises of two N-CNTFET based

pass-transistor networks; one for each flag rail (Sum also, Whole). These N-CNTFET networks pass rationale 0 and rationale 1 yet it debases rationale 2 due to the limit voltage drop over the N-sort transistors. This rationale degradation makes swing (or, on the other hand level) restoration important for Sum (and Aggregate) keeping in mind the end goal to maintain a strategic distance from static streams at the resulting output circuitry. As an outcome, two little P-CNTFETs T1 and T2 are utilized for level restoration of rationale 2. Furthermore, TB is utilized to get fast and high driving capacity without relinquishing the general energy efficiency of the design.

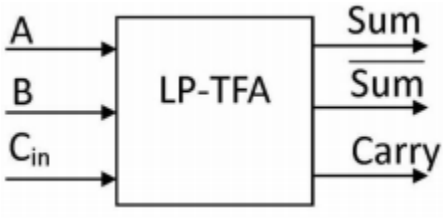


Figure 4.5 (a): Pin diagram of low power ternary full adder (LP-TFA)

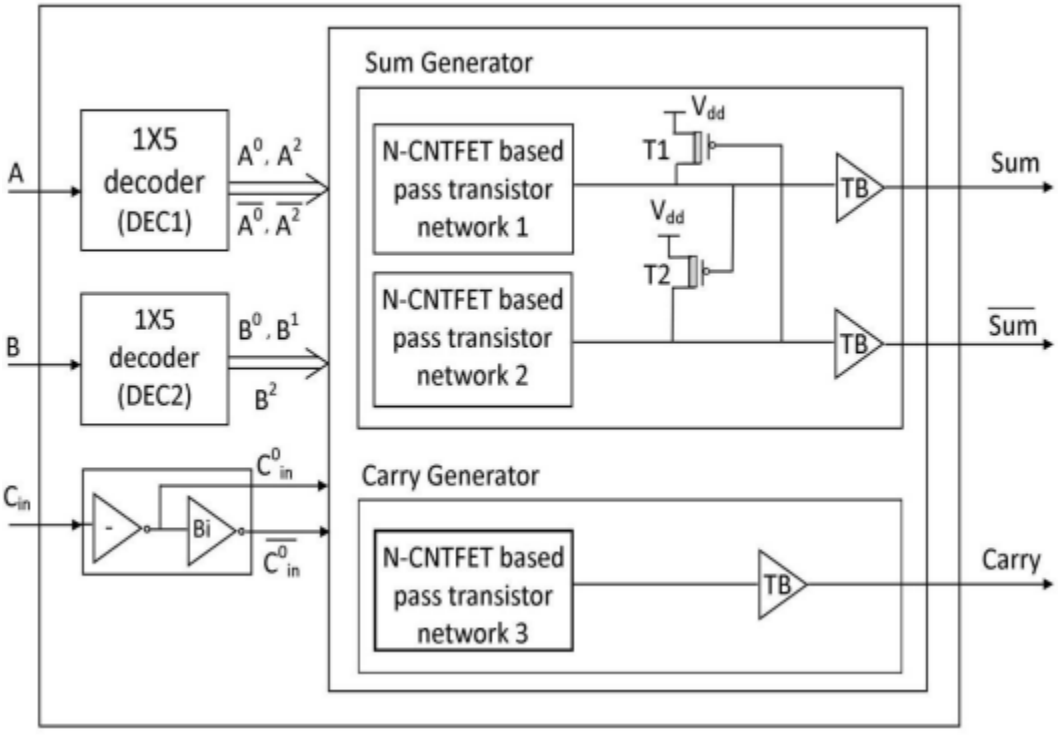


Figure 4.5 (b): Block diagram of low power ternary full adder (LP-TFA)

Carry generator of LP-TFA contains just a single N-CNTFET pass transistor organize in light of the fact that no swing restoration is required for Carry motion as its greatest voltage level is $V_{dd}/2$ as it were. From reality table given in Table 4.1, K-outline LP-TFA design is attracted and appeared Figure 4.6 where An and B are ternary signs and Cin is the binary flag (0 and 1). In light of K-outline, switch level rationale articulations of Sum and Carry are inferred and communicated as:

$$Sum = P_1 * C_{in}^0 + P_2 * \overline{C_{in}^0} \quad \textbf{(4.4)}$$

$$Carry = P_3 * C_{in}^0 + P_4 * \overline{C_{in}^0} \quad \textbf{(4.5)}$$

Here, signals P_1 and P_2 are equal to Sum when C_{in} = 0 and C_{in} = 1, respectively. Simplified expressions of P_1 and P_2 are expressed as follows.

$$P_1 = A * B^0 + (1 * A^0 + \overline{A^2} * \overline{A^0})B^1 + (A^0 * \overline{A^2} + 1 * A^2)B^2 \quad \textbf{(4.6)}$$

$$P_2 = A * B^2 + (A^0 + \overline{A^2} + 1 * A^2)B^1 + (\overline{A^2} * \overline{A^0} + 1 * A^0)B^0 \quad \textbf{(4.7)}$$

Similarly, signals P3 and P4 are equal to the Carry signal when C_{in} = 0 and C_{in} = 1, respectively, and their simplified expressions are as:

$$P_3 = 0 * A^0 + 0 * B^0 + 0 * \overline{A^2}\,\overline{B^2} + 1 * B^2\overline{A^0} + 1 * A^2\overline{B^0} \quad \textbf{(4.8)}$$

$$P_4 = 1 * B^2 + 1 * A^2 + 1 * \overline{A^0}\,\overline{B^0} + 0 * A^0\overline{B^2}+) * B^0\overline{A^2} \quad \textbf{(4.10)}$$

Where $A^0, \overline{A^0}, A^2, \text{and } \overline{A^2}$ the unary elements of A are produced by a 1-to-5-line decoder DEC1; $B^0, B^1 \text{ and } B^2$ are the unary elements of B, produced by decoder DEC2. C_{in}^0 and $\overline{C_{in}^0}$ are produced by a NTI and a binary inverter. The schematic chart of a 1-to-5-line decoder is

appeared in Figure 4.7. It contains one NTI, one PTI and one binary inverter and one binary NOR door for the generation of unary capacities.

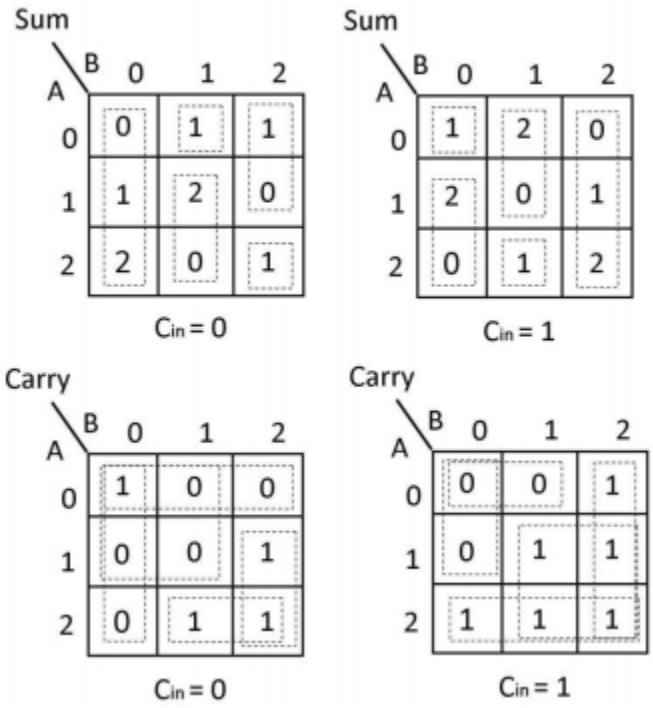


Figure 4.6: K-map of low power ternary full adder (LP-TFA) for (a) Sum (b) Carry

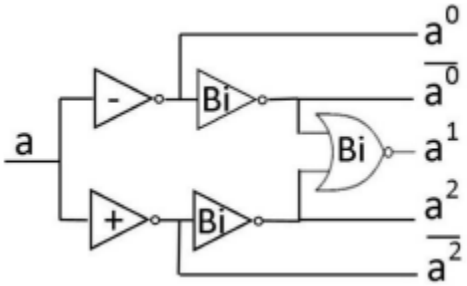


Figure 4.7: Schematic diagram of a 1-to-5-line ternary decoder

The schematic chart of Sum generator and Carry generator of CNTFET-based LP-TFA are appeared in Figure 4.8. Two transistors T3 and T4 perform voltage division in the vicinity of 0 and V_{dd} and create V_x equivalent to $V_{dd}/2$. N-CNTFET pass transistor based system 1 of Sum generator acknowledges P_1 and P_2 in light of the eq. (4.6) and (4.7), separately. As indicated by eq. (4.4), these signs are gone through transistors T5 and T6 to create Sum. Essentially, NCNTFET pass transistor based system 2 of Sum generator figures it out $\bar{P}_1$and $\bar{P}_2$ which are gone through transistors T7 and T8 to produce Aggregate. Keeping in mind the end goal to get

level rebuilding for rationale 2, transistor T1 and T2 are used. Since level rebuilding is not required for rationale 1, these transistors ought to OFF when Sum and Aggregate are equivalent to rationale 1. For this, the edge voltage of T1 and T2 are set as 0.55V which is more prominent than voltage level of rationale 1 (0.45V). TB appeared in Figure 4.4 is utilized at Sum and Entirety for output buffering circuitry.

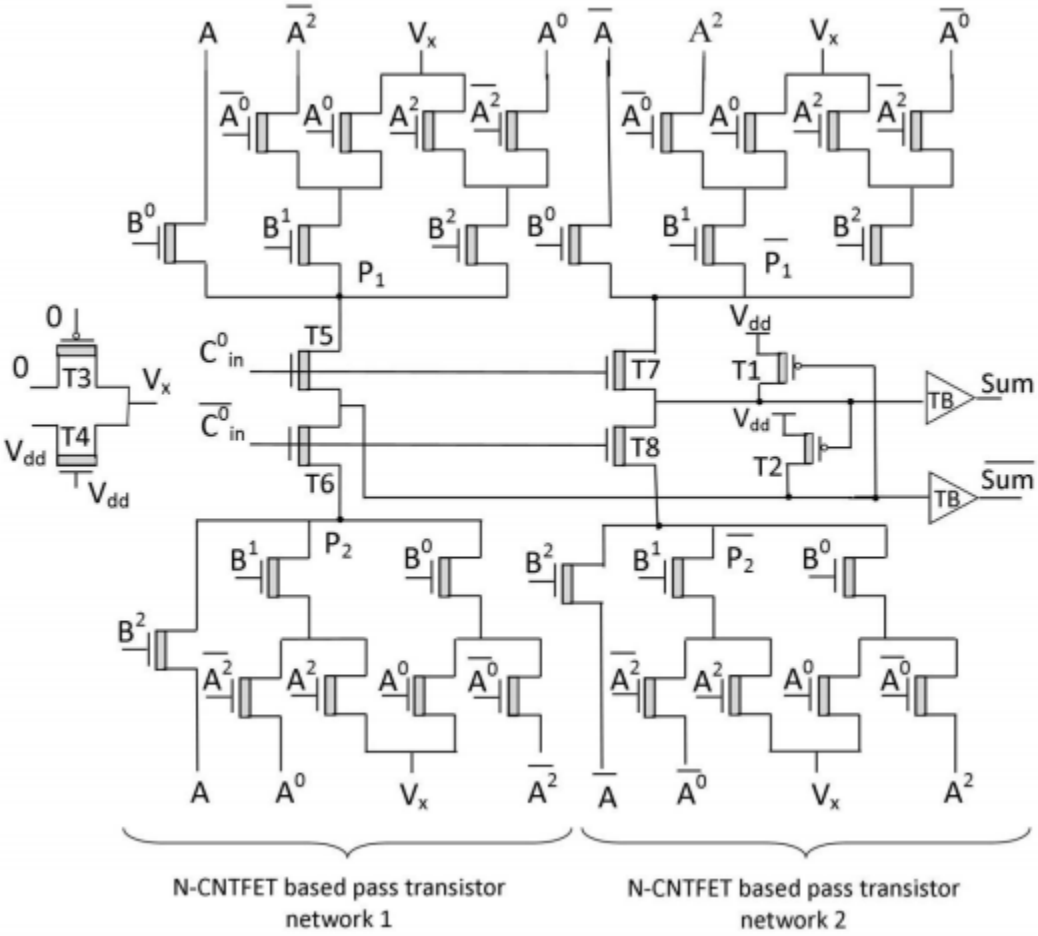


Figure 4.8(a): Schematic diagram of Sum generator of low power ternary full adder (LPTFA)

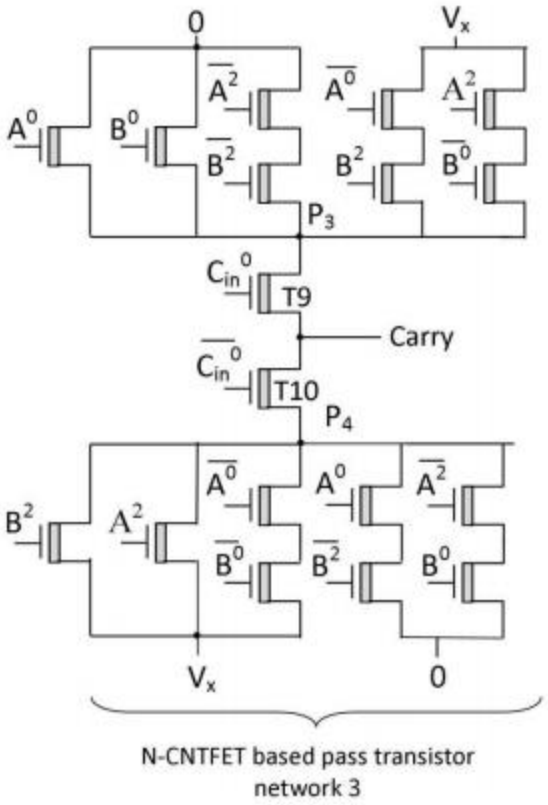


Figure 4.8(b): Schematic diagram of Carry generator of low power ternary full adder (LPTFA)

NCNTFET pass transistor based system 3 of Carry generator acknowledges P3 and P4 in light of the eq. (4.8) and (4.9), individually. At that point, as indicated by the eq. (4.5), these signs are passed through transistors T9 and T10 to create Carry

For all the conceivable conditions of A, B and Cin, LP-TFA gives appropriate way that deliver wanted output rationale. For example, when A = B = 2, at that point $A^2 = B^2 = 2$ and all other unary capacities are 0. Consider Sum generator circuit first; N-CNTFETs whose entryways are associated with $A^2$and B^2 are ON. They exchange V_x (rationale 1) to both P_1 and P_1 what's more, exchange A (rationale 2) and $\bar{}A$(rationale 0) to P_2 and $\bar{}P_2$ separately. At the point when Cin = 0, at that point 0 Cin = 2. T5 and T7 are ON, which pass rationale 1 to Sum and Entirety, separately. At the point when C_{in} = 1, T6, T8 and T2 are ON, which pass rationale 2 and rationale 0 to Sum and Whole, individually. Correspondingly, for Carry generator circuit, N-CNTFETs whose entryways are associated with A2, 0 B also, B2 turn ON, and exchange V_x to both P_3 and P_4. At the point when C_{in} = 0, at that point Cin 0 = 2. T9 is ON which pass P3 (rationale 1) to Carry. At the point when Cin = 1, at that point 0 C_{in} = 2. T10 is ON which pass P_4 (rationale 1) to Carry. LP-TFA usage reduces transistor overhead around by 51% for Carry and dispenses with the need of one additional power supply ($V_{dd}/2$) for rationale 1 as for CPL based CMOS TFA circuit displayed in [161].

4.2.3 Dynamic TFA (DTFA)

The stick graph and square outline of the third proposed TFA are appeared in Figure 4.9. TFA is designed for dynamic rationale style keeping in mind the end goal to accomplish superior and named as dynamic TFA (DTFA). DTFA has five information sources A, B, C_{in}, CLK and $\bar{}$CLK , and two outputs Total and Carry. Sources of info An and B are gone through 1-to-4-line decoders (DEC1 and DEC2) to create their unary capacities. Info Cin is gone through a NTI and a binary inverter. Two transistors T1 and T2 perform voltage division in the vicinity of 0 and V_{dd} to create voltage V_{dd}m (equivalent to Vdd/2) for rationale 1 at outputs. DTFA contains a Sum generator and a Carry generator to create Sum and Carry signals. The Sum generator contains three clock worked transistors T3, T4 and T5, which are in charge of dynamic operation of DTFA. A pull-up organize (i.e. PUN1) and a pull-down arrange (i.e. PDN1) are utilized to get rationale 2 and rationale 0 for Sum. DTFA utilizes a guardian designed for ternary rationale (named as ternary manager) to ease charge sharing issues.

Moreover, TB is utilized at the output to decouple next stage entryway contributions with exhibit stage output and in addition to give high output driving capacities without sacrificing the general vitality effectiveness of the design. Convey generator of TFA contains two clock worked transistors T6 and T7, and one pulldown arrange (i.e. PDN2) just because of the binary nature (0 and 1) of Carry flag. Like Aggregate generator, it utilizes ternary manager and TB at the output.

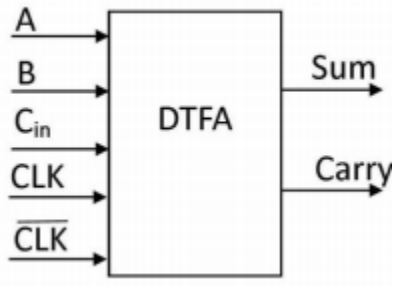


Figure 4.9(a): Pin diagram of dynamic ternary full adder (DTFA)

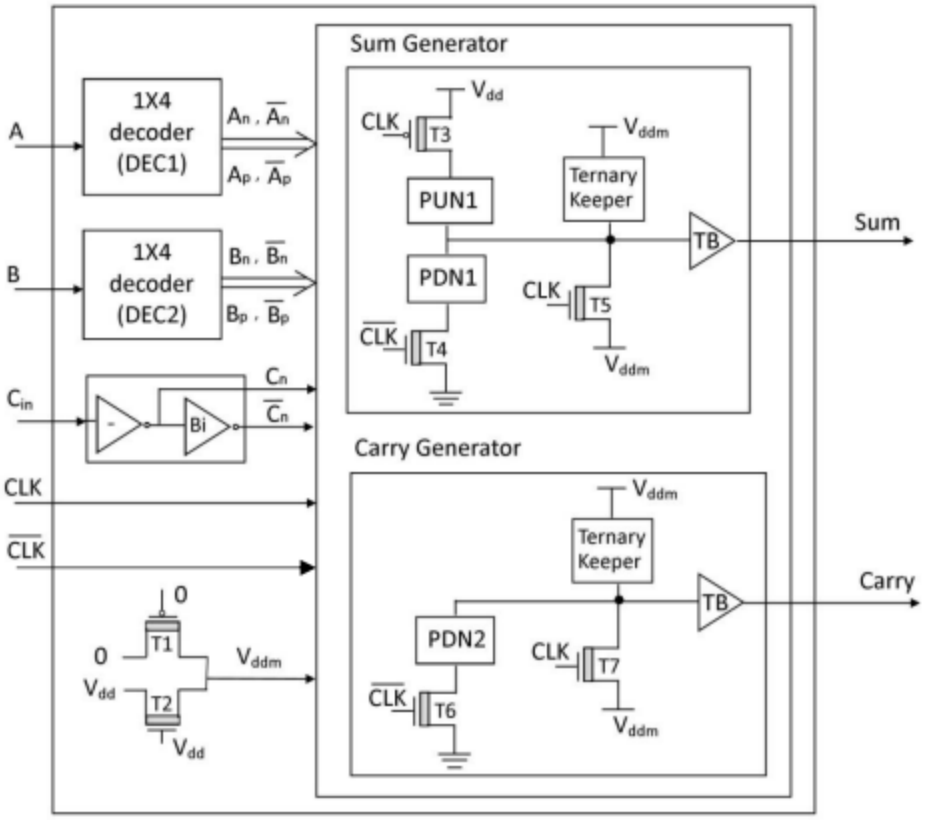


Figure 4.9 (b): Block diagram of dynamic ternary full adder (DTFA)

The schematic outline of Sum generator and Carry generator of CNTFET-based DTFA are appeared in Figure 4.10. Information sources $A_n, \overline{A_n}, A_p$ and $\overline{A_p}$ are the unary elements of A created by DEC1; $B_n, \overline{B_n}, B_p$ and $\overline{B_p}$ are the unary elements of B created by DEC2; and B_n and $\overline{B_n}$ are created by a NTI and took after binary inverter. The schematic chart of 1-to-4-line ternary decoder is appeared in Figure 4.11. It contains one NTI, one PTI and two binary inverters for the generation of unary capacities. PUN1 and PDN1 of Sum generator, and PDN2 of Carry generator are acknowledged in light of truth table of TFA given in Table 4.1. For creating Sum equivalent to 2 and 0, there is constantly one pull-up (PU) way and pull-down (PD) way exist in Sum generator. For making Carry equivalent to 0, a PD way exists in Carry generator circuit. To limit sub-edge leakage current, PUN and PDN utilize CNTFETs with littler diameter which is picked as 0.626 nm.

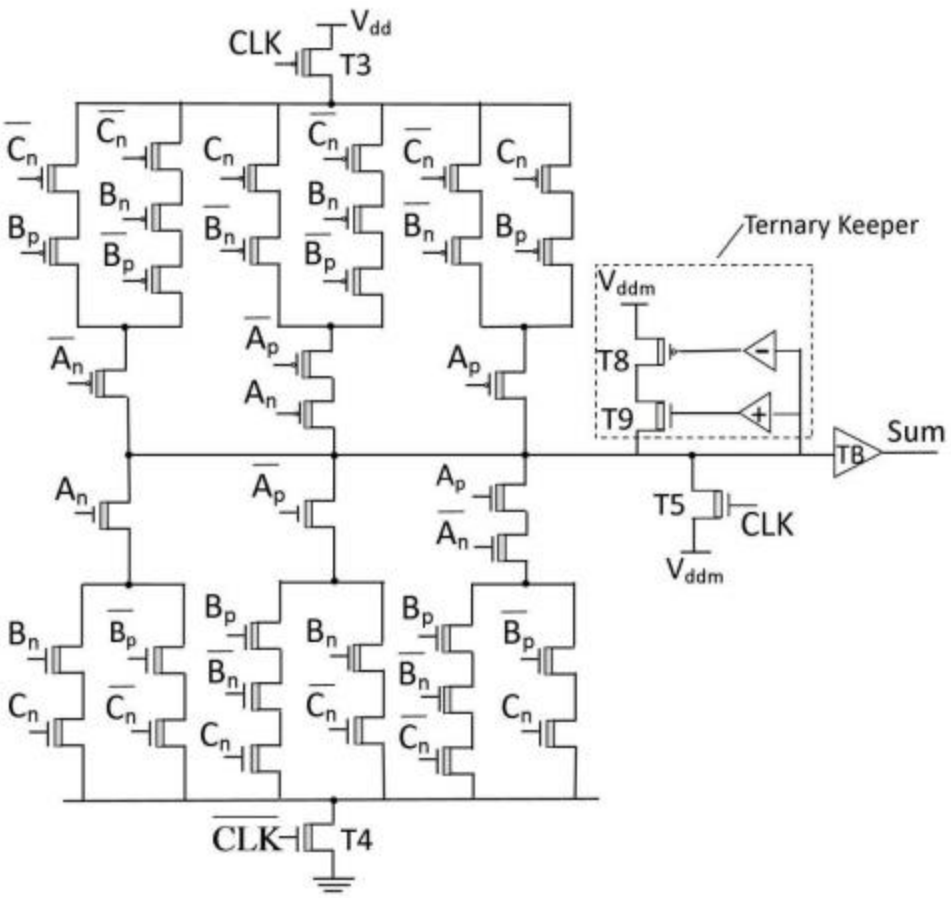


Figure 4.10(a): Schematic diagram of Sum generator of dynamic ternary full adder (DTFA)

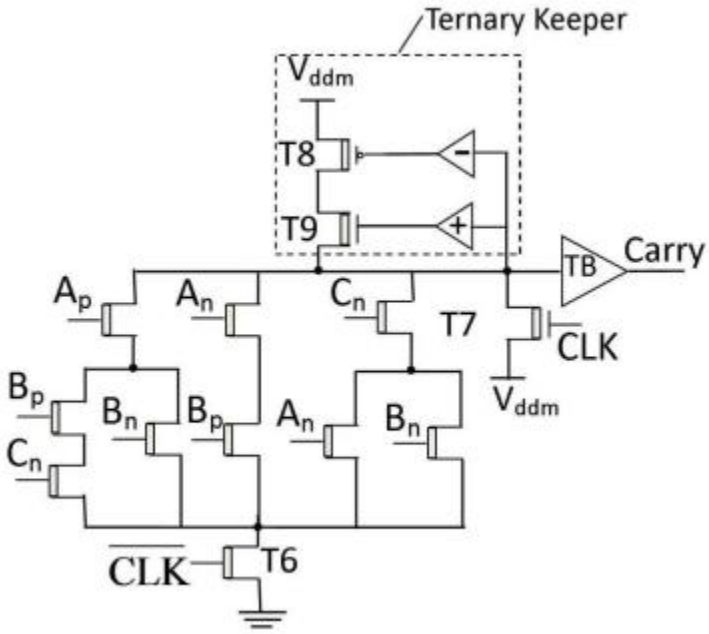


Figure 4.10(b): Schematic diagram of Carry generator of dynamic ternary full adder (DTFA)

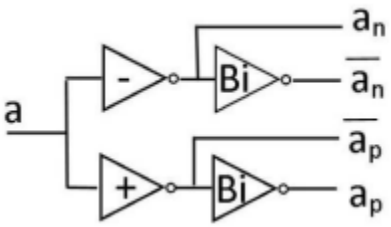


Figure 4.11: Schematic diagram of 1-to-4 ternary decoder

DTFA operation is isolated into two stages precharge stage and evaluation stage.

1) Precharge stage: When CLK = 1, Sum and Carry are precharged to V_{ddm} (rationale 1) through T5 and T7, separately. Amid this stage, evaluation transistors T3, T4 and T6 are OFF and henceforth, pull-up (to rationale 2) and pull-down (to rationale 0) ways are crippled.

2) Evaluation stage: For CLK = 0, precharge transistors T5 and T7 are OFF and, evaluation transistors T3, T4 and T6 are ON. Whole flag is restrictively charged to rationale 2 and released to rationale 0 in view of the Sum generator pull-up and pull-down topology, separately, alongside input esteems. Likewise, Carry flag is restrictively released to rationale 0 in view of the information esteems and Carry generator pull down topology. In the event that all PU also, PD ways are killed, Sum and Carry stay at their precharged esteems (rationale 1) which are additionally kept up by ternary managers. The attendant circuit contains transistors T8 and T9, driven by NTI and PTI, individually as appeared in Figure 4.10. Manager is initiated just when Sum (and Carry) is set to rationale 1. Estimating of T8 and T9 is kept littler (i.e. number of CNTs = 2) than the proportional examining of other pull and pulldown transistors with the goal that coveted output level can be acquired. TB appeared in Figure 4.4, is utilized at Sum and Carry for output buffering circuitry. Keeping in mind the end goal to spare eight transistors, normal NTI and PTI are utilized as a part of both ternary guardian and TB of Sum generator and Convey generator.

4.2.4 Results and Discussion

In this segment, proposed designs of TFA are investigated and assessed under different test conditions utilizing Synopsis HSPICE test system with 32nm Stanford CNTFET model which

considers down to earth non-idealities of CNTFET. Subtle elements of the Stanford demonstrate have been given in segment 2.2 of section 2. In TFA designs, the chirality vector of CNTFETs used for voltage divider is (14, 0). The limit voltage of these transistors is 0.392 V with the diameter of 1.096 nm. The chirality vector of PUN and PDN transistors of DTFA are (8, 0). The limit voltage of these transistors is 0.686 V with the diameter of 0.624 nm. The chirality vector of outstanding CNTFETs of all TFA designs is (19, 0). The limit voltage of these transistors is 0.289 V with the diameter of 1.487 nm. The other innovation parameters of CNTFET have same esteems as specified in area 2.2 of part 2. For examination of proposed designs, as of late distributed CNTFET-based TFA designs of [212] what's more, [213] are duplicated. Further, design of ternary half snake (THA) introduced in [199] leads to vitality productive and minimal design as for other CNTFET-based THA circuits. As a outcome, TFA is additionally executed utilizing the design strategy of [199] and alluded as CNTFET-based TFA of [199]. In this TFA, Vdd/2 is produced utilizing an indistinguishable technique from utilized as a part of LP-TFA and DTFA, so as to perform examination with proposed TFA designs which don't have any additional power supply. For replicated designs, chirality vector of CNTFETs and esteem of other gadget parameters are picked by the data given in the individual papers from the literature.

Simulation Setup

Every one of the designs are recreated at room temperature, at 250MHz working frequency and at 0.9 V power supply voltage. Also, a capacitor of 2.1fF is associated at all output nodes of the circuit to incorporate loading effects. An entire info design including every one of the 324 conceivable input transitions is connected to the circuit. Add up to 387 delays which consider all Sum and Carry transitions are measured. For static TFA (HS-TFA, LP-TFA, TFA of [199], [212] and delay is measured from half of voltage level of contribution to half of voltage level of output. For DTFA, delay is computed from half of voltage level of clock flag (CLK) to half of voltage level of output since outputs seem just when clock flag makes transition from rationale 2 to rationale 0 for evaluation stage. The greatest estimation of measured delay is expressed as the delay of the circuit. The power consumption of the circuits incorporates power from supply (V_{dd}) and info sources (and clock likewise for DTFA). To get this, normal power from V_{dd}, input sources and clock are measured independently with the example of 324 info transitions for quite a while period, and after that additional. Albeit some of info transitions may not modify the

estimations of the output nodes, they could cause switching exercises at inside nodes bringing about some power consumption. As a result, an info design of every single conceivable transition affirms that deliberate normal power consumption is a precise estimation of the power consumption of the circuit. Because of the exchange off between power consumption and delay, circuits are additionally assessed in view of PDP which is processed by increase of the normal power consumption and greatest delay. Further, to assess the performance at TALU architecture level, information ways accessible in HO-TALU, which contains decoder, FSB-AHO, TGB-AHE and TFA piece, have been reproduced.

Evaluation of Proposed TFA

Figure 4.12 demonstrates the specimen transient waveform of HS-TFA. The initial three wave shapes speak to inputs A, B and C_{in}, and the last two wave frames indicate Sum and Carry signals which authenticate its right operation. Transient wave types of LP-TFA and DTFA are incorporated into Appendix.

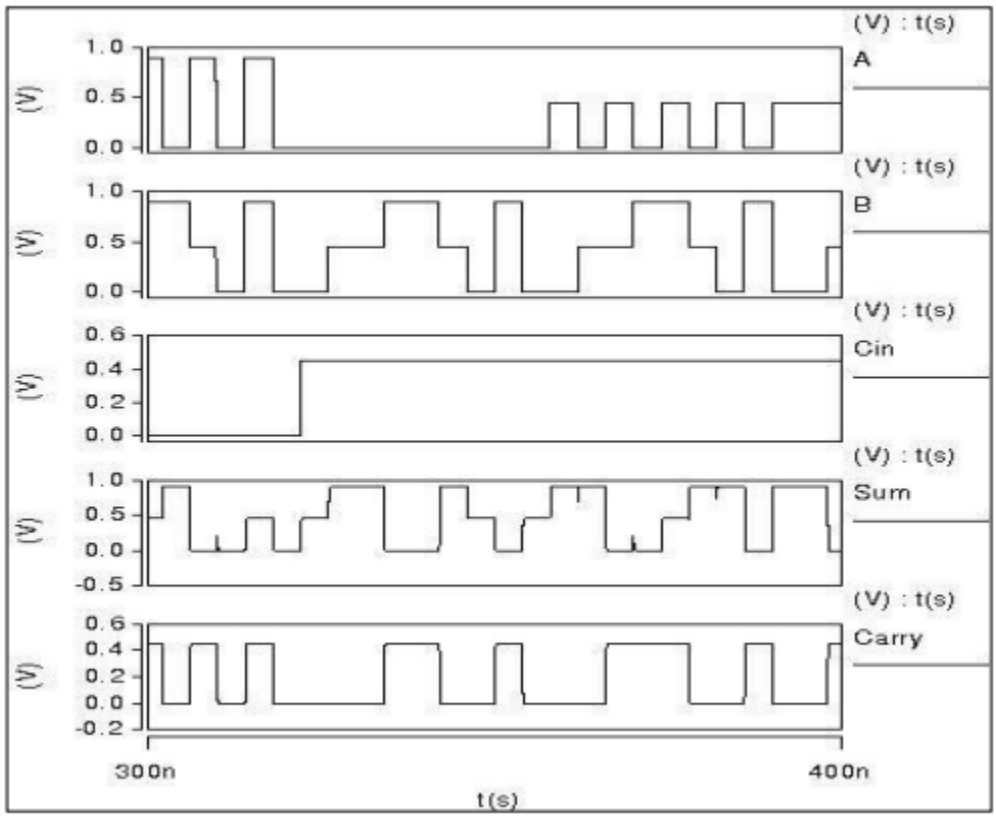


Figure 4.12: Transient waveform of high speed ternary full adder (HS-TFA)

An examination on delay, power consumption, PDP and gadget number of CNTFET-based TFA designs is appeared in Table 4.4. Simulation comes about demonstrate that HS-TFA works quicker among all the CNTFET-based static designs. In examination with TFA of [199], HS-TFA picks up diminishment in delay and gadget number by 9% furthermore, half, separately, yet consumes 69.7% more power. Contrasted with the design of [212], HS-TFA accomplishes lessening in delay and gadget check by 49% and 13%, individually; however it consumes 36.8% more power. In examination with TFA,HS-TFA works 16% speedier with 87% decreased Power and 25% less gadget number. Also, performance parameters extricated at architecture level, are appeared in Table 2 of Appendix II.

As per above detailed outcomes, LP-TFA has the most minimal power among all the CNTFETbased TFA designs. Contrasted with the design LP-TFA consumes less power by 24% with diminishment in gadget number by 52% however it has 20% more delay. In examination with TFA.It accomplishes lessening in delay, power and gadget number by 30.5%, 66.6% and 16%, separately. Contrasted with the design of [213], LP-TFA consumes less power by 97% with lessening in gadget number by 28% yet it has 13% more delay.

Simulation comes about recorded in Table 4.4 demonstrate that DTFA accomplishes most reduced delay and PDP among all the CNTFET-based designs. In correlation with the design of, it picks up decrease in delay, power and gadget tally by 24%, 15% and 51%, individually. Looked at to the design DTFA gets preferences in delay, power and PDP by 57.6%, 62.5% furthermore, 14%, individually. Essentially, it demonstrates 98% less power, 30% less delay and 28% less gadget tally, concerning the TFA design. As indicated by the directed simulation comes about, TFA have PDP of same request while TFA has higher request of PDP, in this manner, proposed TFAs are contrasted and design of just in the following simulations.

Table 4.4: Simulation results of CNTFET-based ternary full adder (TFA) design

Circuits	Delay ($\times 10^{-10}$ S)	Power ($\times 10^{-6}$ W)	PDP ($\times 10^{-16}$ J)	Device Count
HS-TFA (proposed)	0.73	6.89	5.05	106
LP-TFA (proposed)	1.00	1.45	1.45	102
DTFA (proposed)	0.61	1.63	0.99	105
TFA of [199]	0.80	1.91	1.53	214
TFA of [212]	1.44	4.35	6.26	122
TFA of [213]	0.87	53.7	46.7	142

As the driving ability is a critical parameter for an advanced circuit, proposed TFA designs are tried under various loading conditions to inspect their driving capacity. For this reason, simulations are performed with various estimations of output stack extending from 2 fF to 6 fF at room temperature with 0.9 V power supply and 250 MHz working frequency. The delay, power consumption and PDP of TFA designs versus stack capacitor are plotted in Figure 4.13. In spite of the fact that HS-TFA has high power consumption and high PDP variety, it indicates less delay and its variety contrasted with that of other static designs (LP-TFA, TFA at all estimations of output stack. Figure 4.13 demonstrates that LP-TFA accomplishes less power in examination with that of other TFA designs under all loading condition. Likewise, it demonstrates marginal abatement in PDP variety however high delay variety concerning other static designs at all output loads. It can be seen that DTFA gets bring down delay and PDP too as their variety, than other TFA designs on various burdens. In this way, the predominance of DTFA and HS-TFA turns out to be more extensive with expanded load capacitance, which demonstrates their high driving ability contrasted with existing TFA designs. To look at the performance of TFA designs at various frequencies, simulations are directed at working frequency shifting from 100 MHz to 1000 MHz with room temperature, 0.9 V power supply and 2.1 fF output stack. The power consumption of ternary circuits is plotted in Figure 4.14. As per the simulation comes about, proposed TFA designs work legitimately and, LP-TFA and DTFA expends less power however

HS-TFA has high power consumption contrasted with existing TFA designs, at various frequencies.

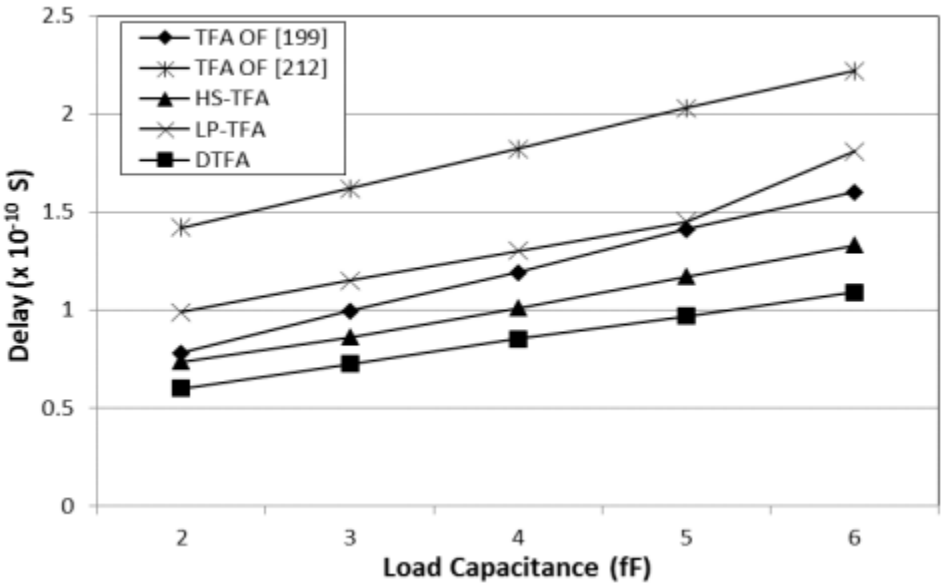


Figure 4.13 (a): Delay versus output load capacitor plot for five ternary full adder (TFA) designs

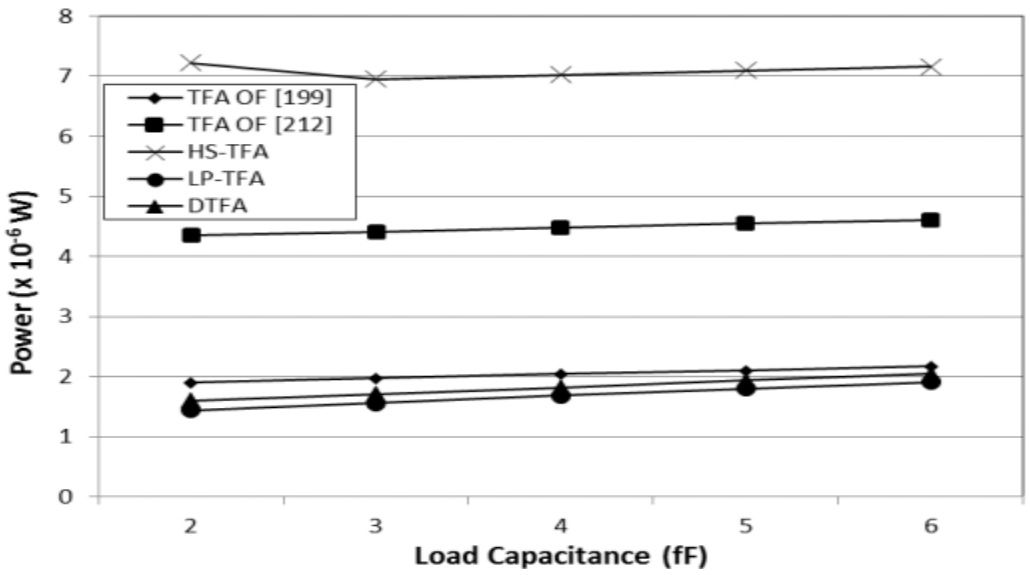


Figure 4.13 (b): Power consumption versus output load capacitor plot for five ternary full adder (TFA) designs

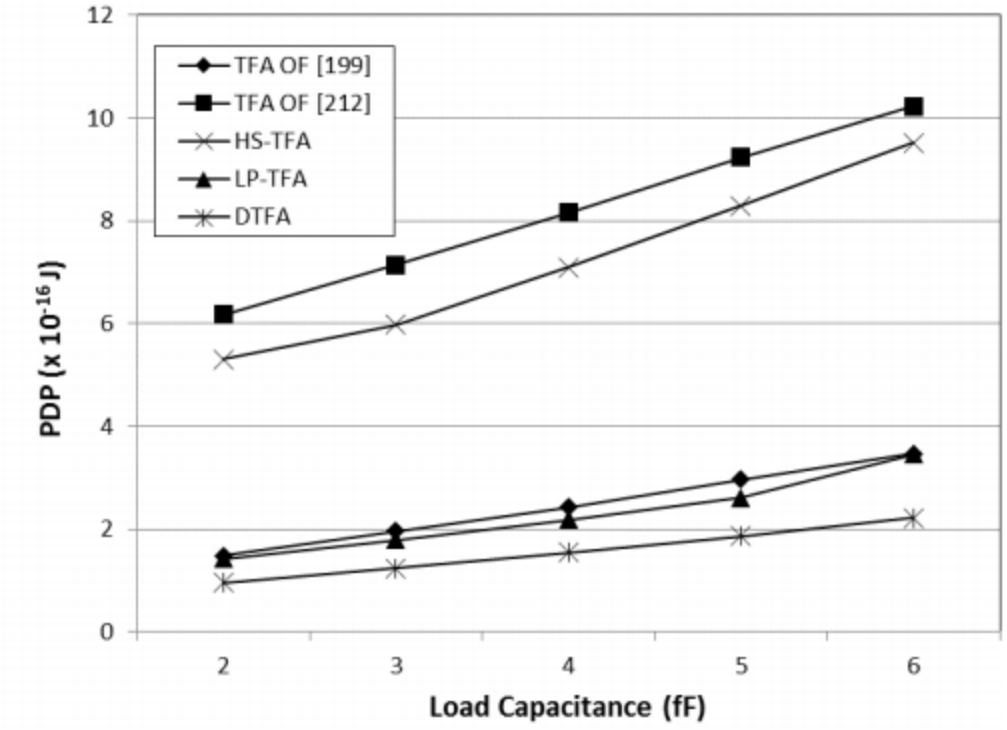


Figure 4.13 (c): Power-delay product (PDP) versus output load capacitor plot for five ternary full adder (TFA) designs

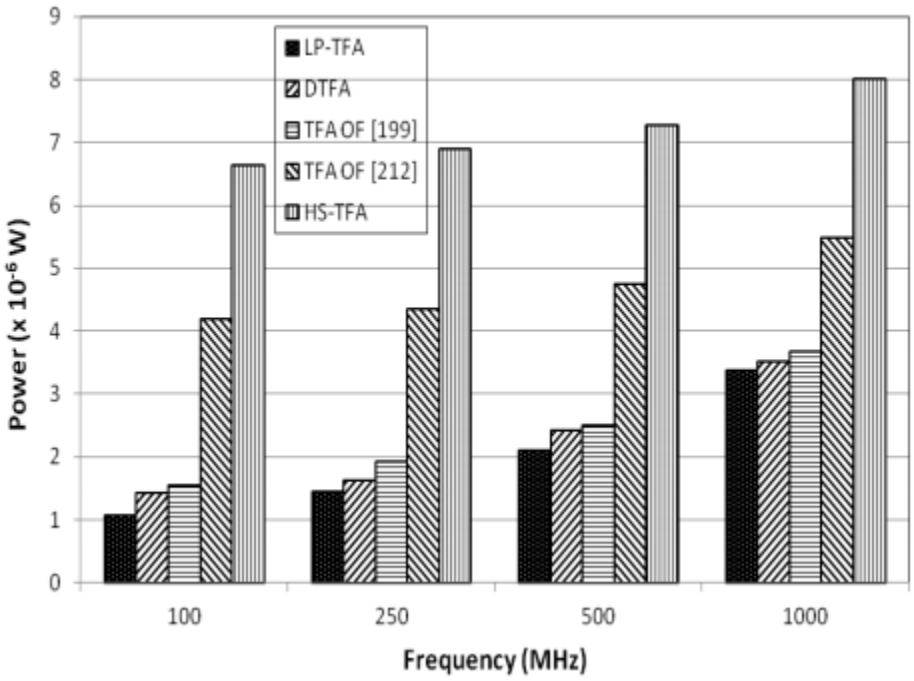


Figure 4.14: Power consumption versus operating frequency plot for five ternary full adder (TFA) designs

As the driving ability is a critical parameter for an advanced circuit, proposed TFA designs are tried under various loading conditions to inspect their driving capacity. For this reason, simulations are performed with various estimations of output stack extending from 2 fF to 6 fF at room temperature with 0.9 V power supply and 250 MHz working frequency. The delay, power consumption and PDP of TFA designs versus stack capacitor are plotted in Figure 4.13. In spite of the fact that HS-TFA has high power consumption and high PDP variety, it indicates less delay and its variety contrasted with that of other static designs (LP-TFA, TFA)at all estimations of output stack. Figure 4.13 demonstrates that LP-TFA accomplishes less power in examination with that of other TFA designs under all loading condition. Likewise, it demonstrates marginal abatement in PDP variety however high delay variety concerning other static designs at all output loads. It can be seen that DTFA gets bring down delay and PDP too as their variety, than other TFA designs on various burdens. In this way, the predominance of DTFA and HS-TFA turns out to be more extensive with expanded load capacitance, which demonstrates their high driving ability contrasted with existing TFA designs.

To look at the performance of TFA designs at various frequencies, simulations are directed at working frequency shifting from 100 MHz to 1000 MHz with room temperature, 0.9 V power supply and 2.1 fF output stack. The power consumption of ternary circuits is plotted in Figure 4.14. As per the simulation comes about, proposed TFA designs work legitimately and, LP-TFA and DTFA expends less power however HS-TFA has high power consumption contrasted with existing TFA designs, at various frequencies.

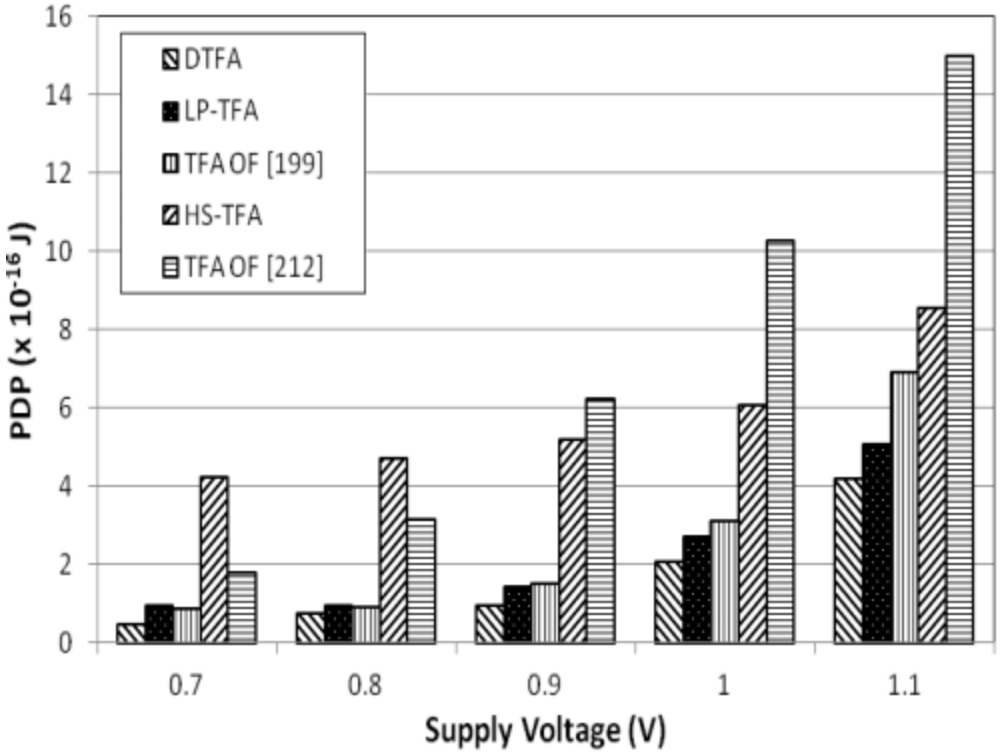


Figure 4.15: Power-delay product (PDP) versus supply voltage plot for five ternary full adder (TFA) designs

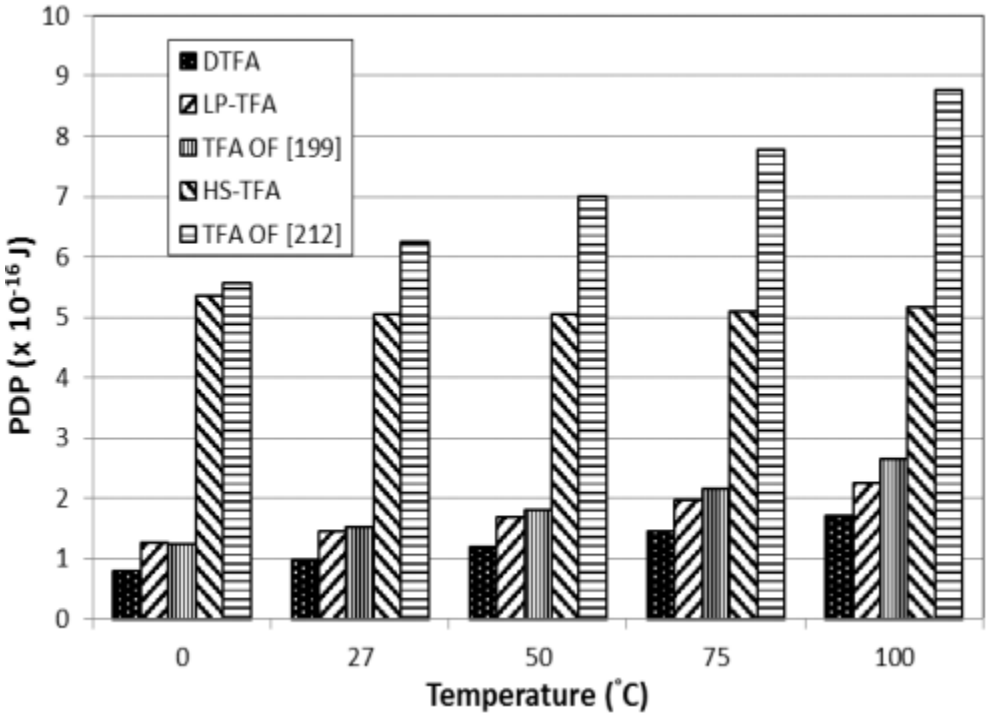


Figure 4.16: Power-delay product (PDP) versus temperature plot for five ternary full adder (TFA) designs

4.3 Design of Comparator Module

Regular designs of ternary comparator exhibited in [73], [206] and [252], create three essential outputs: GR, LE and EQ that indicate A > B, A < B and A = B conditions, individually. At the point when A > B, outputs GR, LE and EQ moves toward becoming 2, 0 and 0, individually. For A < B, outputs GR, LE and EQ are 0, 2 and 0, correspondingly. Essentially, when A = B, outputs GR, LE and EQ moves toward becoming 0, 0 and 2, individually. It is watched that lone two outputs are adequate to translate the magnitude relationship amongst An and B, as appeared in Table 4.5. Consequently, just two outputs GR and EQ are considered for the reaction of proposed comparator. Be that as it may, it makes the disentangling rationale of comparator reaction complex in those applications where three outputs are coveted.

Table 4.5: Decoding of outputs for comparison response

Comparator Outputs		Results
GR	EQ	
2	0	A > B
0	2	A = B
0	0	A < B
2	2	Invalid

4.3.1 1-bit Comparator

The stick outline and piece graph of proposed 1-bit comparator are appeared in Figure 4.17. 1-bit comparator thinks about two 1-bit ternary numbers (An and B) and creates outputs GR what's more, EQ. Information sources An is gone through a NTI and a PTI to produce A_n and A_p,

individually. Essentially, B is gone through a NTI and a PTI to produce B_n and B_p, correspondingly. 1-bit comparator is designed in view of pass transistor rationale style. It contains network1 and arranges 2 for generation of GR and EQ, separately. Reality table of 1-bit comparator is given in Table 4.6. In view of this table, K-maps are drawn for GR and EQ, and appeared in Figure 4.18. From K-maps, switch level articulations of these outputs are inferred and communicated as:

$$GR = 0 * A_n + B_n * A_n A_p + B_p * A_p \quad \textbf{(4.10)}$$

$$EQ = A_n * B_n + (0 * A_n + A_p * A_n) B_n B_p + (0 * A_p + 2 * A_p) B_p \quad \textbf{(4.11)}$$

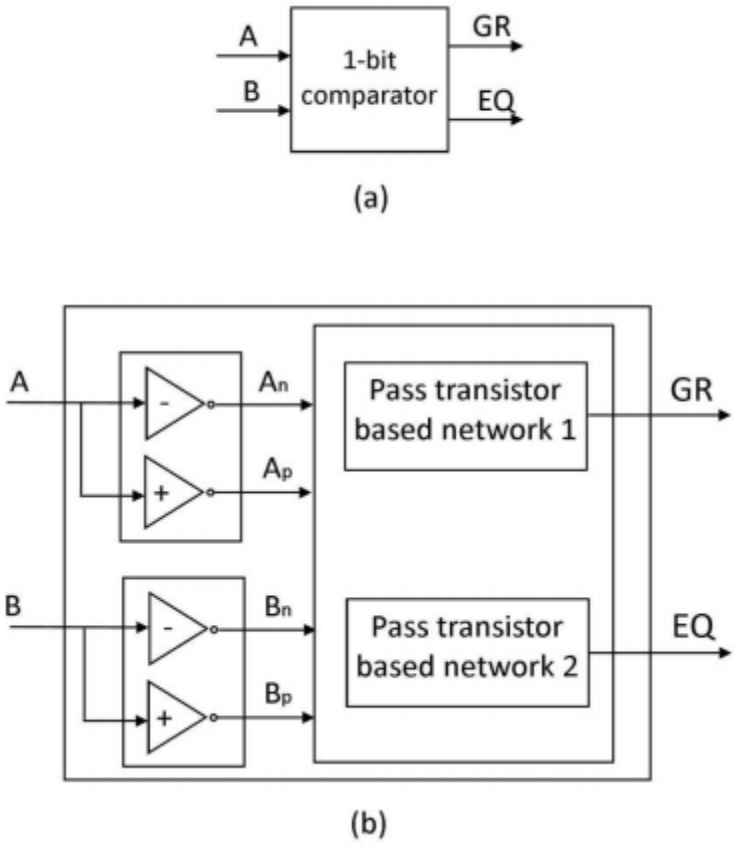


Figure 4.17 1-bit ternary comparator (a) pin diagram (b) block diagram

Table 4.6: Truth table of 1-bit comparator

A	B	GR	EQ
0	0	0	2
0	1	0	0
0	2	0	0
1	0	2	0
1	1	0	2
1	2	0	0
2	0	2	0
2	1	2	0
2	2	0	2

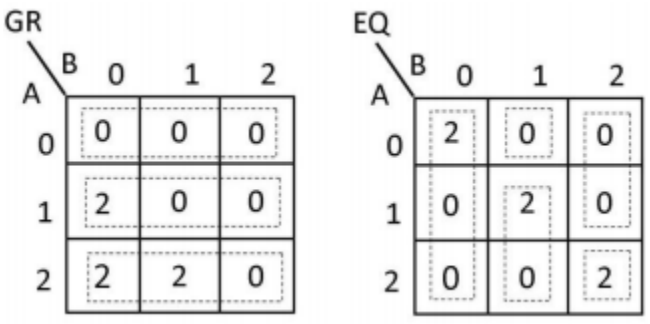


Figure 4.18: K-map for 1-bit comparator

The transistor level implementation of pass transistor based system 1 and system 2 of 1-bit comparator are appeared in Figure 4.19. These networks are acknowledged in view of eq. (4.10) and (4.11). Since the P-CNTFET and N-CNTFET gadget with same size have same carrier mobility and thusly same current driving capacity, the two devices are used in realization of pass transistor based networks. For all the conceivable mixes of An and B, circuit of 1-bit comparator gives appropriate way that produces wanted output rationale. For occurrence, when A = 0, An is 2 and transistor T1 is ON, which passes 0 to GR. Presently, consider three unique estimations of B. At the point when B = 0, B_n is 2, transistor T5 is ON and passes A (rationale 2) to EQ. For this case, outputs GR and EQ are set to 0 and 2, separately, which indicates break even with

condition. At the point when B = 1, B_p and B_n are 2 and 0 individually. Transistors T6, T8 and T9 are ON and pass 0 to EQ. For this situation, the two outputs GR and EQ are set to 0 which indicates lesser condition. Essentially, when B = 2, Transistors T10 and T12 are ON and pass 0 to EQ. The two outputs GR and EQ stays at 0 to demonstrate lesser condition. Contrasted with the 1-bit comparator, proposed one reduces the quantity of transistor from 32 to 20 (counting inverters).

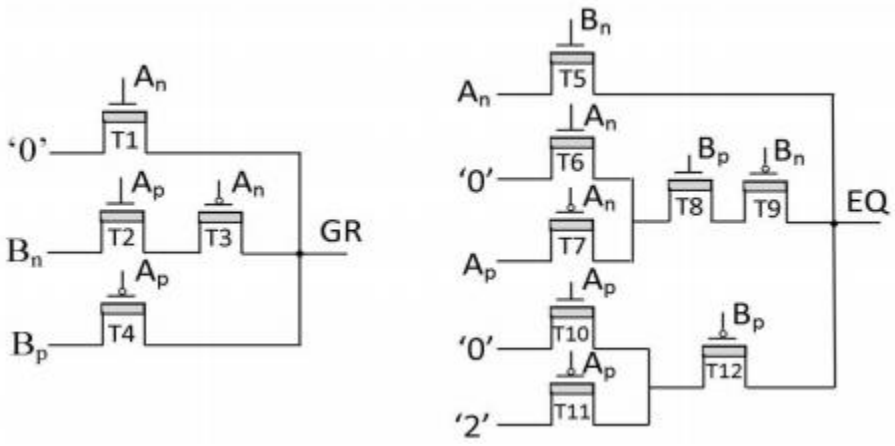


Figure 4.19: Schematic diagram of 1-bit comparator

4.3.2 Design of N-bit Comparator

An N-bit comparator compares two N-bit ternary numbers AN-1….A1A0 and BN-1….B1B0,and produces two outputs GR[N-1 : 0] and EQ[N-1 : 0]. It is designed using proposed 1-bitcomparator blocks and a binary tree network of [206]. 1-bit comparator generates greater andequal signals indicated by GRi and EQi, respectively, for bit position (i) = 0….N-1. Binarytree network contains binary grouping blocks which combine these signals to form groupsignals which are defined as follows

$$GR[2j+1:2j] = GR[2j+1] + EQ[2j+1]GR[2j] \quad \textbf{(4.19)}$$

$$EQ[2j+1:2j] = EQ[2j+1]EQ[2j] \quad \textbf{(4.20)}$$

Where j =0….N/2 - 1. In the tree design, this gathering is done at each phase until last greater and equivalent signs demonstrated by GR $_{[N-1:\ 0]}$ and EQ $_{[N-1:\ 0]}$ are not gotten. Figure 4.20

demonstrates the stick graph and square outline of a 2-bit comparator. The primary stage contains two 1-bit comparator squares which produce GR_i and EQ_i for i = 0, 1. The second organize contains a binary gathering square which produces supplements of GR $_{[1: 0],}$ and EQ $_{[1: 0]}$. To get GR $_{[1: 0]}$ and EQ $_{[1: 0],}$ two binary inverters are utilized at the yields. Further, to appear the usage of N-bit outline, a case of 4-bit comparator is considered.

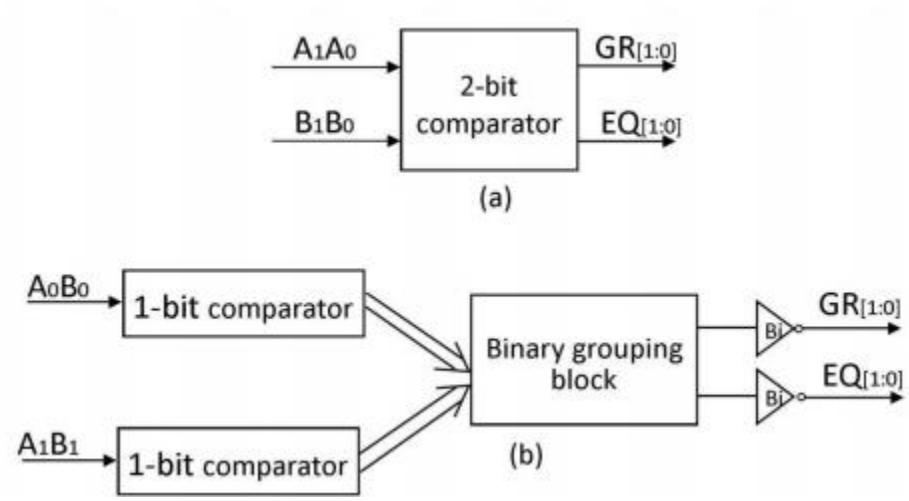


Figure 4.20: 2-bit comparator (a) pin diagram (b) block diagram

Figure 4.21 demonstrates the pin outline and square chart of a 4-bit comparator. The principal organize contains four 1-bit comparator blocks which produce GR_i and EQ_i for i = 0. . . 3. The second organize contains two binary grouping blocks which produce GR $_{[1: 0],}$ EQ $_{[1: 0],}$ GR $_{[3: 2]}$ and EQ $_{[3: 2].}$ The third stage contains one transformed binary grouping square which creates last yields GR [3: 0] and EQ [3: 0].

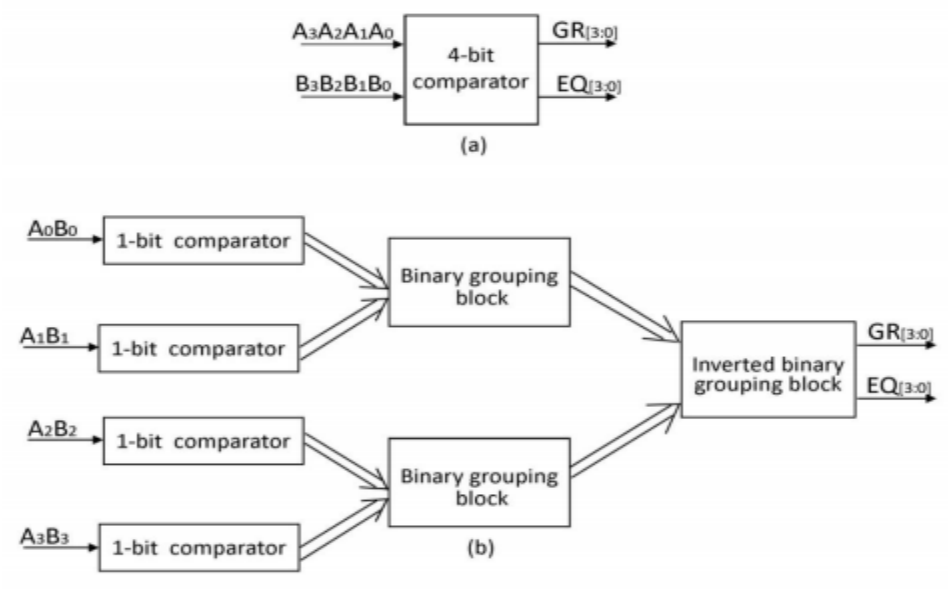


Figure 4.21: 4-bit comparator (a) pin diagram (b) block diagram

The schematic graph of both binary grouping square and its rearranged variant are appeared in Figure 4.22. They are executed in light of correlative CNTFET rationale style. Despite the fact that 1-bit comparator hardware produces debased rationale levels at its yields because of edge voltage drop crosswise over N-CNTFET and P-CNTFET devices, plan of binary grouping piece gives level reclamation and as a result, full rationale levels are acquired at the last yields of N-bit plan. Contrasted with the N-bit comparator proposed one decrease the quantity of stages in the basic way by taking neither out a slower NOR gate and in this manner, it leads to a rapid plan.

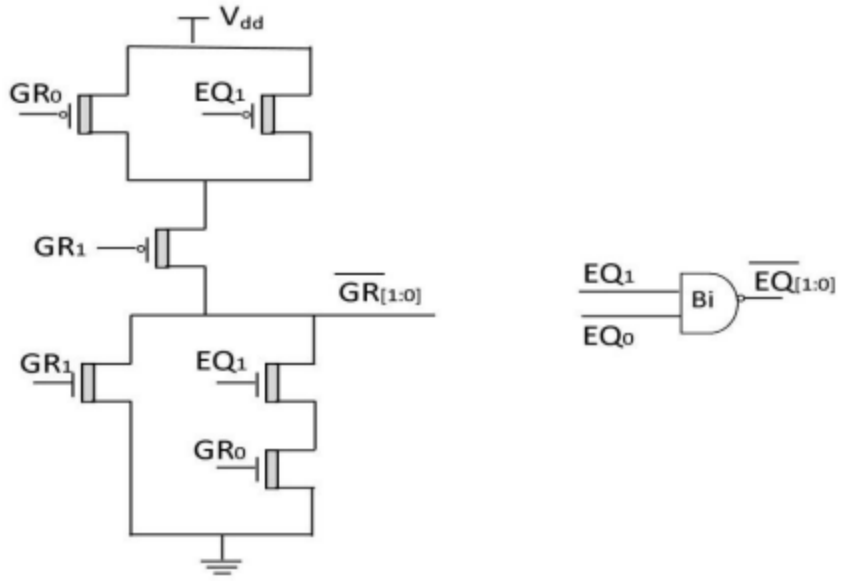


Figure 4.22(a): Schematic diagram of binary grouping block

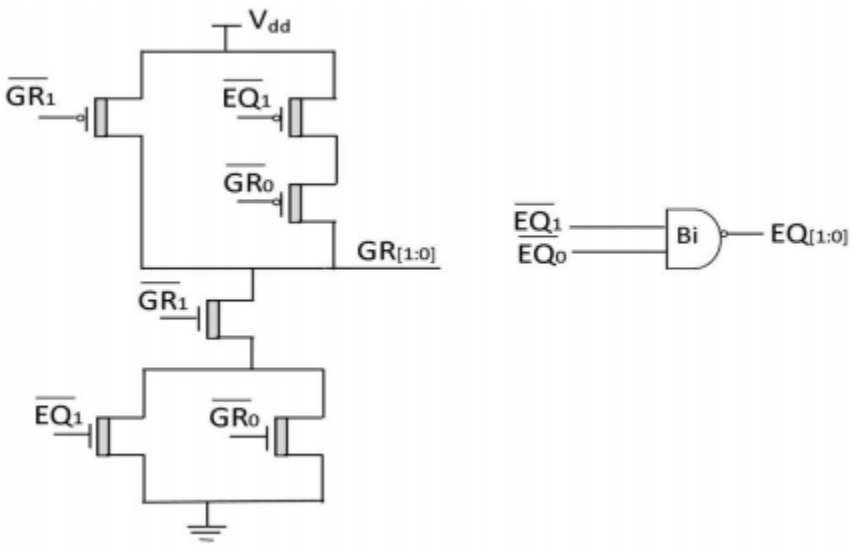


Figure 4.22(b): Schematic diagram of inverted binary grouping block

4.3.3 Results and Discussion

In this area, the proposed 2-bit comparator is analyzed and simulated utilizing Synopsis HSPICE simulator with 32nm Stanford CNTFET show under different conditions. The chirality vector of all CNTFETs utilized as a part of comparator circuit is (19, 0).The limit voltage of these

transistors is 0.289V with the distance across of 1.487 nm. Other innovation parameters of CNTFETs have same esteems as specified in segment 2.2 of part 2. For examination of proposed comparator plan, CNTFET-based comparators repeated. Furthermore, 2-bit comparator is executed utilizing CNTFET-based ternary gates as these rationale gates beat other existing CNTFET-based gates, and alluded as CNTFET-based comparator for examination. For recreated outlines, chirality vector of CNTFETs and estimation of other gadget parameters are picked by the data given in the individual papers from the writing. Here, ternary outline of section 3 which was distributed is eluded as plan.

Simulation Setup

Transient recreation is performed at room temperature, at 250MHz operational recurrence also, at 0.9V supply voltage. Also, stack capacitor of 2.1fF is utilized at all yield hubs of the circuit for the reenactment. The normal power utilization is measured over a long stretch of time. For most pessimistic scenario postpone assurance, all conceivable yield move delays are measured. The deferral is measured at the half purpose of the rising edge of info information to the half purpose of the rising edge of the comparator yield. By virtue of the exchange off between control utilization and postponement, PDP is registered by the duplication of the normal power and more terrible case delay.

Evaluation of Proposed 2-bit Comparator

Figure 4.23 demonstrates the example transient waveform of 2-bit comparator. The initial four waveforms speak to inputs A0, A1, B0 and B1, and the last two waveforms demonstrate yields GR and EQ which affirms its right operation. An examination on delay, control utilization, PDP and gadget number of CNTFET-based 2-bit comparator outlines is appeared in Table 4.7. It can be seen from the reenactment comes about that proposed configuration accomplishes 16% less postponement, 14% less power and 29% less PDP with 34% less gadget number in correlation with that of comparator. Contrasted with comparator proposed one accomplishes decrease in delay, power, PDP and gadget check by 14%, 33%, 48% and 43%, separately. In correlation with comparator. Comparator gets points of interest in delay, power, PDP and gadget number by 49%, 57%, 91% and 79%, separately. Further, recreation comes about are likewise gotten with various

reproduction set-up in which 500 MHz working recurrence, 2 fF yield load and 20 nS transient time are set. These outcomes are exhibited

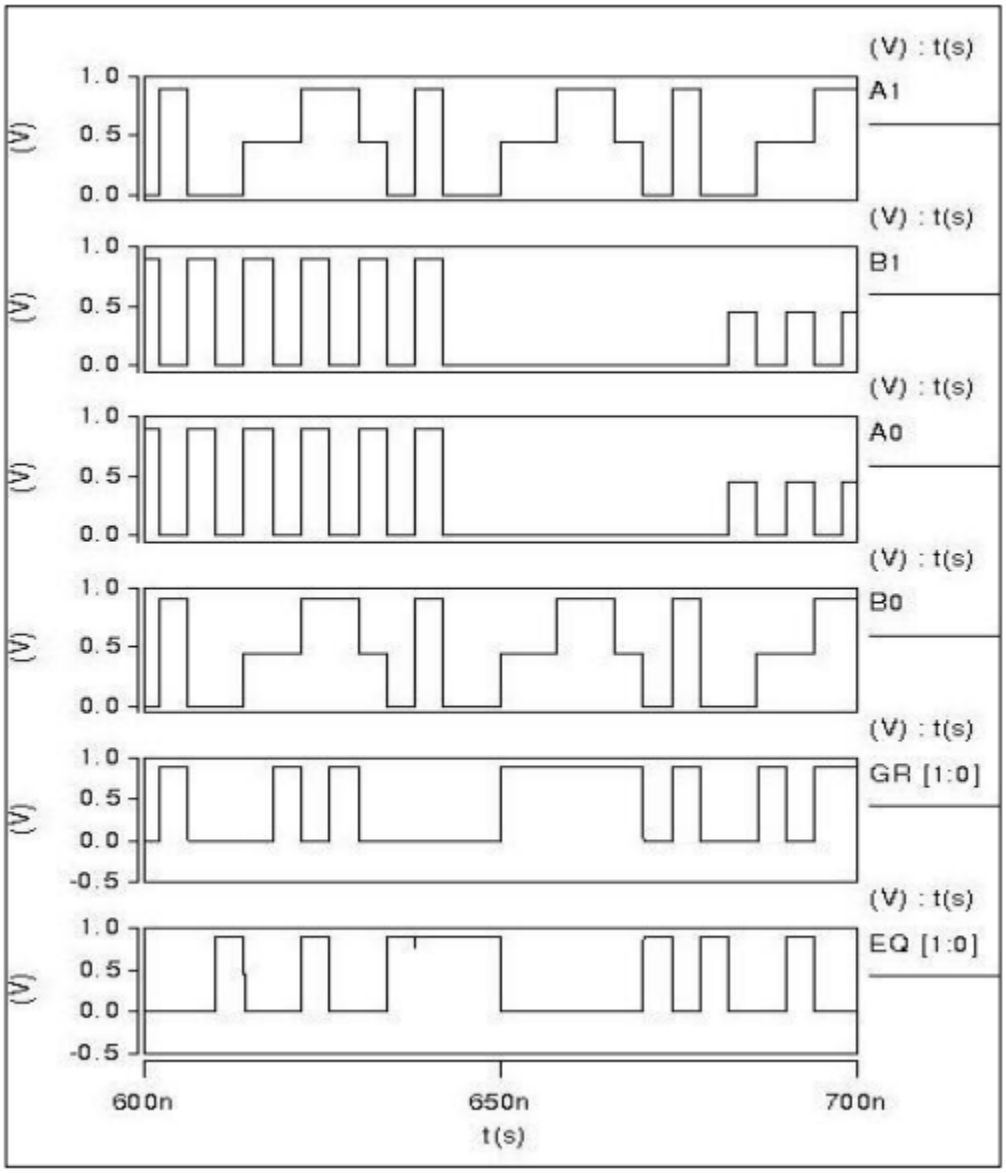


Figure 4.23: Transient waveform of 2-bit comparator

Table 4.7: Simulation results of 2-bit comparator circuits

Circuits	Delay ($\times 10^{-10}$ S)	Power ($\times 10^{-6}$ W)	PDP ($\times 10^{-16}$ J)	Device Count
Proposed comparator	0.41	0.42	0.17	54
Comparator of [206]	0.49	0.49	0.24	82
Comparator of [252]	0.48	0.63	0.30	104
Comparator of [73]	0.81	0.99	0.80	600

To look at driving ability of comparator outlines, they are simulated utilizing different output stack capacitors, ran from 2 fF up to 6 fF, at 250 MHz working recurrence with room temperature and 0.9 V supply voltage. The deferral, control consumption and PDP of 2- bit comparator outlines against stack capacitor variety are plotted in Figure 4.24. Concurring to the plotted outcome, deferral and energy of proposed 2-bit comparator are lower than that of different outlines for all output load capacitors. What's more, the superiority of proposed 2-bit comparator turns out to be more significant by expanding the heap capacitance, which demonstrates its high driving ability.

To assess the execution of comparator outlines at various frequencies, recreations are led at working recurrence extending from 100 MHz to 1000 MHz with 0.9 power supply, room temperature and 2.1fF output stack. Figure 4.25 plots control consumption of 2- bit comparator plans as opposed to working recurrence. Recreation comes about demonstrate that proposed 2-bit comparator works dependably and consumes less power in correlation with different plans at all frequenciesV to 1.1 V. For this, reenactments are performed at room temperature with 250 MHz recurrence and 2.1 fF output stack. PDP of 2-bit comparator processed from this reenactment are plotted in Figure 4.26. It can be surmised from comes about that the proposed 2-bit configuration is strong to voltage variations, and has low PDP at all supply voltages, in

examination with different outlines. Further, to inspect the affectability of the comparator outlines to temperature variations, reenactments are directed at various temperatures changing from 0◦C to 100◦C. Other test parameters are 0.9 V supply voltage, 250 MHz recurrence and 2.1 fF output stacks. PDP of 2- bit comparator with temperature variety is plotted in Figure 4.27. The plotted outcome demonstrates less vulnerability of proposed 2-bit comparator configuration to temperature variations as for different outlines. Reenactment has likewise been performed to survey process variations at two extreme corners where the CNT measurement of all transistors utilized as a part of the outline is taken as a ±10% variety from the first esteem. Execution parameters counting delay, control utilization and PDP, separated from these reproductions are appeared in Table 3 of Appendix II. As per the announced outcomes, the proposed comparator prompts a productive plan in correlation with other existing counterparts.

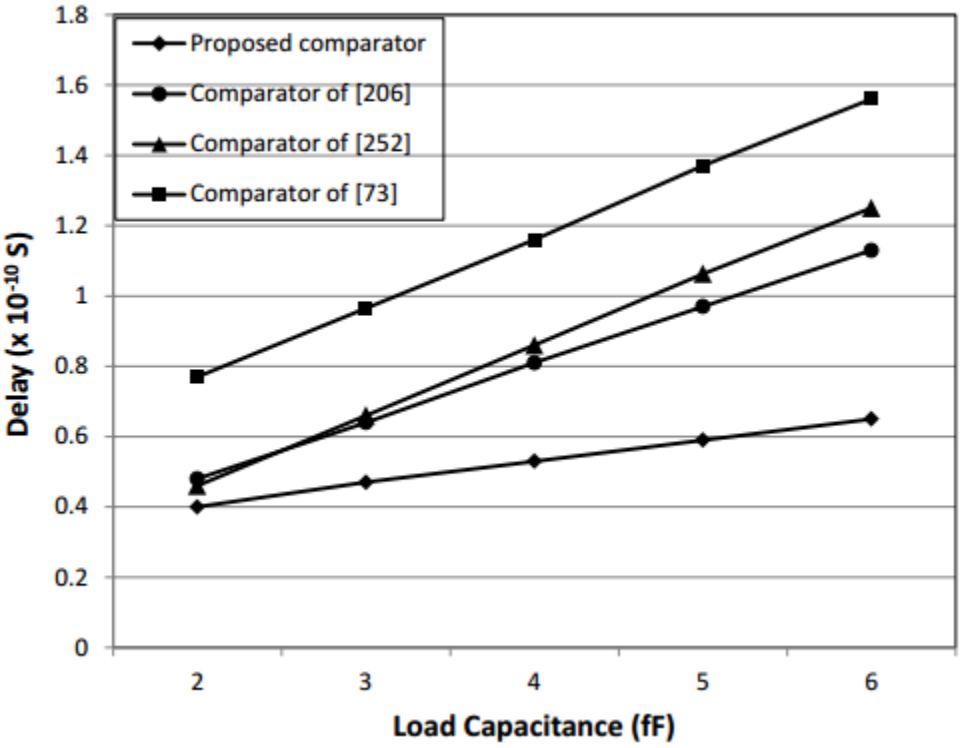


Figure 4.24 (a): Delay versus output load capacitor plot for 2-bit comparator circuits

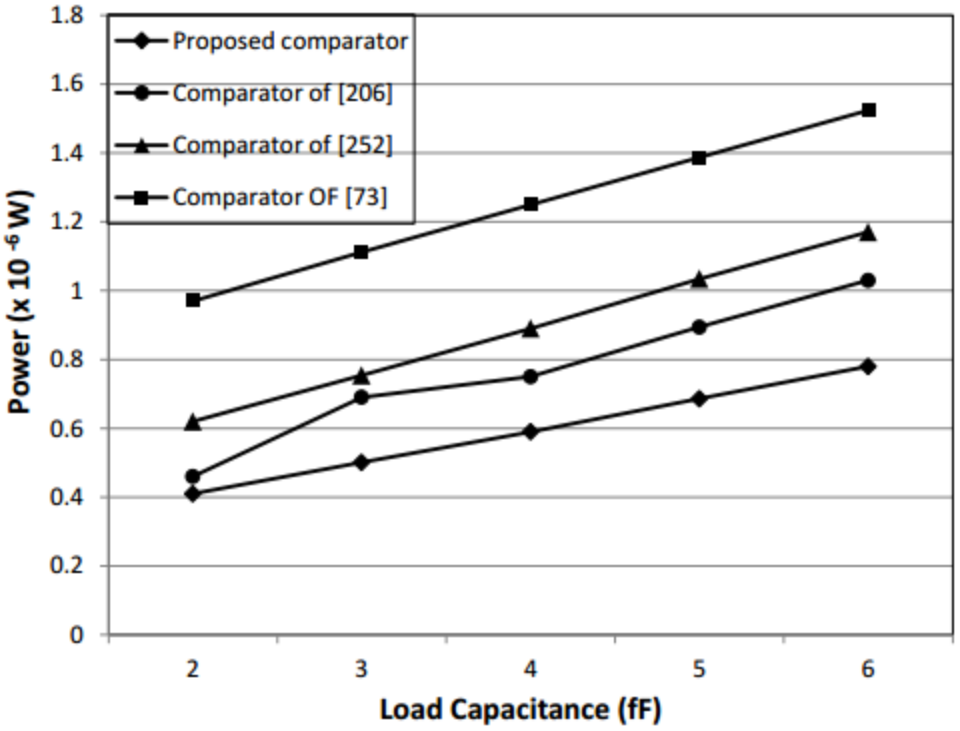


Figure 4.24 (b): Power consumption versus output load capacitor plot for 2-bit comparator circuits

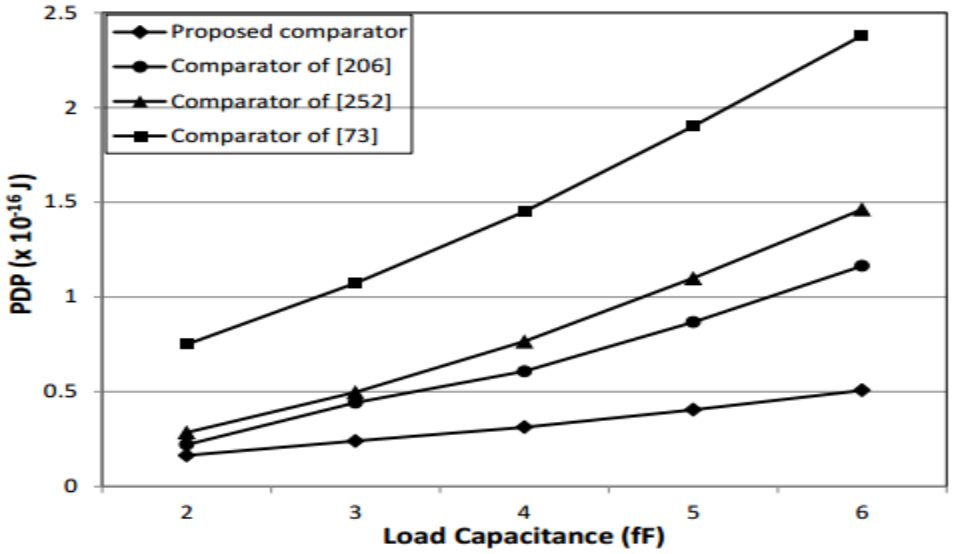


Figure 4.24 (c): Power-delay product (PDP) versus output load capacitor plot for 2-bit comparator circuits

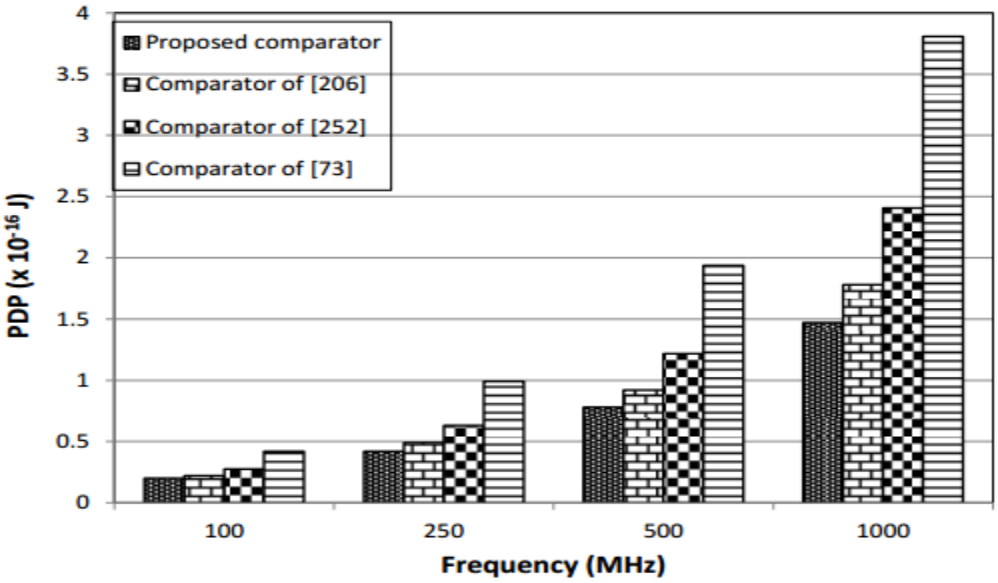


Figure 4.25: Power consumption versus operating frequency plot for 2-bit comparator circuits

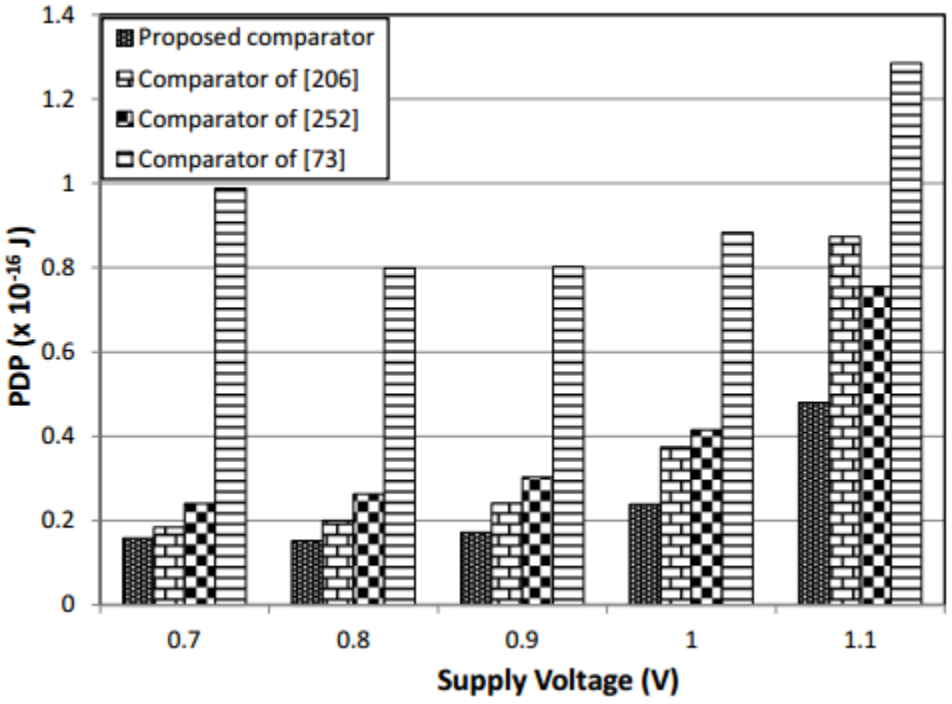


Figure 4.26: Power-delay product (PDP) versus supply voltage plot for 2-bit comparator circuits

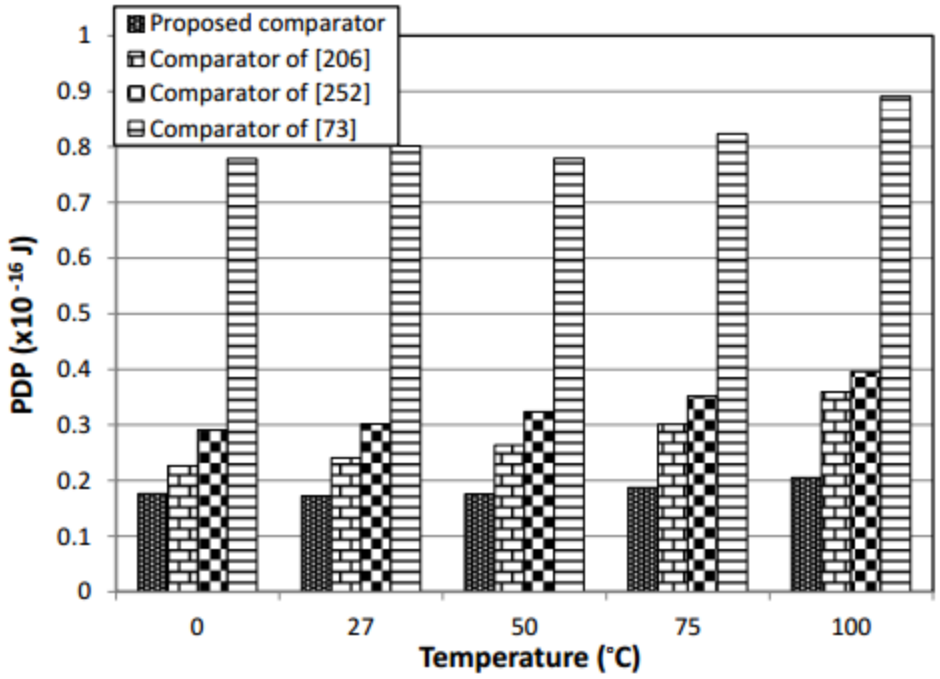


Figure 4.27: Power-delay product (PDP) versus temperature plot for 2-bit comparator circuits

4.4 Conclusion

This part has exhibited three novel plans of CNTFET-based TFA which is an essential subblock of AS useful module of 2-bit HO-TALU, utilizing diverse circuit methods. The to begin with TFA named as HS-TFA contains a symmetric draw up and pull-down systems along with a resistive voltage divider as its integral part, which is arranged utilizing transistors. Contrasted with most vitality productive TFA accessible in literature, HS-TFA has high driving capacity and gets decrease in delay by 9% however it demonstrates high power dissipation. The second TFA named as LP-TFA has been created utilizing complimentary pass transistor logic style. This LP-TFA indicates decrease in control by 24% with change in PDP by 5%, yet it has 20% more postponement. The third TFA named as dynamic TFA (DTFA) has been actualized based on dynamic logic, which utilizes a ternary manager to remunerate charge misfortune because of charge sharing issue. DTFA has high driving ability and accomplishes decrease in power, deferral and PDP by 24%, 15% and 35%, individually. Be that as it may, it needs CNTFET devices with littler distance across (0.626 nm) furthermore so as to decrease charge spillage. Each of the three TFAs have been composed based on characteristic binary nature (0 and 1) of information convey, which prompts decreased gadget tally in outlines.

Further, new outline of 1-bit comparator has been created utilizing pass transistor logic with lessened number of stages in basic defer way. This outline has been utilized to make 2-bit and N-bit comparator where a static binary tree setup has been used to rectify the voltage levels. The proposed 2-bit comparator has high driving capacity and accomplishes 29% lessening in PDP with 34% less gadget number contrasted with that of its partner accessible in literature. Be that as it may, it has two output signs to check greater, lesser and level with conditions, which make the translating logic of comparator reaction complex in those applications where three outputs (one for each condition) are coveted. Aside from these, all new TFAs and 2-bit comparator demonstrate less susceptibility to voltage and temperature variations concerning existing outlines.

In the following part, outline of 2-bit control upgraded ternary ALU (PO-TALU) utilizing CNTFETs is introduced. 2-bit PO-TALU makes utilization of new reciprocal CNTFET-based configuration style and a low unpredictability encoder in usage of ternary capacities to accomplish low power consumption. What's more, it consolidates snake subtractor-select OR module which prompts smaller TALU structure.

Chapter 5

Design of 2-bit Power Optimized Ternary ALU (PO-TALU) using CNTFETs

5.1 Introduction

Minimizing region, postponement and cost have dependably been principle requirements for VLSI creators, however as of late, diminishing the power consumption has likewise gotten impressive attention due to expanding estimations of integration thickness, and the need of portable and dependable circuits. There is a colossal enthusiasm towards minimal and portable applications, for example, note pad and smart phones, require high throughput and enormously expanded capacity. Consequently, low power consumption has turned out to be one of the essential imperatives in outlining of present day processor. Further, an ALU is a critical piece of a digital computer where it plays out all arithmetic and logical operations. Current CPU and illustrations preparing unit require powerful ALU. This section introduces an outline of 2-bit control upgraded ternary ALU (PO-TALU) utilizing CNTFETs. 2-bit PO-TALU practical modules: viper subtractor-elite OR (ASE) and multiplier, are planned utilizing new corresponding CNTFET-based binary computational unit and a low multifaceted nature encoder (in correlation with earlier plan of [213] and [252]). ASE wipes out selective OR and subtractor modules from the regular architecture. Multiplier utilizes a new productive convey include (CA) hinder set up of ternary half snake. Thus, PO-TALU configuration gets huge changes as far as power and power-defer item (PDP) with gadget number contrasted with existing outlines. Plan of 2-bit PO-TALU cut is demonstrated so that parallel N-bit PO-TALU can be developed with N/2 cuts associated in course. Whatever remains of the section will be sorted out as takes after. In segment 5.2, architecture and capacities of PO-TALU is exhibited. Area 5.3 demonstrates minimization and acknowledgment of POTALU ternary capacities. In segment 5.4, outline and execution of PO-TALU utilitarian modules are depicted. Area 5.5 presents the expansion of PO-TALU for 2-bit PO-TALU cut. Area 5.6 gives reproduction results and examination with existing CNTFET-based plans, trailed by the conclusion in segment 5.7.

5.2 Architecture and Functions of 2-bit PO-TALU

Figure 5.1 demonstrates the pin chart and architecture of proposed 2-bit PO-TALU. The ternary information contributions from An (A_1 A_0) are consolidated with the ternary information

contributions from B (B_1 B_0) and operations are performed to create one of the accompanying outputs: Sum/Diff/XOR and Convey/Borrow, PROD, GR and EQ, "A.B" and 'A+B'. Two select information sources (S_1 and S_0) are utilized to select one craved operation, as portrayed in Table 5.1. PO-TALU performs six arithmetic and three logic operations. The arithmetic operations incorporate option (ADD), subtraction (SUB), increase by logic 1 (INC), decrement by logic 1 (DEC), duplication (MUL) and correlation (COMP). The logic capacities incorporate AND, selective OR (XOR) or potentially.

Contrasted with TALU architecture, the proposed one wipes out selective OR module, and performs two more arithmetic capacities: INR and DEC, without including any additional utilitarian module. In addition, the required logic 1 for INC and DEC operations is created by utilizing two continually exchanged on transistors T1 and T2. T1 (P-CNTFET) and T_2 (N-CNTFET) with same geometry and equivalent limit voltage bring a similar resistance because of the equivalent mobility of N and P substances. As an outcome, they can be used to perform voltage division for era of $Vd_d/2$ (i.e. voltage level of logic 1). Thus, POTALU does not require an additional power supply for $V_{dd}/2$. Term "Bi" is utilized to elude binary logic gates in ternary framework.

PO-TALU configuration is made out of the accompanying fundamental segments: 1-to-6-line ternary decoder, work select logic hinder with dynamic low outputs (FSB-ALO), transmission gate hinder with dynamic low empower (TGB-ALE) and separate utilitarian modules like ASE, multiplier and comparator and so on.

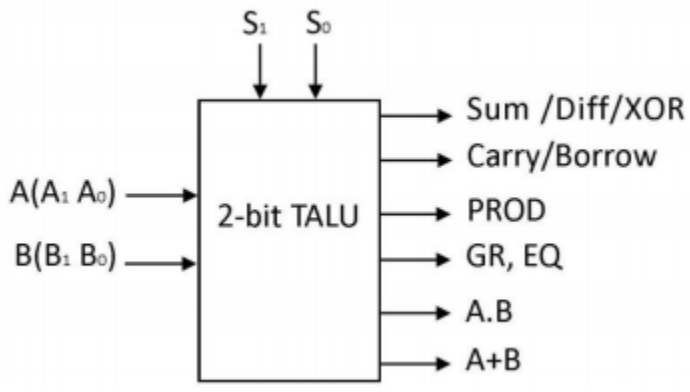


Figure 5.1 (a): Pin diagram of 2-bit PO-TALU

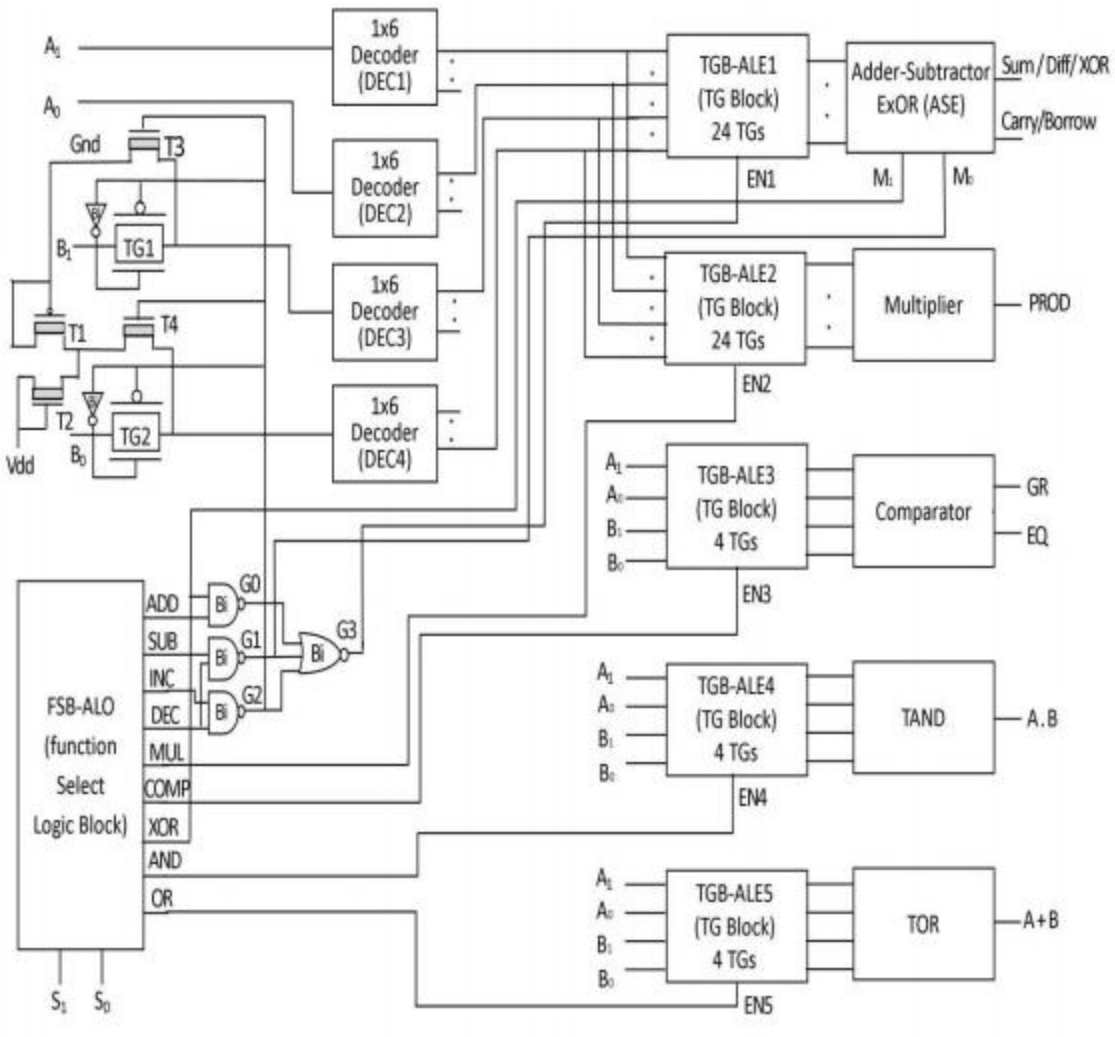


Figure 5.1 (b): Architecture of 2-bit PO-TALU

Table 5.1: Function table of 2-bit PO-TALU

Selection Lines		Function
S_1	S_0	
0	0	ADD
0	1	SUB
0	2	INC
1	0	DEC
1	1	MUL
1	2	COMP
2	0	XOR
2	1	AND
2	2	OR

1-to-6-line Ternary Decoder A 1-to-6-line ternary decoder introduced in section 4 (Figure 4.2) is utilized here and appeared in Figure 5.2. It contains one negative ternary inverter (NTI), one positive ternary inverter (PTI) and three binary inverter and one binary NOR gate for the era of unary capacities. As appeared in Figure 5.1(b), DEC1 (1-to-6-line decoder) creates unary capacities $A^0_0, A^1_0, A^2_0, \bar{}A^0_0, \bar{}A^1_0$, and $\bar{}A^2_0$ for A_0DEC2 generates $A^0_1, A^1_1, A^2_1, \bar{}A^0_1, \bar{}A^1_1$ and $\bar{}A^2_1$Similarly, DEC3 generates $B^0_0, B^1_0, B^2_0, \bar{}B^0_0, \bar{}B^1_0$ and $\bar{}B^2_0$ for B_0, These unary functions are fed to different functional modules for desired outputs.

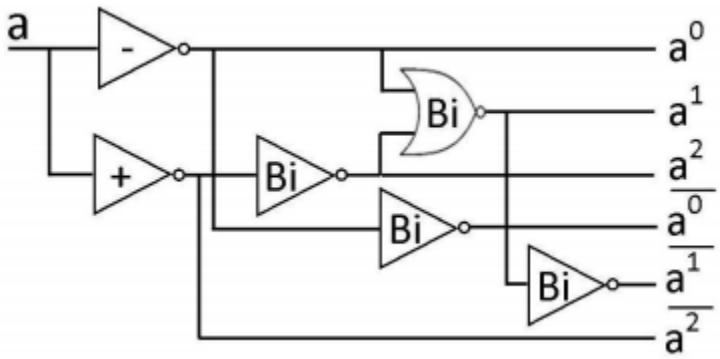


Figure 5.2: Logic level diagram of 1-to-6-line ternary decoder

Capacity Select Logic Block with Active Low Outputs (FSB-ALO) the logic level outline of capacity select logic block with dynamic low outputs (FSB-ALO) is appeared in Figure 5.3. FSB-ALO has two select sources of info S_0 and S_1, and nine dynamic low outputs Include, SUB, INR, DEC, MUL, COMP, XOR, and OR. It involves binary NAND gates what's more, two 1-to-

3-line decoders (DEC1 and DEC2). Here, decoder outline is utilized since just unary capacities are required for S1 and S0. DEC1 produces signals S^0_0, S^1_0 and S^2_0 for S_0. So also, DEC2 produces signals S^0_1, S^1_1 and S^2_1 for S_1. These signals are connected to NAND gates for coveted outputs. FSB-ALO chooses one specific TALU operation depending on the bit blend of S_0 and S_1, as portrayed in Table 5.1. Consider the situation when S_1S_0 = 12. S^0_1, S^1_1 what's more, S^2_1 are 0, 2 and 0, separately. Thus, S^0_0, S^1_0 what's more, S^2_0 are 2, 0 and 0, separately. In the variety of NAND gates, sixth NAND gate makes its output COMP equivalent to logic 0 on the grounds that both of its data sources (S^1_1 what's more, S^2_0) are equivalent to logic 2. While all other NAND 115 gates have (at least one) input equivalent to logic 0, which makes their outputs equivalent to logic 2. The dynamic low "COMP" additionally empowers TGB-ALE3 to pass include information for examination operation, as appeared in Figure 5.1(b). Accordingly, for every conceivable mix of S_0 and S_1, there is just a single specific output which is dynamic low for individual TALU work.

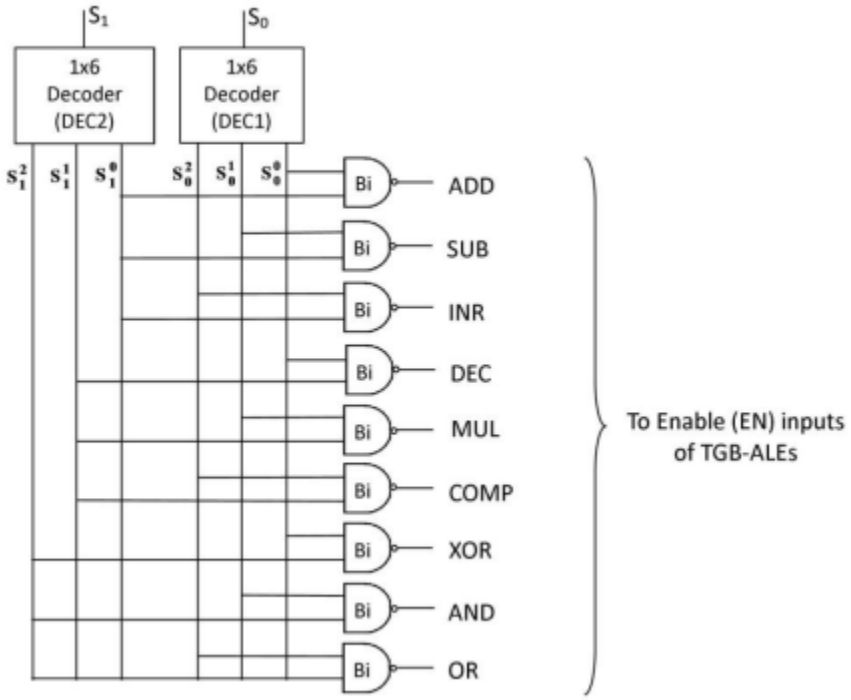


Figure 5.3: Logic level diagram of function select logic block with active low outputs (FSBALO)

Transmission Gate Block with Active Low Enable (TGB-ALE) Figure 5.4 shows logic level outline of transmission gate block with dynamic low empowers (TGBALE). A TGB-ALE contains a variety of transmission gates (TGs), which interface decoder output lines created for input A and B, to the information contributions of useful block. This exhibit is activated when input empower (EN) is low. In Figure 5.1(b), the quantity of TGs utilized as a part of the cluster is specified with every individual TGB-ALE. A TG is actualized utilizing the parallel association of P-CNTFET and N-CNTFET. In a TG exhibit, the gate of P-CNTFET of all TGs is associated with EN and the gate of all N-CNTFETs is associated with EN which is produced by utilizing a binary inverter. At the point when EN is equivalent to logic 0, the P-CNTFET gate is at ground furthermore, the N-CNTFET gate is at V_{dd}, along these lines, the two transistors conduct and there is a shut way between input (I/P) and output (O/P) of TG. At the point when EN is equivalent to logic 2, the P- 116 CNTFET gate is at Vd_d and the N-CNTFET gate is at ground, the two transistors are OFF and there is an open circuit between I/P and O/P of TG. In this manner, the dynamic low estimation of EN empowers TGB-ALE. TGB-ALE gets estimation of EN from at least one outputs of FSB-ALO through either some logic or specifically, as appeared in Figure 5.1(b). FSB-ALO outputs MUL, COMP, What's more, and OR are associated straightforwardly to EN2 of TGB-ALE2, EN3 of TGB-ALE3, EN4 of TGBALE4 what's more, EN5 of TGB-ALE5, separately. Since TGB-ALE1 is related with the ASE useful module which performs five operations ADD, SUB, INC, DEC and XOR, its empower input EN1 must be dynamic low at whatever point one of these operations is fancied. For this, a little logic neither circuit containing three binary NAND gates and one binary NOR gate is included with FSB-ALO. FSB-ALO outputs ADD and XOR are connected to the main NAND gate G0, SUB and DEC are connected to the second NAND gate G1 and, INC and DEC are associated with third NAND gate G2. The outputs of gate G0, G1 and G2 are then passed to a NOR gate G3 which creates EN1 of TGB-ALE1. Once the dynamic low estimation of EN empowered a TGB-ALE, ternary information esteems are exchanged to the individual useful module and fancied operation is performed. Further, INC and DEC elements of the PO-TALU are communicated as "A+1" and 'A-1' individually. These operations are executed by ASE module which performs "A+B" and 'Stomach muscle'; accordingly, B (B_1B_0) ought to be set to logic 1. To set B1B0 as 01, two N-CNTFETs T3 and T4 with two TGs: TG1 and TG2 are utilized. As appeared in Figure 5.1(b), the gate of T3, T4 and TG transistors are associated with the output of gate G2. At whatever point FSB-ALO output INC (or DEC) is made dynamic low, output of gate G2 is set to logic 2, T3 and

T4 are activated while TG1 and TG2 are crippled, which pass logic 0 (ground) and logic 1 (i.e. $V_{dd}/2$ created by T1 and T2) set up of B1 and B0, individually, to the decoders. Along these lines, logic 1 is passed to the ASE module to perform augmentation and decrement by logic 1. At the point when output of gate G2 is set to logic 0, T3 and T4 are OFF and, TG1 and TG2 are activated which pass B1 and B0 to the decoders with the goal that coveted operation can be performed on input information A (A_1A_0) and B (B_1B_0).

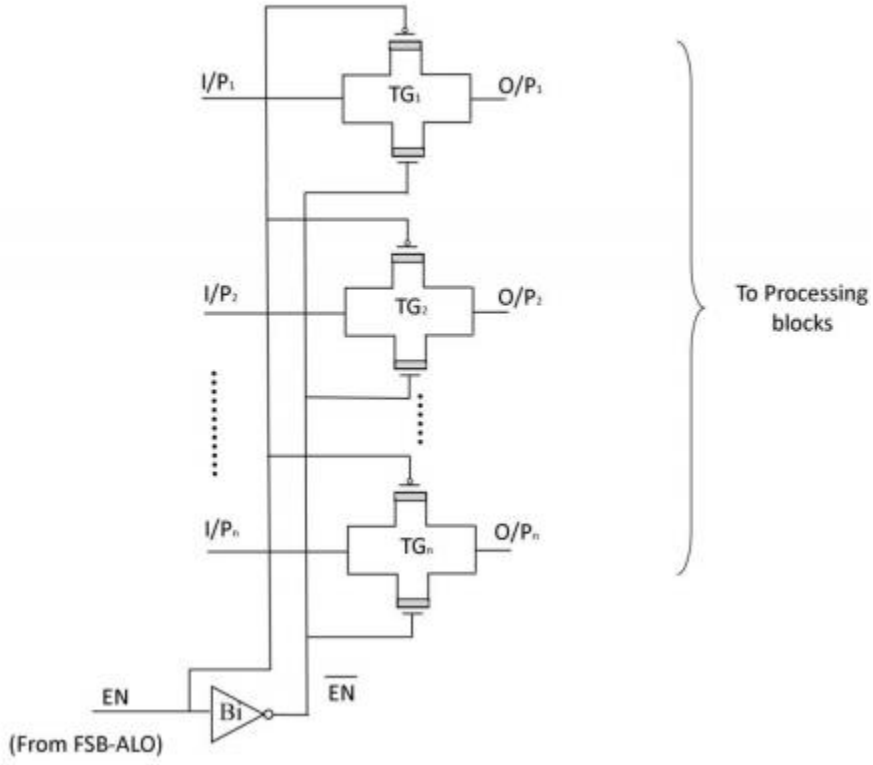


Figure 5.4: Logic level diagram of transmission gate block with active low enable (TGB-ALE)

5.3 Minimization and Realization of 2-bit PO-TALU Functions

2-bit PO-TALU utilizes ternary K-delineate for ternary capacity minimization. The detail of this K-outline is given in section 3. Further, a conventional technique for acknowledgment of ternary

capacity utilizes a ternary to binary decoder; a binary computation unit and an encoder for converting binary yields back to ternary yields. It is watched that encoder and computation circuit can be enhanced (when contrasted with ternary plans. Figure 5.5 demonstrates the square chart of ternary capacity usage for PO-TALU. Keeping in mind the end goal to accomplish low power plan, its useful modules: ASE and multiplier are planned utilizing corresponding CNTFET-based binary computation unit and pass transistor-based encoder circuit. Plan of encoder is portrayed underneath.

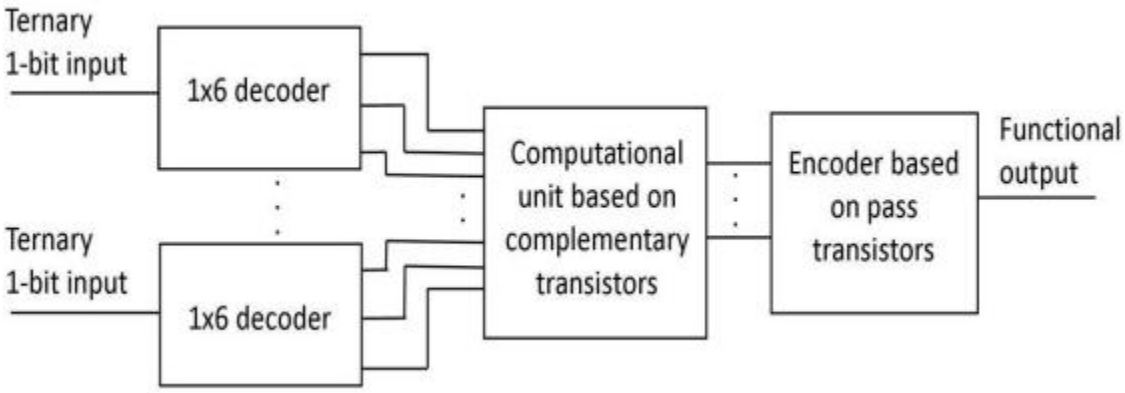


Figure 5.5: Ternary function implementation for 2-bit PO-TALU

Design of Ternary Encoder

Figure 5.6 demonstrates the design of ternary encoder and its image. This design contains two transistors T1 and T2, which have indistinguishable parameters and works as a resistive voltage divider. As a result, yield hub "Out" can be communicated as:

$$\text{Out} = \frac{X_1 + X_2}{2} \quad \textbf{(5.1)}$$

Here, X_1 and X_2 are encoder inputs having binary nature (0 and 2). Reality table of encoder is appeared in Table 5.2. As indicated by (1), out is the normal estimation of X1 and X2. On the off chance that X_1 furthermore, X_2 progresses toward becoming 0, out will likewise be equivalent to 0. In a similar way, if X_1 and X_2 moves toward becoming 2, Y will likewise be 2. Finally, if X_1 and X_2 progresses toward becoming 0 and 2, individually, Y will be equivalent to 1. Comparable scenario will happen if X_1 and X_2 moves toward becoming 2 and 0, separately. Further, the

proposed encoder design utilizes pass transistor rationale and takes out an immediate way from V_{dd} to ground which brings about less power dissipation contrasted with that of encoder design displayed. Along these lines, the proposed encoder prompts low power designs of TALU practical modules (as appeared in area 5.6.2).

Table 5.2: Truth table of ternary encoder

X_1	X_2	Out
0	0	0
0	2	1
2	2	2

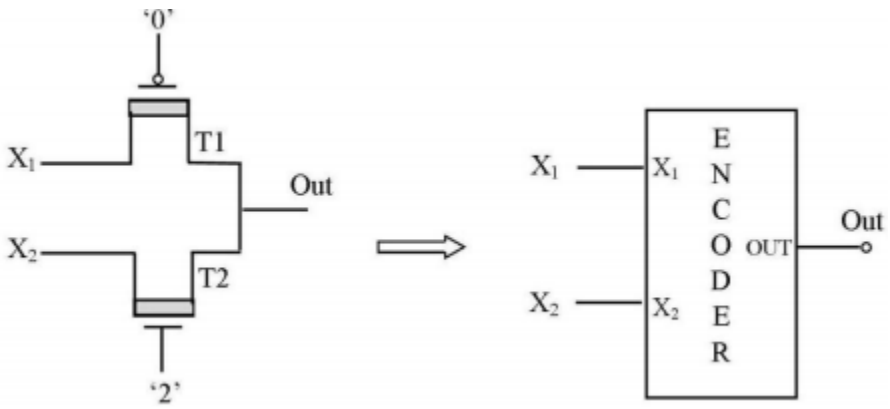


Figure 5.6: Design of ternary encoder

5.4 Design and Implementation of 2-bit PO-TALU Functional Module

5.4.1 Adder-Subtractor-Exclusive-OR (ASE) Module

The proposed ASE module contrasts from the viper subtractor (AS) module in such a way that it performs XOR operation likewise alongside expansion and subtraction operations utilizing one basic viper structure, by using the idea of Modulo-3 expansion of ternary numbers. Figure 5.7 demonstrates the square diagram of the proposed ASE module where operations are performed on A_1A_0 and B_1B_0. Yields $S_0/D_0/E_0$ and $S_1/D_1/E_1$ speak to minimum critical piece (LSB) and most noteworthy piece (MSB) of Sum/Difference/XOR yield of POTALU, what's more, yield

C_1/B_1 speaks to the Carry/Borrow yield of PO-TALU. M_0 and M_1 are binary mode inputs utilized for operation determination of ASE module, as exhibited in Table5.3.

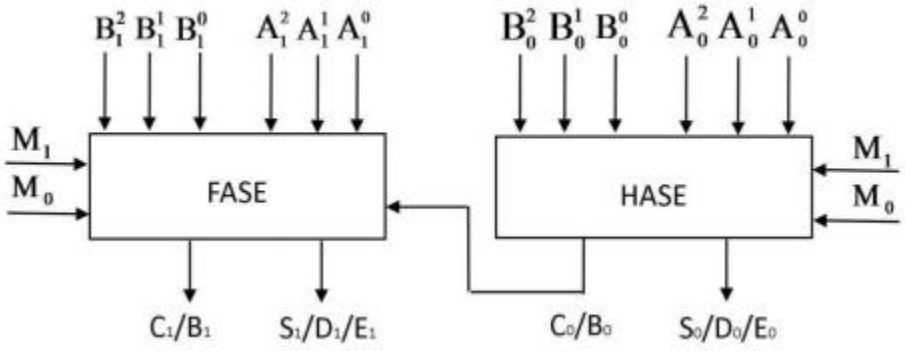


Figure 5.7: Block diagram of adder-subtractor-exclusive-OR (ASE) module

Table 5.3: Function select table for ASE module

M_0	M_1	Operation
0	2	Addition
2	2	Subtraction
0	0	XOR

As appeared in Figure 5.1(b), flag M0 is produced through the binary NAND entryway G1, whose inputs are SUB and DEC, and M1 is straightforwardly connected to the XOR yield of FSB-ALO. For diverse operations, following rationales are fulfilled in view of the rationale conditions of M_0 and M_1.

a) The estimation of M_0 is rationale 2 at whatever point SUB (or DEC) is dynamic low else it is rationale 0.

b) The estimation of M_1 is rationale 0 at whatever point XOR is dynamic low else it is rationale 2.

c) When ADD (or INC) work is chosen, $M_0 = 0$ and $M_1 = 2$ which cause ASE module to perform expansion.

d) For SUB (or DEC) work, both M_0 and M_1 are rationale 2 and ASE module functions as asubtractor.

e) If XOR work is chosen, both M_0 and M_1 are rationale 0 and ASE module performs expansion with zero yield convey.

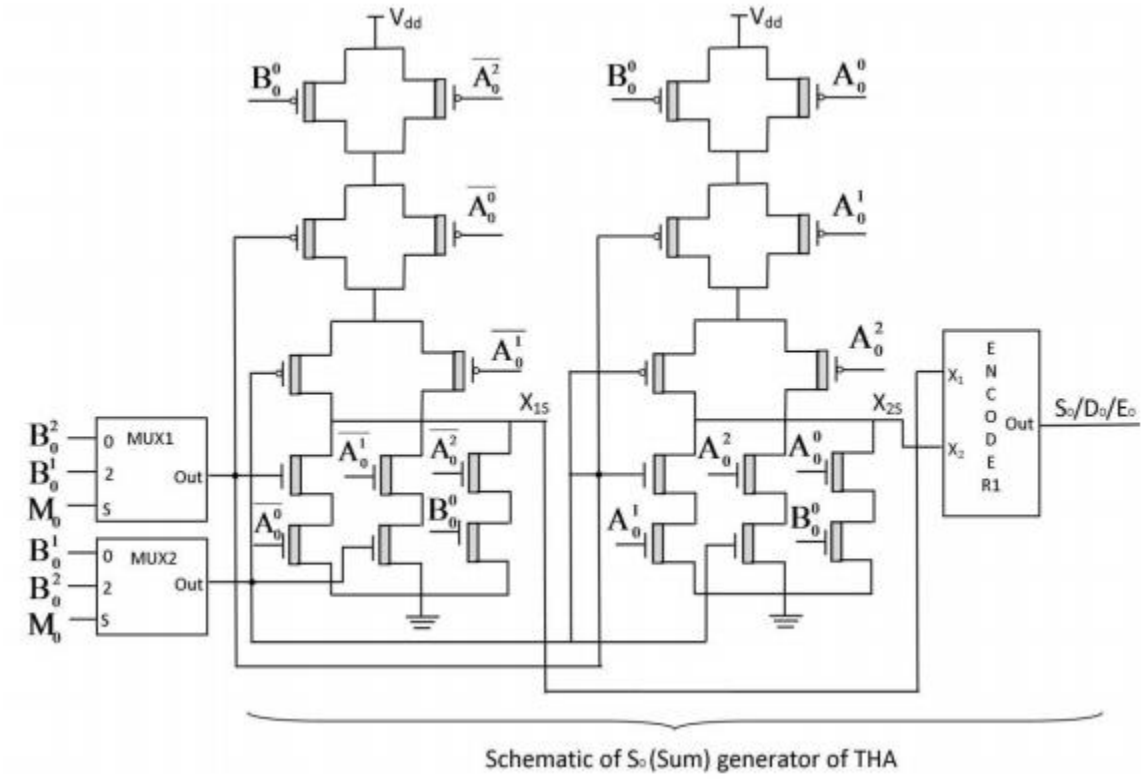
The ASE module contains two sub-pieces: half snake subtractor-selective OR (HASE) and full viper subtractor-select OR (FASE) to execute operations with 2-bit ternary numbers. As appeared in Figure 5.7, HASE performs operations on A_0 and B_0, and creates $S_0/D_0/E_0$ with C_0/B_0. The estimation of C_0/B^0 is exchanged to FASE that includes A_1 and B_1 with C_0/B_0, and produces $S_1/D_1/E_1$ and C_1/B_1. Half Adder-Subtractor-Exclusive-OR (HASE) Block The proposed HASE performs expansion, subtraction and XOR operations utilizing a ternary half snake (THA) circuit just with the assistance of multiplexers and pass transistors. Design of HASE is appeared in Figure 5.8. In view of ternary expansion rules given in Table 5.4 and Table 5.2 (the truth table of encoder), the proposed design finds encoder input factors X_1S and X_2S for Total (S_0) yield and, X_1C and X_2C for Carry (C_0) yield of THA. The estimations of X_1S, X_2S, X_1C and X_2C for various information mixes are additionally incorporated into Table 5.4. The K-maps of X_1S, X_2S, X_1C and X_2C are appeared in Figure 5.9. From the K-maps, the streamlined articulations 121 of these encoder inputs are determined and communicated as takes after

$$X_{1s} = \overline{\overline{A_0^0}\,B_0^2 + \overline{A_0^1}\,B_0^1 + \overline{A_0^2}\,B_0^0} \qquad X_{2s} = \overline{\overline{B_0^2}\,A_0^1 + \overline{A_0^2}\,B_0^1 + \overline{A_0^0}\,B_0^0}$$

$$X_{1C} = 0,\ X_{2C} = \overline{A_0^0 + B_0^0 + A_0^1 B_0^1} \qquad \textbf{(5.2)}$$

Table 5.4: Addition rules for ternary half adder (THA)

A_0	B_0	X_{1S}	X_{2S}	S_0 (Sum)	X_{1C}	X_{2C}	C_0 (Carry)
0	0	0	0	0	0	0	0
0	1	0	2	1	0	0	0
0	2	2	2	2	0	0	0
1	1	2	2	2	0	0	0
1	2	0	0	0	0	2	1
2	2	0	2	1	0	2	1



Schematic of S_0 (Sum) generator of THA

Figure 5.8 (a): Schematic diagram of S0/D0/E0 generator of half adder-subtractor-exclusiveOR (HASE)

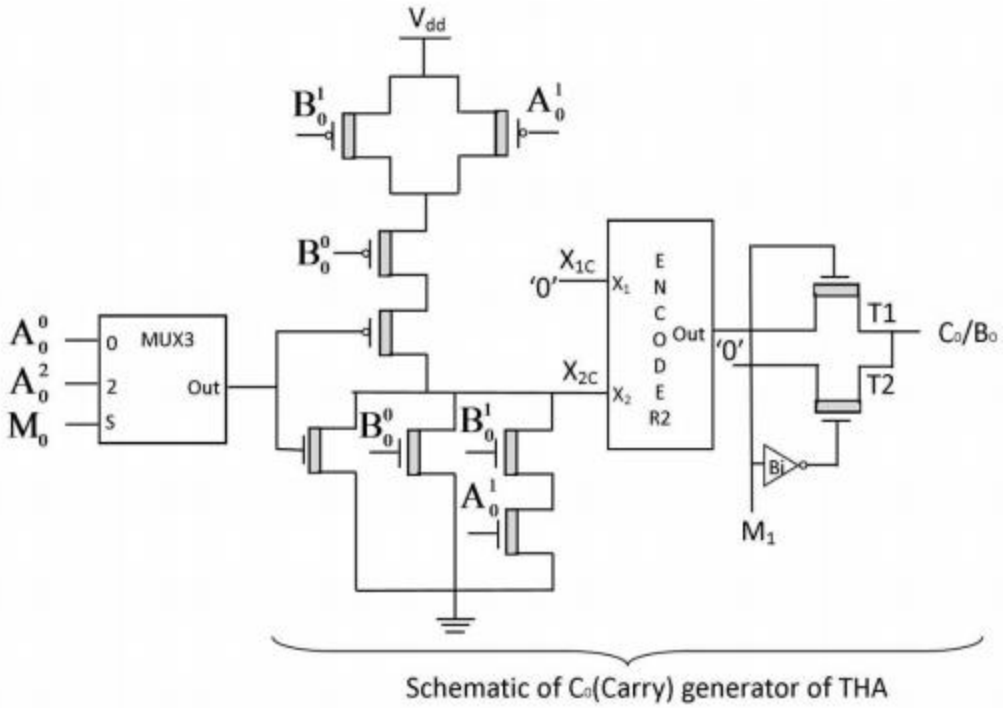


Figure 5.8 (b): Schematic diagram of C0/B0 generator of half adder-subtractor-exclusive-OR (HASE)

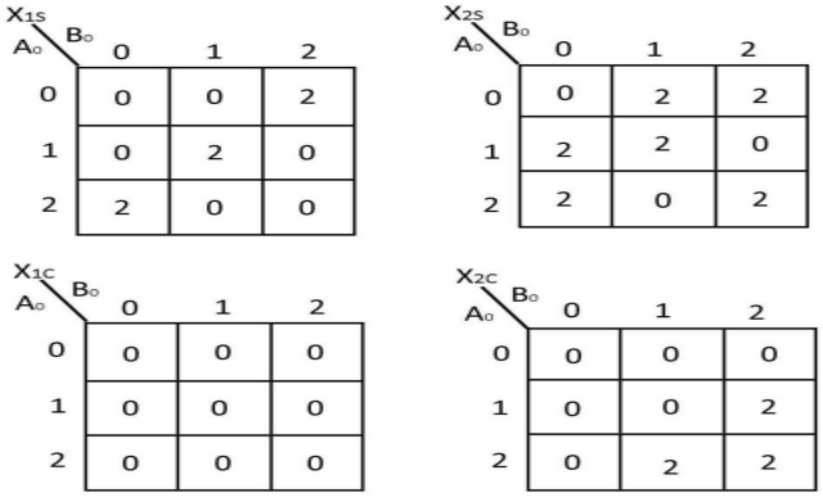


Figure 5.9: K-maps of X1S, X2S, X1C and X2C for ternary half adder (THA)

For the subtraction operation, in light of ternary subtraction rules gave in Table 5.5 and Table 5.2, encoder input factors X_1D and X_2D for Difference (D_0) era and, X_1B and X_2B for Borrow (B_0) era are found. Table 5.5 likewise incorporates the estimations of X_1D, X_2D, X_1B what's more, X_2B. The K-maps for these encoder inputs are appeared in Figure 5.10. From the K-maps, the streamlined articulations of X_1D, X_2D, X_1B and X_2B are determined, and communicated as:

$$X_{1D} = \overline{\overline{A_0^0}B_0^1 + \overline{A_0^1}B_0^2 + \overline{A_0^2}B_0^0}, \quad X_{2D} = \overline{A_0^1B_0^1 + A_0^2B_0^2 + A_0^0B_0^0}$$

$$X_{1B} = 0, \; X_{2B} = \overline{A_0^2 + B_0^0 + A_0^1B_0^1} \qquad \textbf{(5.3)}$$

Table 5.5: Subtraction rules for ternary half subtractor (THS)

A_0	B_0	X_{1D}	X_{2D}	D_0 (Difference)	X_{1B}	X_{2B}	B_0 (Borrow)
0	0	0	0	0	0	0	0
0	1	2	2	2	0	2	1
0	2	0	2	1	0	2	1
1	0	0	2	1	0	0	0
1	1	0	0	0	0	0	0
1	2	2	2	2	0	2	1
2	0	2	2	2	0	0	0
2	1	0	2	1	0	0	0
2	2	0	0	0	0	0	0

As per (5.2) and (5.3), THA can deliver X_1D, X_2D, X_1B and X_2B likewise having appropriate choice of info factors. As a consequence, HASE adds multiplexers with THA to perform subtraction operation, using the design idea of HAS introduced. For XOR work, it includes two transistors T_1 and T2with a binary inverter at the yield of encoder2 to make its Carry/Borrow yield (C0/B0) equivalent to rationale 0 so engendered Carry does not influence the Modulo-3 expansion of A_1 and B_1 in FASE. At the point when mode input M_1= 2, T1 is ON, T2 is OFF and

passes the yield of encoder2 (created Carry/Borrow) to C_0/B_0 for expansion and subtraction operation. At the point when M_1 = 0, T1is OFF, T2 is ON and passes 0 to C_0/B_0 for XOR operation. Along these lines, when M_0 = 0 and M1 = 2, HASE works as THA and register the capacities given by (5.2) for encoder inputs which are then gone through Encoder1 and Encoder2 to create last Sum and Carry yields, individually. So also, when M_0= 2 and M_1 = 2, HASE carries on as a ternary half subtractor (THS) and processes the capacity given by (5.3) for encoder inputs, at that point encoder yields give last subtraction yields. Finally, when M0 = 0 and M_1 = 2, HASE works as a XOR circuit and performs modulo-3 expansion with zero yield Carry.

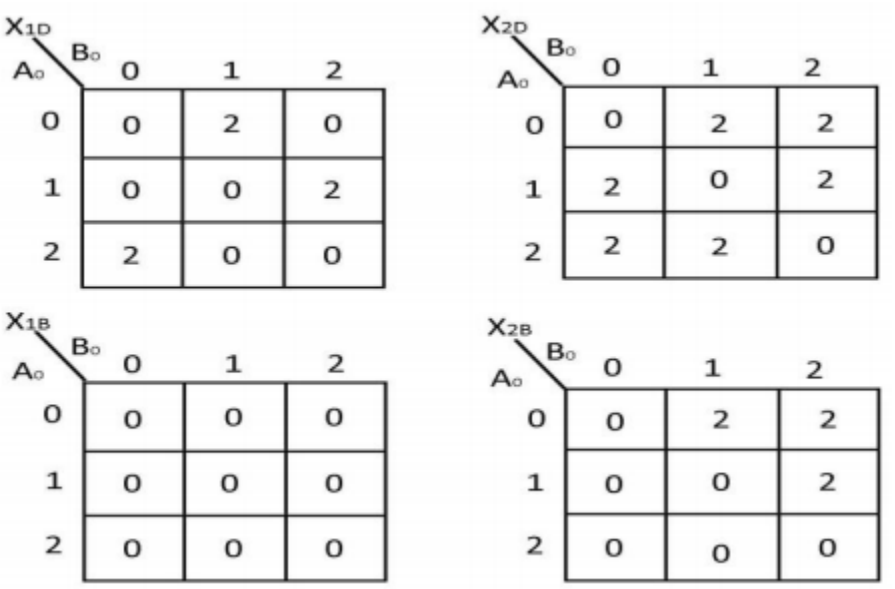


Figure 5.10: K-maps of X_1D, X_2D, X_1B and X_2B for ternary half subtractor (THS)

Full Adder-Subtractor-Exclusive-OR (FASE) Block the proposed FASE performs expansion, subtraction and XOR operations utilizing one ternary full viper (TFA) circuit just with the assistance of multiplexers and pass transistors. A TFA includes three bits in which two are huge bits (1-bit ternary numbers) and third one is Carry bit (C_0) created by the past piece expansion amid N-bit operation. In this, the most extreme total of two 1-bit ternary numbers is 4 in any event noteworthy position and 5 at different positions, which gives most extreme estimation of C_0 i.e. rationale 1. In this manner, C_0 never gets rationale 2 in ternary expansion [257]. By utilizing this idea, TFA is designed in view of the binary nature (0 and 1) of C_0. Thusly, proposed TFA takes out the need of a 1-to-6-line decoder for C0 and employments just a single NTI and a binary inverter for C^0_0 furthermore,C^1_0 . Design of FASE is appeared in Figure 5.11.

Like HASE, the proposed FASE actualizes encoder input factors (X_3S, X_4S, X_3C and X_4C) for realization of TFA, and includes multiplexers and two transistors (with one binary inverter) at the yield of Encoder2 to develop subtractor and selective OR structures, separately. Design rules for expansion operation including X_3s, X_4s, X_3c and X_4c are given in Table 5.6. The K-maps for X_3s, X_4s, X_3c and X_4c are appeared in Figure 5.12. From 125 the K-maps, the rearranged articulations of these encoder inputs are inferred and communicated as takes after

$$X_{3S} = \overline{C_0^0 Y_1 + C_0^1 Y_2}, \qquad X_{4S} = \overline{C_0^0 \overline{Y}_2 + C_0^1 \overline{Y}_3}$$

$$X_{3C} = 0, \qquad X_{4C} = \overline{B_1^0 \overline{A_1^2} + A_1^0 \overline{B_1^2} + C_0^0[(\overline{A_1^2} + B_1^0)(A_1^0 + \overline{B_1^2})]} \quad \textbf{(5.4)}$$

Where

$$Y_1 = \overline{(\overline{A_1^0} + \overline{B_1^0})\ (\overline{A_1^1} + \overline{B_1^2})(\overline{A_1^2} + \overline{B_1^1})}, \quad Y_2 = \overline{(\overline{A_1^0} + \overline{B_1^2})\ (\overline{A_1^1} + \overline{B_1^1})(\overline{A_1^2} + \overline{B_1^0})}$$

$$Y_3 = \overline{(\overline{A_1^0} + \overline{B_1^1})\ (\overline{A_1^1} + \overline{B_1^0})(\overline{A_1^2} + \overline{B_1^2})}$$

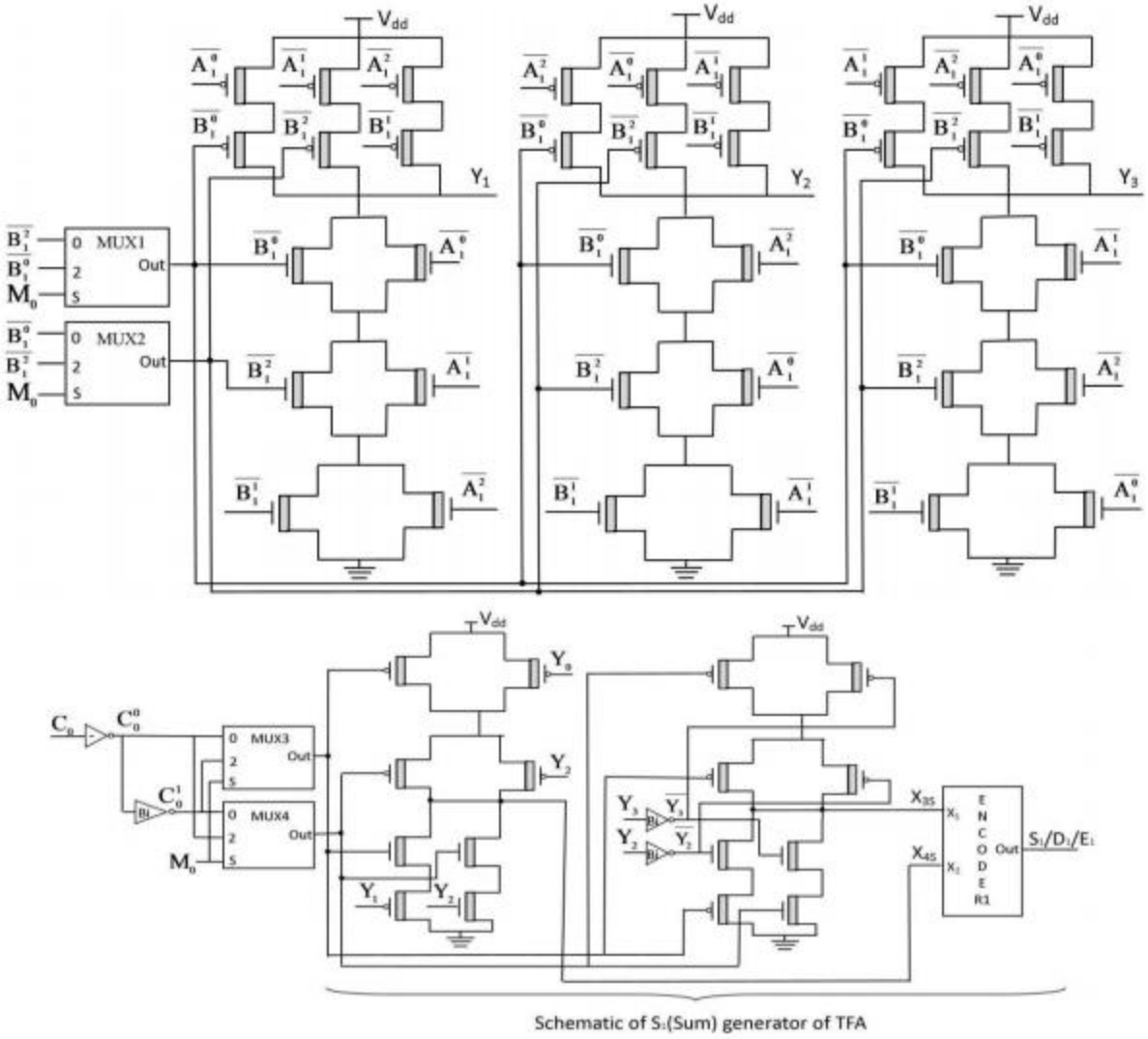


Figure 5.11 (a): Schematic diagram of S1/D1/E1 generator of full adder-subtractor-exclusive OR (FASE)

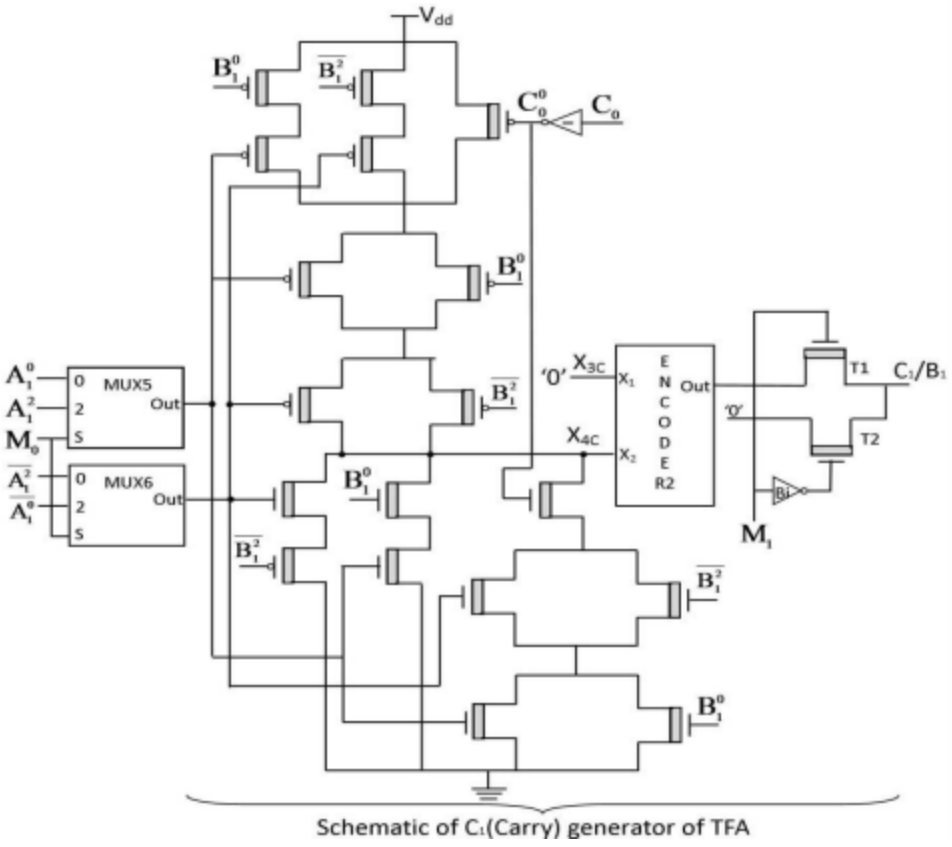


Figure 5.11 (b): Schematic diagram of C1/B1 generator of full adder-subtractor-exclusive OR (FASE)

X_{3S}

A_1 \ B_1	0	1	2
0	0	0	2
1	0	2	0
2	2	0	0

$C_o = 0$

X_{3S}

A_1 \ B_1	0	1	2
0	0	2	0
1	2	0	0
2	0	0	2

$C_o = 1$

X_{4S}

A_1 \ B_1	0	1	2
0	0	2	2
1	2	2	0
2	2	0	2

$C_o = 0$

X_{4S}

A_1 \ B_1	0	1	2
0	2	2	0
1	2	0	2
2	0	2	2

$C_o = 1$

Figure 5.12 (a): K-maps of X3S and X4S for ternary full adder (TFA)

Table 5.6: Addition rules for ternary full adder (TFA)

A_1	B_1	C_0	X_{3S}	X_{4S}	S_1 (Sum)	X_{3C}	X_{4C}	C_1 (Carry)
0	0	0	0	0	0	0	0	0
0	0	1	0	2	1	0	0	0
0	1	0	0	2	1	0	0	0
0	1	1	2	2	2	0	0	0
0	2	0	2	2	2	0	0	0
0	2	1	0	0	0	0	2	1
1	0	0	0	2	1	0	0	0
1	0	1	2	2	2	0	0	0
1	1	0	2	2	2	0	0	0
1	1	1	0	0	0	0	2	1
1	2	0	0	0	0	0	2	1
1	2	1	0	2	1	0	2	1
2	0	0	2	2	2	0	0	0
2	0	1	0	0	0	0	2	1
2	1	0	0	0	0	0	2	1
2	1	1	0	2	1	0	2	1
2	2	0	0	2	1	0	2	1
2	2	1	2	2	2	0	2	1

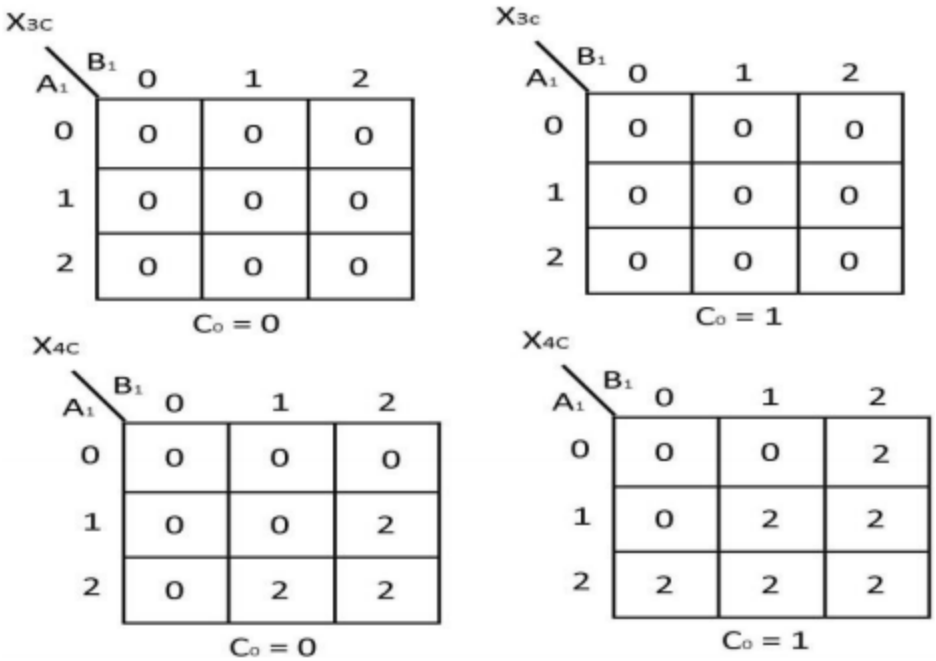


Figure 5.12 (b): K-maps of X3C and X4C for ternary full adder (TFA)

To analyze the basic symmetry exhibit amongst TFA and ternary full subtractor (TFS), encoder input factors X_3D and X_4D for Difference (D1) yield, and X_3B and X_4B for Borrow (B_1) yield of TFS are discovered in view of design lead for subtraction given in Table 5.7. This table likewise incorporates the estimations of X_3D, X_4D, X_3B and X_4B. The K-maps for these encoder inputs are appeared in Figure 5.13. From the K-maps, the streamlined articulations are inferred and communicated as takes after.

$$X_{3D} = \overline{C_0^0 Z_2 + C_0^1 Z_1}\,, \qquad X_{4D} = \overline{C_0^0 Z_3 + C_0^1 \overline{Z_2}}$$

$$X_{3B} = 0, \qquad X_{4B} = \overline{B_1^0 \overline{A_1^0} + A_1^2 \overline{B_1^2} + C_0^0[(\overline{A_1^0} + B_1^0)(A_1^2 + \overline{B_1^2})]} \quad \textbf{(5.5)}$$

Where

$$Z_1 = \overline{(\overline{A_1^0} + \overline{B_1^2})\ (\overline{A_1^1} + \overline{B_1^0})(\overline{A_1^2} + \overline{B_1^1})}, \quad Z_2 = \overline{(\overline{A_1^0} + \overline{B_1^0})\ (\overline{A_1^1} + \overline{B_1^1})(\overline{A_1^2} + \overline{B_1^2})}$$

$$Z_3 = \overline{(\overline{A_1^0} + \overline{B_1^1})\ (\overline{A_1^1} + \overline{B_1^2})(\overline{A_1^2} + \overline{B_1^0})}$$

Eq. (5.4) and (5.5) affirm that TFA and TFS have same schematic with variety in inputs. Contingent on the estimation of mode input M_0 and M_1, the proposed FASE gets particular inputs and in like manner, processes the function given by eq. (5.4) and (5.5) to perform expansion and subtraction operation, separately. For XOR operation, FASE performs expansion of A_1 and B_1 with C_0 which is equivalent to rationale 0, produced from the HASE. In this way, it finishes Modulo-3 expansion for XOR function of A_1 and B_1, with generation of zero yields convey. The operation mechanism of the proposed FASE is like that of proposed HASE.

Table 5.7: Subtraction rules for ternary full subtractor (TFS)

A_1	B_1	C_0	X_{3D}	X_{4D}	D_1 (Difference)	X_{3B}	X_{4B}	B_1 (Borrow)
0	0	0	0	0	0	0	0	0
0	0	1	2	2	2	0	2	1
0	1	0	2	2	2	0	2	1
0	1	1	0	2	1	0	2	1
0	2	0	0	2	1	0	2	1
1	0	0	0	2	1	0	0	0
1	0	1	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
1	1	1	2	2	2	0	2	1
1	2	0	2	2	2	0	2	1
1	2	1	0	2	1	0	2	1
2	0	0	2	2	2	0	0	0
2	0	1	0	2	1	0	0	0
2	1	0	0	2	1	0	0	0
2	1	1	0	0	0	0	0	0
2	2	0	0	0	0	0	0	0
2	2	1	2	2	2	0	2	1

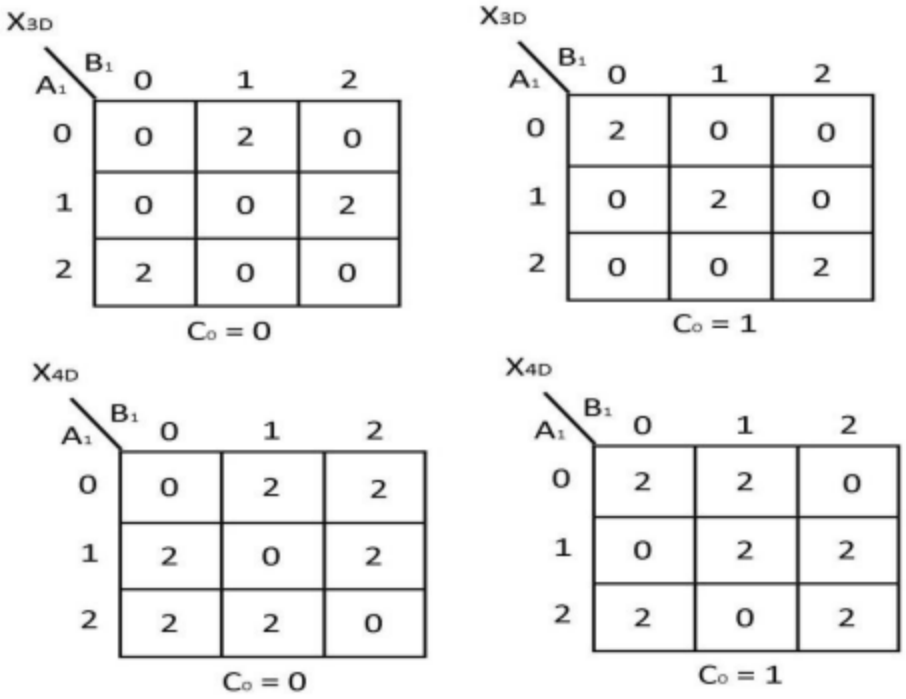


Figure 5.13 (a): K-maps of X3D and X4D for ternary full subtractor (TFS)

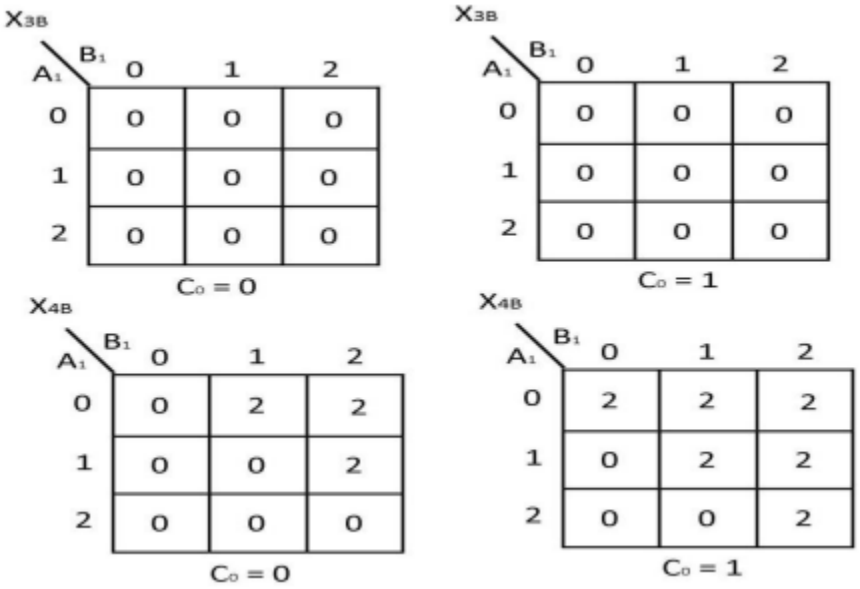


Figure 5.13 (b): K-maps of X3B and X4B for ternary full subtractor (TFS)

It merits mentioning that by performing expansion, subtraction and XOR operations utilizing ASE module, PO-TALU design spares one finish exclusive-OR functional module in correlation

with TALU design of [252]. Alongside this sparing, it additionally spares a subtractor functional module in correlation with TALU design.

5.4.2 Multiplier Module

Figure 5.14 shows implementation of the multiplier functional module (decoded unary functions for input information is not appeared). This module performs augmentation amongst A_1A_0 and B1B0, and produces result of four bits $M_3M_2M_1M_0$. It contains 1-bit multiplier, THA, TFA and another square named as convey snake (CA), for halfway item generation, left shift operations and summation of all shifted incomplete items. These squares are depicted beneath. Design of CA is appeared in Figure 5.15. It is utilized for the expansion of moderate conveys bits which have just two rationale esteems 1 and 0. There are two data sources C1 and C2, and one yield OCA which is ternary in nature. Reality table of CA is appeared in Table 5.8. In view of table 5.2 and table 5.8, the proposed design finds encoder input factors X_1CA and X_2CA. The estimations of X_1CA and X_2CA are additionally incorporated into Table 5.8. The K-maps for X_1CA and X_2CA are appeared in Figure 5.16. The rearranged articulations of these encoder inputs are gotten from the K-maps, and communicated as:

$$X_{1CA} = \overline{C_{1n} + C_{2n}}, \; X_{2CA} = \overline{C_{1n}.C_{2n}} \qquad \textbf{(5.6)}$$

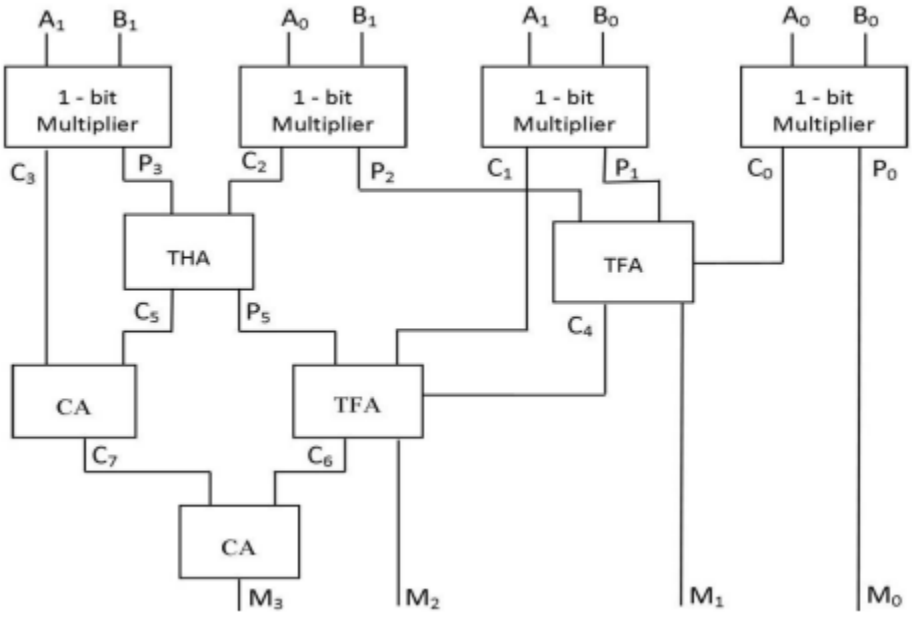


Figure 5.14: Block diagram of multiplier functional module

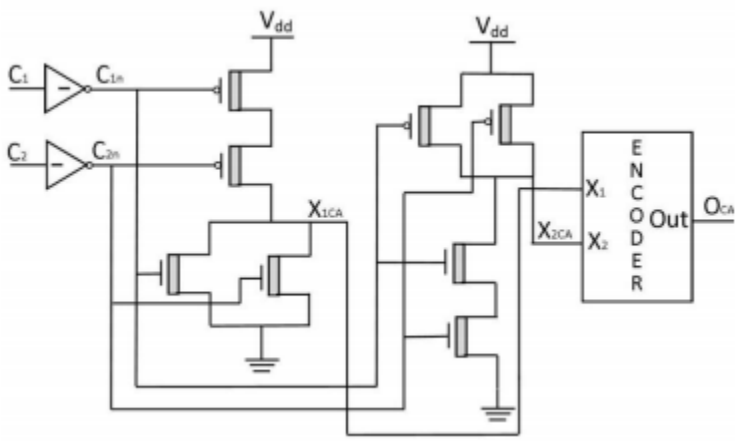


Figure 5.15: Logic level diagram of carry add (CA)

Table 5.8: Truth table of carry add (CA)

C_1	C_2	X_{1CA}	X_{2CA}	O_{CA}
0	0	0	0	0
0	1	0	2	1
1	0	0	2	1
1	1	2	2	2

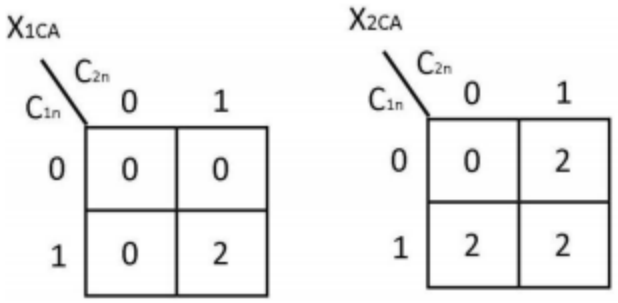


Figure 5.16: K-maps of X1CA and X2CA for CA

The schematic diagram of ternary 1-bit multiplier is appeared in Figure 5.17. In view of design lead of augmentation gave in Table 5.9 and Table 5.2, the proposed design finds encoder input factors X_{1P0}, X_{2P0} for the yield item (P_0) and, X_{1c0} and X_{2c0} for yield convey (C0). The estimations of X_{1p0}, $X_{2p0,}$ X_{1c0} and X_{2c0} are given in Table 5.9. The K-maps for X_{1p0}, X_{2p0}, X_{1c0} and X_{2c0} are appeared in Figure 5.18. The rearranged articulations of these encoder inputs derived from the K-maps, and communicated as takes after

$$X_{1P0} = A_0^2 B_0^1 + A_0^1 B_0^2, \quad X_{2P0} = \overline{\overline{A_0^0} + \overline{B_0^0}}$$

$$X_{1C0} = 0, \quad X_{2C0} = \overline{(\overline{A_0^2} + \overline{B_0^2})} \qquad \textbf{(5.7)}$$

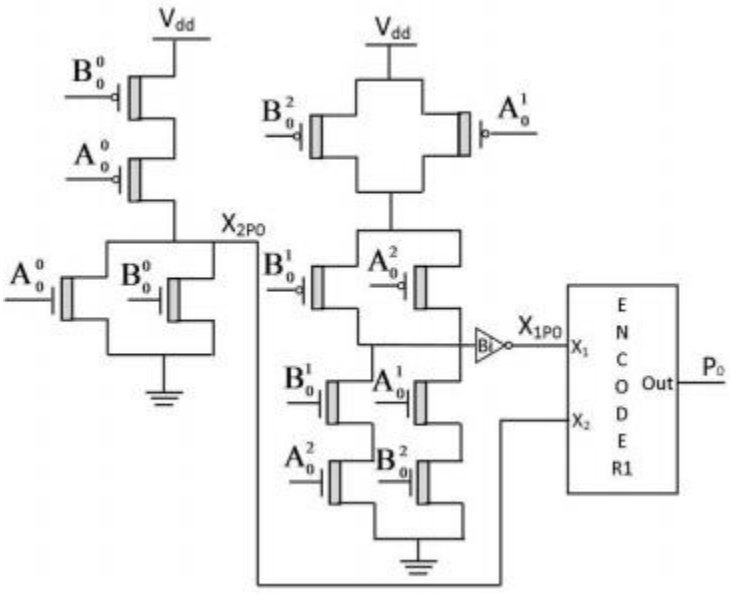


Figure 5.17 (a): Schematic diagram for P0 (Product) generator of ternary 1-bit multiplier

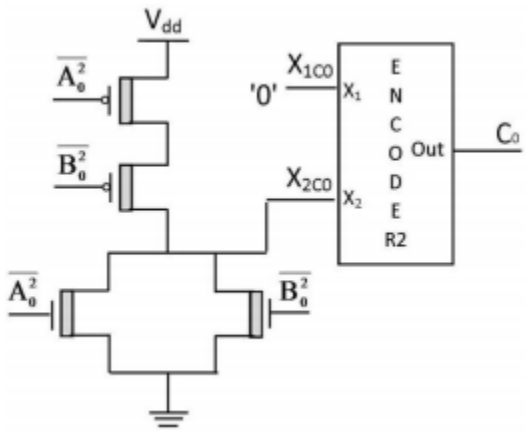


Figure 5.17(b): Schematic diagram for C0 (Carry) generator of ternary 1-bit multiplier

Table 5.9: Design rules for ternary 1-bit multiplication

A_0	B_0	X_{1P0}	X_{2P0}	P_0 (Product)	X_{1C0}	X_{2C0}	C_0 (Carry)
0	0	0	0	0	0	0	0
0	1	0	2	1	0	0	0
0	2	2	2	2	0	0	0
1	1	0	2	1	0	0	0
1	2	0	0	0	0	2	1
2	2	0	2	1	0	2	1

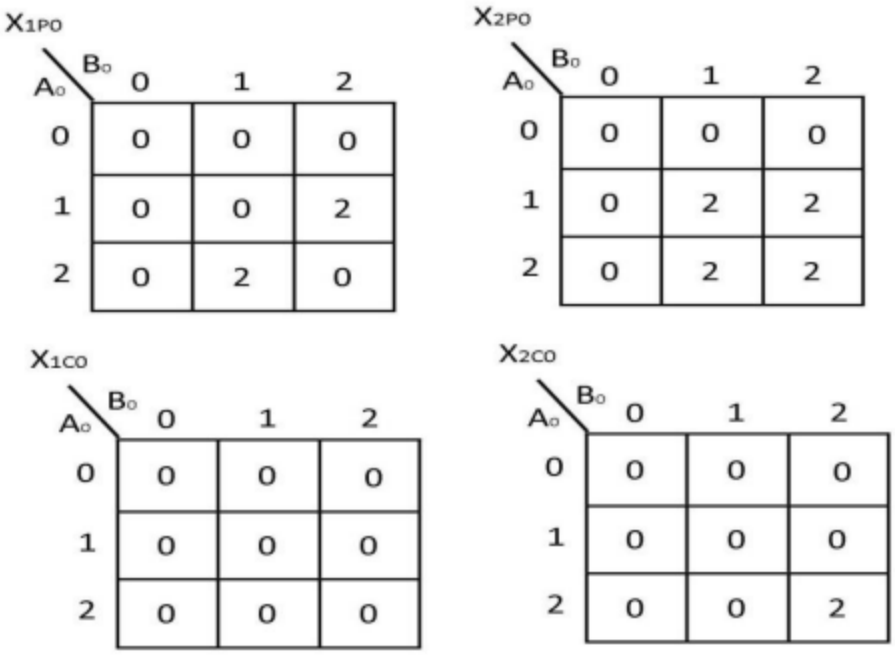


Figure 5.18: K-maps of X1P0, X2P0, X1C0 and X2C0 for ternary 1-bit multiplier

The proposed 1-bit multiplier processes the functions given by (5.7) and creates X_1P_0, X_2P_0, X_1C_0 and X_2C_0. X_1P_0, X_2P_0 are bolstered to an Encoder1 which produces P_0. Likewise, X1C and X2C are encouraged to Encoder2 which produces C_0. Further, the implementation of THA and TFA are same as HASE and FASE, individually, excluding multiplexers and pass transistors. The proposed multiplier functional module decreases no. of transistors at two levels. At first level, it utilizes just two CA obstructs instead of four HA squares utilized as a part of multiplier design]. Also, design of CA contains less number of transistors contrasted with HA. At second level, it utilizes proposed encoder-based 1-bit multiplier, THA and TFA, which are exceptionally conservative in correlation with their counterparts.

5.4.3 Comparator Module

A comparator module is a circuit that performs correlation between An (A1A0) and B (B1B0) and produces two yields represented by GR and EQ. Decoding of these two yields for correlation reaction is appeared in Table 5.10. Design of 2-bit comparator presented in section 4 is utilized

here. This design contains two pass transistor based 1-bit ternary comparators, one binary grouping piece and two binary inverters for non-inverted yields.

Table 5.10: Decoding of outputs for comparison response

Comparator Outputs		Results
GR	EQ	
2	0	Greater
0	2	Equal
0	0	Lesser
2	2	Invalid

Design of logic functional modules TAND and TOR are same as described in chapter 3.

5.5 Implementation of 2-bit PO-TALU Slice

2-bit PO-TALU design is reached out to construct a 2-bit PO-TALU cut which can be fell for n/2 times to develop a N-bit TALU. Figure 5.19 demonstrates the pin diagram of the 2-bit PO-TALU cut. Contrasted with 2-bit PO-TALU, it has some additional inputs named as fell signals: $Carry_c$/$Borrow_c$, GRc and EQc. To include these inputs to acknowledge 2-bit PO-TALU cut, PO-TALU design is altered.Altered ASE (MASE) functional module is appeared in Figure 5.20. MASE utilizes FASE instead of HASE to manage fell Carry/Borrow flag (i.e. $Carry_c$/$Borrow_c$). For N-bit TALU, the fell design of MASE is appeared in Figure 5.21. For expansion and subtraction operations, the operating mechanism of MASE is same as MAS module of 2-bit TALU cut presented in part 3. For XOR operation, each MASE module performs modulo-3 expansion with zero input and yield Carry flag.

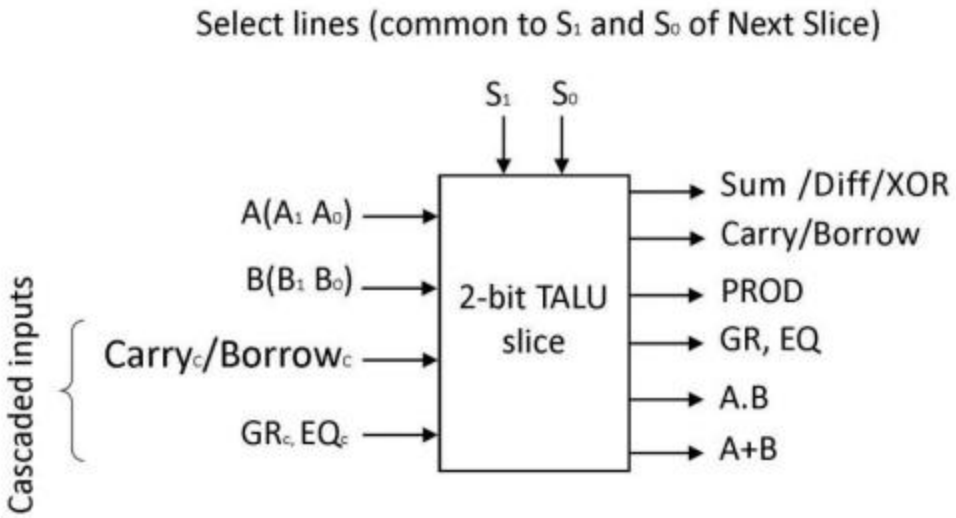


Figure 5.19: Pin diagram of 2-bit PO-TALU slice

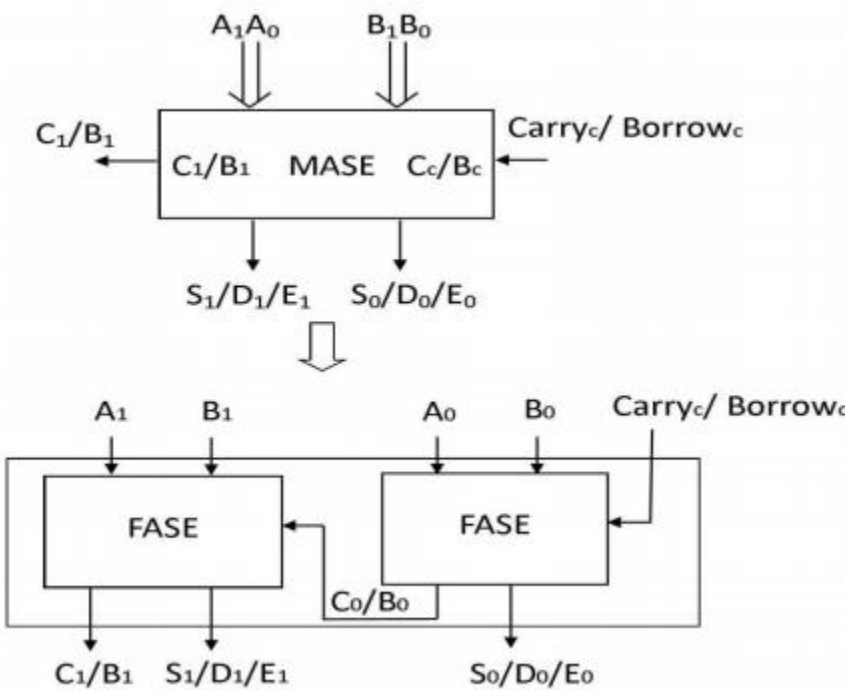


Figure 5.20: Block Diagram for modified adder-subtractor-exclusive-OR (MASE)

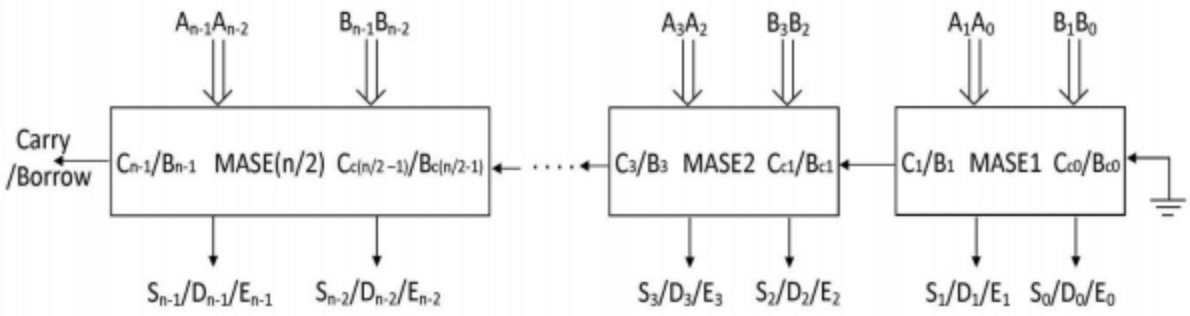


Figure 5.21: Cascaded configuration for modified adder-subtractor-exclusive-OR (MASE) of N-bit PO-TALU

For adjustment of comparator module, grouping rationale technique presented in section 4 isused. Multiplier module is broadened in view of the design strategy of [62]. Rationale modules of PO-TALU which utilize ternary AND (TAND) and ternary OR (TOR) gates just, are most certainly not required any modifications.

5.6 Results and Discussion

In this area, proposed 2-bit PO-TALU design is investigated and mimicked using HSPICE test system with the Stanford display for 32 nm. This standard model has been exhibited in segment 2.2 of part 2. Further, the chirality vector of always exchanged ON transistors utilized as a part of the generation of $V_{dd}/2$ for rationale 1 and in addition in proposed encoder, is (14, 0). The breadth of these transistors is 1.096 nm with the limit voltage of 0.392 V. The chirality vector of every single remaining transistor utilized as a part of the PO-TALU design is (19, 0). The edge voltage of these transistors is 0.289 V with the distance across of 1.487 nm. Other innovation parameters of CNTFET have same esteems as specified in area 2.2 of part 2. To analyze the execution of the proposed circuits depicted in the past areas, the CNTFET-based ternary circuits are repeated and reenacted. Ternary designs utilize an additional power supply (i.e. $V_{dd}/2$), which has been eliminated using always exchanged ON transistors having the chirality vector of (14, 0). The width of the CNTFETs and the estimation of the other gadget parameters are picked

according to the information gave in the individual papers of the writing. Here, ternary designs of part 3 which are eluded.

5.6.1 Functional Verification of 2-bit PO-TALU

For functional confirmation of 2-bit PO-TALU, sub-circuits and additionally whole design of POTALU are tried through transient recreations. The reproduced waveform of the proposed FASE is appeared in Figure 5.22. The initial three waveforms represent inputs A_1, B_1 and C_0 (input Carry/Borrow). At the point when mode inputs M0 = 0 and M1 = 2, FASE performs expansion (A_1+B_1+C_0) and creates yields S_1 (Sum) and C_1 (Carry), which are appeared by the fourth and fifth waveforms individually. Likewise, when M_0 = M_1 = 2, FASE performs subtraction (A_1- B_1-C_0) and creates two yields D_1 (Difference) and B_1 (Borrow), which are appeared by the fifth and 6th waveforms individually. Finally, when M_0 = M_1= 0, FASE performs modulo-3 expansion with zero yield convey to execute XOR operation. For this, it produces E1 (i.e. A_1 XOR B_1) and C_1 (Carry-XOR), which are shown in the remaining two waveforms. Depending upon the estimation of mode inputs M_0 and M_1, FASE performs redress ternary expansion, subtraction and XOR operations and along these lines, the functionality of FASE is confirmed. Essentially, the mimicked transient waveforms included in Appendix, affirms the right functionality of proposed HASE, CA, 1-bit multiplier, and rationale function modules (as it were TOR is appeared).

5.6.2 Performance Evaluation of 2-bit PO-TALU

To assess execution of proposed ternary circuits, speed and power are removed from transient reenactments. The normal power utilization is measured over a drawn out stretch of time. For most pessimistic scenario postpone determination, all conceivable yield move delays are measured. On record of the exchange off between power utilization and postponement, the productivity of the circuits is assessed by computing power-postpone item (PDP), which is the increase of the normal power utilization and the most extreme postponement. Reproductions are performed at room temperature, at 250 MHz operating recurrence and at 0.9 V power supply voltage with yield stack capacitor of 2.1 fF. Further, to assess the execution at TALU engineering level, data pathsof PO-TALU, which contains decoder, FSB-ALO, TGB-ALE and functional module, have been reenacted. An examination on delay, power utilization, and PDP

and gadget number of CNTFET-based viper circuits is appeared in Table 5.11. Reproduction comes about demonstrate that the proposed THA accomplish awesome change in power by 68%, with decrease in delay by 8% and 11% contrasted with the THA and HAS individually. Moreover, it indicates diminishment in gadgetnumber by 41% and 53% as for the THA and HAS individually.

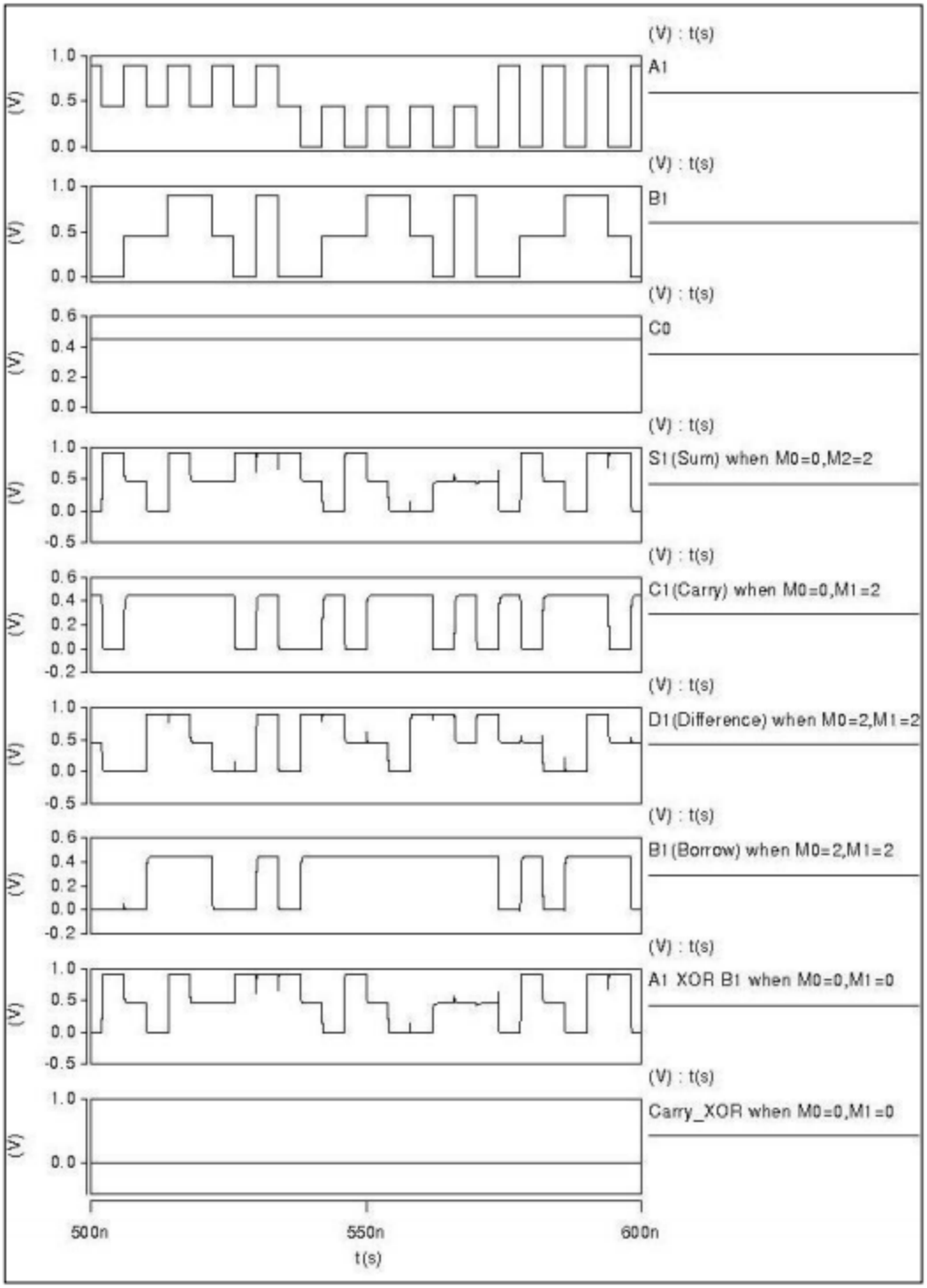


Figure 5.22: Transient waveform of full adder-subtractor-exclusive-OR (FASE)

Table 5.11: Simulation results of CNTFET-based ternary adder circuits

Circuits	Delay ($\times 10^{-10}$ S)	Power ($\times 10^{-6}$ W)	PDP ($\times 10^{-16}$ J)	Device Count
Proposed THA	0.63	0.47	0.30	66
THA of [199]	0.69	1.47	1.02	112
Proposed HASE	0.66	0.49	0.32	82
HAS of [252]	0.71	1.48	1.05	142
Proposed TFA	0.83	0.82	0.68	114
TFA of [256]	0.61	1.63	0.99	105
TFA of [257]	1.00	1.45	1.45	102
TFA of [199]	0.80	1.91	1.53	214
TFA of [255]	0.73	6.89	5.05	106
TFA of [212]	1.44	4.35	6.26	122
TFA of [213]	0.87	53.7	46.7	142
Proposed FASE	0.87	0.86	0.75	140
FAS of [252]	0.82	1.95	1.61	280

Likewise, the proposed HASE (for ADD operation) consumes 66% less power with 4% and 7% less postpone contrasted with the THA and HAS, individually. Also, it gets decrement in gadget include by 26% and 42% correlation with the THA and HAS, individually. According to the reported aftereffects of Table 5.11, the proposed TFA indicates most reduced power among all the CNTFET-based TFA designs. It consumes less power by half however it has increase in postponement and gadget number by 26% and 7%, separately. In examination with TFA, it accomplishes 44% decrease in power and 20% lessening in delay however gadget number is increased by 10%. The proposed TFA indicates change in power and gadget tally by 57% and 47% with an increase in delay by 3% as it were. In correlation with TFA, it spares power by 88% however demonstrates 12% and 7% increase in postponement and gadget check, individually. it accomplishes diminishment in power, deferral and gadget check by 81%, 42% and 7%, separately. Additionally, the proposed TFA demonstrates change in power, postponement and gadget check by 81%, 5% and 20%, separately, concerning the design. In correlation with FSA, it gets 58% diminishment in power and 59% lessening in gadget number with equivalent defer execution. Table 5.11 additionally demonstrates that the proposed FASE (for ADD operation) gets focal points in power and deferral with gadget check contrasted with different designs.

Recreation consequences of CNTFET-based multiplier circuits are recorded in Table 5.12. According to Table 5.12, the proposed 1-bit and 2-bit multipliers have least power among all

CNTFET-based multiplier designs. The proposed 1-bit multiplier gets change in power; postponement and gadget check by 70%, 5% and 37%, individually, contrasted with its partner presented in [199]. So also, the proposed 2-bit multiplier demonstrates 62% lessening in power, 31% decrease in delay and 65% lessening in gadget tally as for 2-bit multiplier. Ternary circuits are additionally recreated at 500MHz operating recurrence with 1fF yield load and little transient time interval. Results obtained from these recreations are recorded. Also, execution parameters removed from the reproductions done at design level, are appeared in Table 4 of Appendix II. Further, as found in Table 5.11, in this manner the proposed TFA is contrasted and these TFA designs just in the following reproductions.

Table 5.12: Simulation results of CNTFET-based multiplier circuits

Circuits	Delay ($\times 10^{-10}$ S)	Power ($\times 10^{-6}$ W)	PDP ($\times 10^{-16}$ J)	Device Count
Proposed 1-bit multiplier	0.51	0.29	0.15	50
1-bit multiplier of [199]	0.54	0.97	0.52	80
Proposed 2-bit multiplier	1.00	2.94	2.94	458
2-bit multiplier of [252]	1.45	7.82	11.34	1296

To examine the driving capability, the proposed designs are tried under various loading conditions. Reproductions are performed with various estimations of yield stack ranging from 2fF to 6fF at room temperature with 0.9V power supply and 250 MHz operating recurrence. The delay, power utilization and PDP of TFA designs versus stack capacitor are plotted in Figure 5.23. The plotted outcomes demonstrate that the proposed design outflanks every single other design as far as power and PDP at all estimations of yield stack.

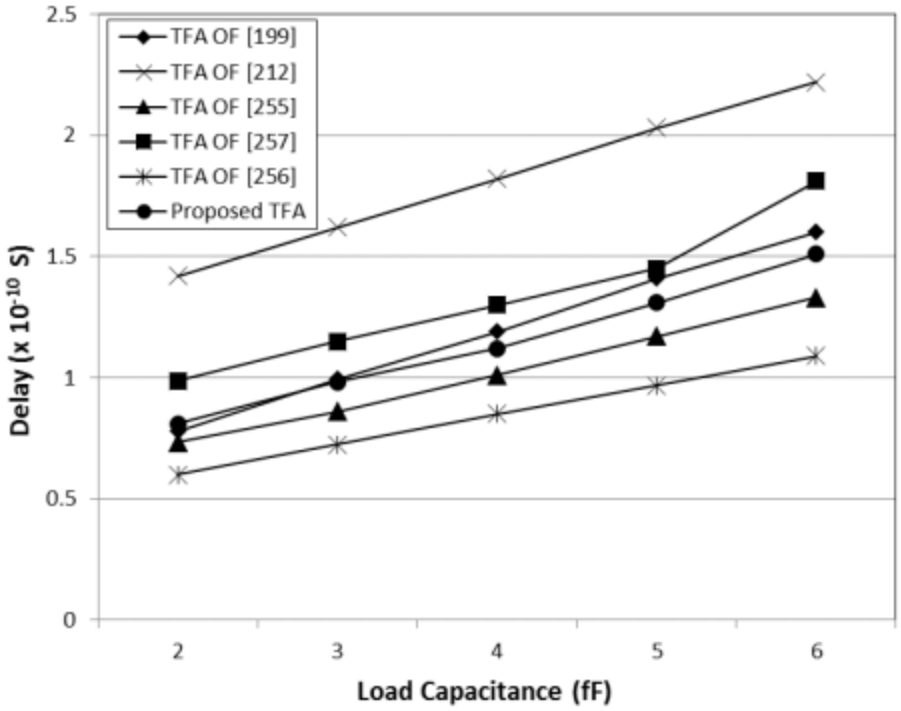


Figure 5.23 (a): Delay versus output load capacitor plot for six ternary full adder (TFA) designs

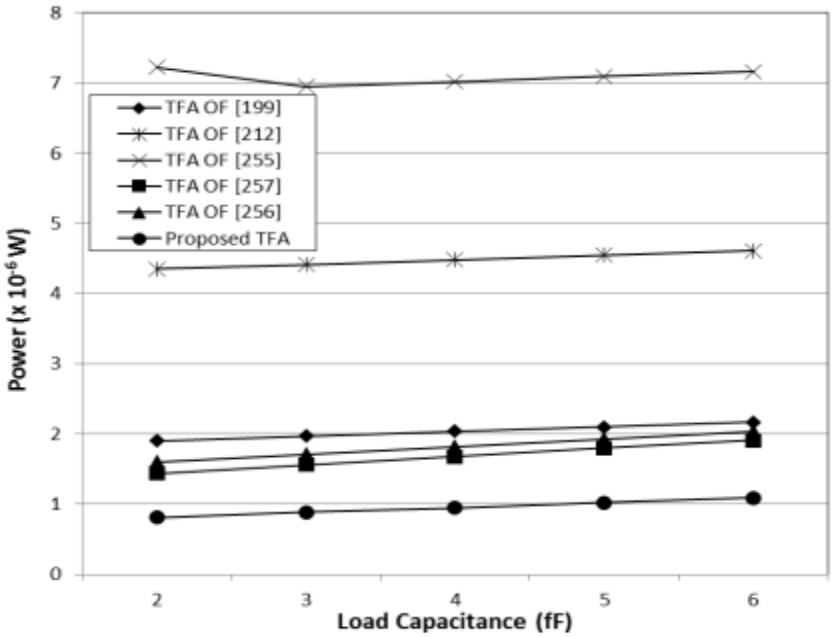


Figure 5.23 (b): Power consumption versus output load capacitor plot for six ternary full adder (TFA) designs

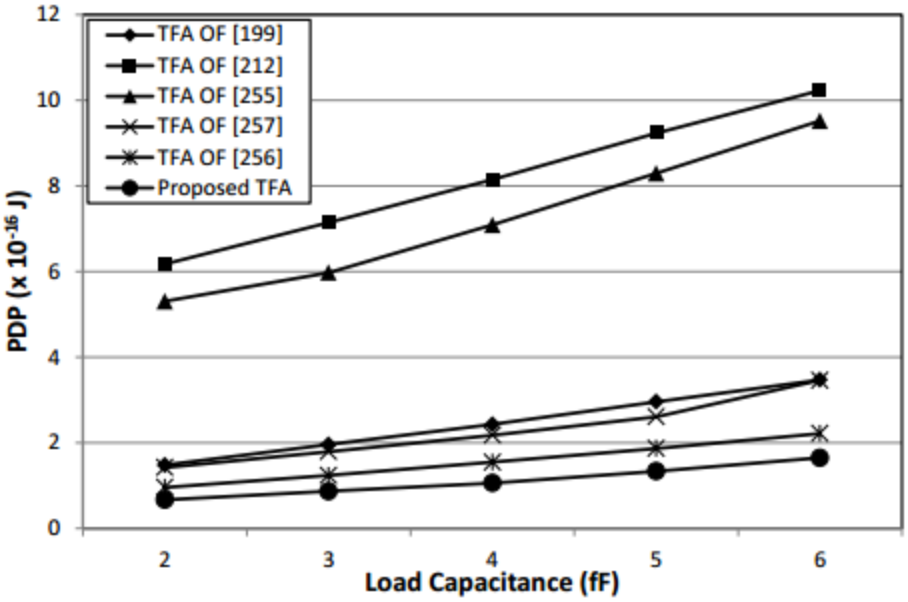


Figure 5.23 (c): Power-delay product (PDP) versus output load capacitor plot for six ternary full adder (TFA) designs

To assess the execution of proposed designs at various frequencies, recreations are performed at operating recurrence varying from 100 MHz to 1000 MHz with room temperature, 0.9 V power supply and 2.1 fF yield stack. The power utilization of TFA designs with various recurrences is appeared in Figure 5.24. For THA and multiplier designs, the power utilization come about with various recurrences are appeared in Figure 1 and Figure 2 of Appendix II. According to the plotted outcomes, proposed designs work legitimately, and devour less power contrasted with all other existing designs, at all frequencies. The proposed designs are tried under voltage varieties to check their sensitivity to these varieties. Recreation is performed at various supply voltages ranging from 0.7 V to 1.1 V. Other recreation parameters are consumed as space temperature, 250 MHz recurrence and 2.1fF yield stack. For TFA designs, PDP registered from this reproduction is plotted in Figure 5.25. PDP consequences of THA and multiplier are plotted in Figure 3 and Figure 4 of Appendix II.

According to the plotted outcomes, proposed designs are less delicate to voltage variety in examination with their counterparts. Recreations are additionally led at various temperatures varying from 0◦C to 100◦C. Other test parameters are 0.9 V supply voltage, 250 MHz recurrence

and 2.1 fF yield stack. PDP with temperature variety is appeared in Figure 5.26. It can be inferred from the outcomes that the proposed designs work dependably and beats existing designs in a huge scope of ambient temperatures.

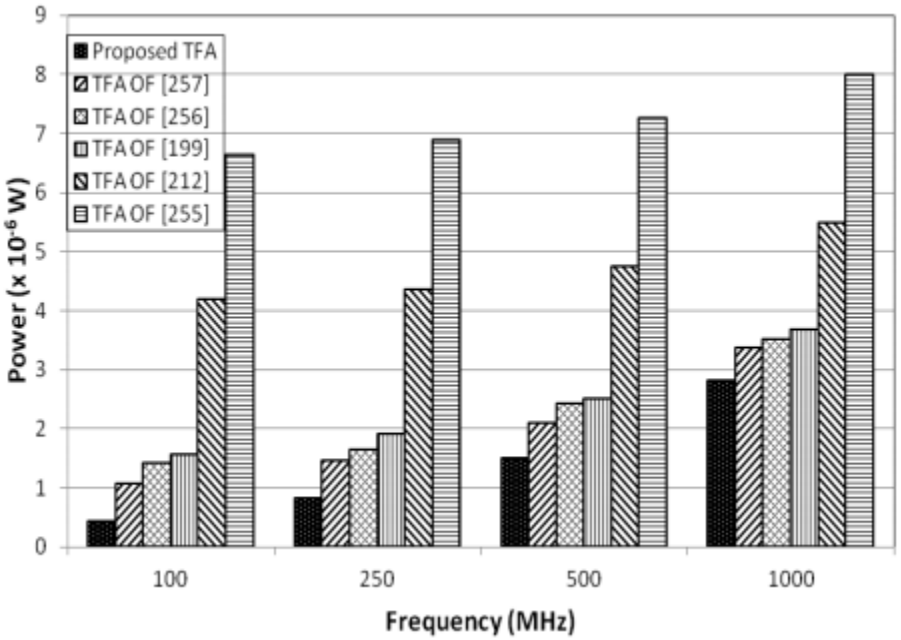


Figure 5.24Power consumption versus operating frequency plot for six ternary full adder (TFA) designs

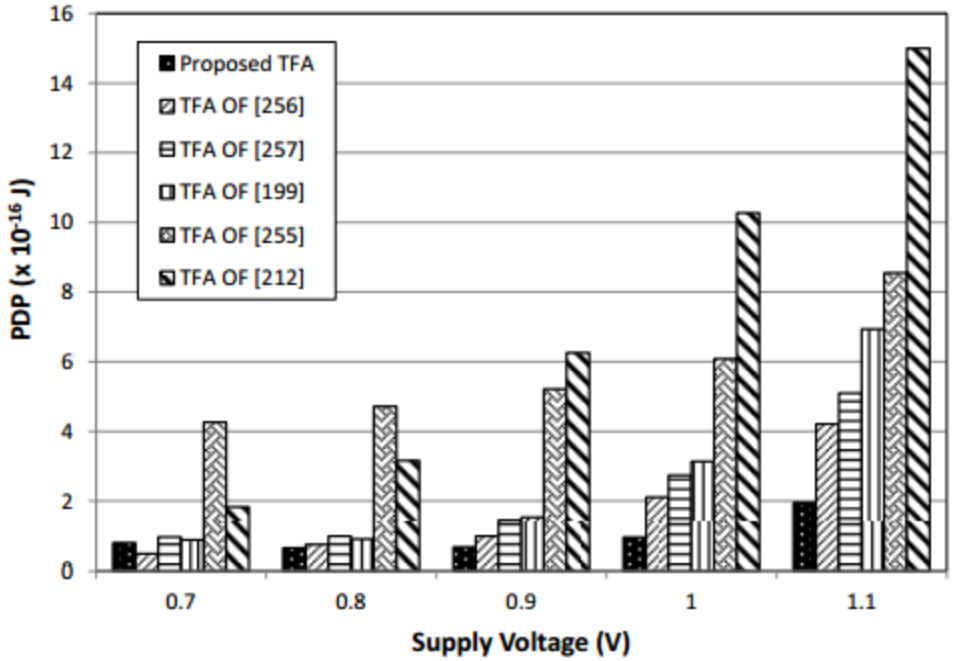


Figure 5.25 Power-delay product (PDP) versus supply voltage plot for six ternary full adder (TFA) designs

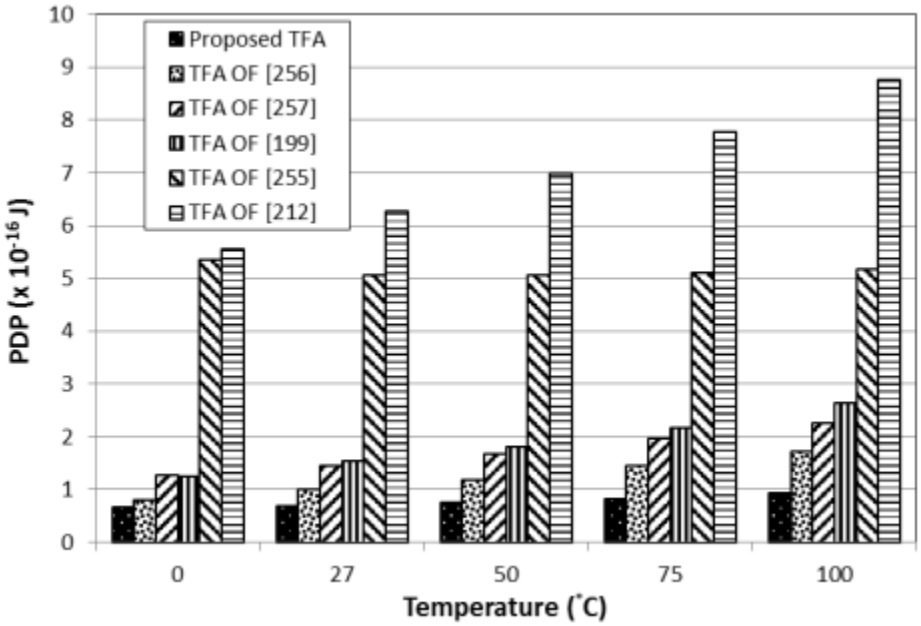


Figure 5.26 Power-delay product (PDP) versus temperature plot for six ternary full adder (TFA) designs

5.7 Conclusion

This section has presented a 2-bit PO-TALU in CNTFET innovation. PO-TALU functional modules: ASE and multiplier have been designed using new integral CNTFET-based binary computational unit and a low unpredictability encoder. ASE eliminates an exclusive-OR module and subtractor module from the conventional design. Multiplier utilizes another effective CA obstruct set up of THA. In correlation with existing vitality effective CNTFET-based designs, HSPICE reenactment comes about have demonstrated that the sub-pieces of ASE: HASE and FASE devour 66% and 47% less power. HASE indicates decrease in delay and gadget count by 4% and 26%, correspondingly. FASE indicates 25% decrease in gadget count yet it has 29% more delay. Sub-piece of multiplier module: 1-bit multiplier demonstrates diminishment in power, delay and gadget count by 70%, 5% and 37%, individually. ASE and multiplier are less sensitive to voltage and temperature varieties. Design of 2-bit PO-TALU has been changed to execute 2-bit PO-TALU cut which could be effortlessly cascaded to shape a N-bit PO-TALU.

Chapter 6

Design of High Speed Content Addressable Memory (CAM) cells using CNTFETs

6.1. Introduction

Content addressable memory (CAM) is an application particular memory that permits its access in view of the put away data instead of a physical address area. CAM performs parallel data examination with data stockpiling, and the consequence of this correlation is determined by the condition of the match lines. There are two sorts of CAM: Binary CAM (BCAM) and Ternary CAM (TCAM). BCAM is equipped for storing and searching two rationale states: 0 and 2. This cell performs correct match looks and is mainly utilized for label examination in reserve memory. TCAM is fit for storing and searching three rationale states: 0, 2 and couldn't care less (X). Consequently, TCAM gives an additional adaptability of example matching with the utilization of X. An interchange design of a TCAM using three-esteemed circuit structure (i.e. 3CAM) has been presented in the writing keeping in mind the end goal to lessen cell zone. A 3CAM takes a shot at genuine esteemed ternary rationale esteems: 0, 1 and 2, where rationale 1 represent couldn't care less (X) state. TCAM are prevalent mainly to realize organize applications, for example, bundle forwarding and parcel characterization. Specifically, elite system switches require a great deal of quick TCAM cells to get sought quick look-into operation in bigger routing tables. In this manner, design of quick and minimized CAM structure continues to be of the most noteworthy need without a doubt time applications.

In this part, BCAM and TCAM cells designed in view of low capacitance look rationale of [235] are presented in CNTFET innovation. Another three-esteemed CAM (3CAM) cell is moreover presented. This cell utilizes CNTFETs with two diverse edge voltages in implementation of low capacitance look arrange which prompts quick and minimized CAM design concerning CNTFET based 3CAM cell as of late reported in the writing. In segment 6.2, design and implementation of CNTFET-based BCAM, TCAM and 3CAM cells are presented. Segment 6.3 gives reenactment results and examination with the existing designs, trailed by the conclusion in area 6.4.

6.2 Design of CAM Cells

6.2.1 Binary CAM (BCAM) Cell

Figure 6.1 demonstrates a schematic diagram of CNTFET-based BCAM cell actualized using nine transistors and named as 9T BCAM cell. It is fit for storing and searching two rationale states: 0 and 2. 9T BCAM comprises of an essential 6T SRAM cell for data stockpiling, and a pursuit organize for data examination. SRAM cell includes a hook containing transistors T1, T2, T3 and T4, alongside two access transistors T5 and T6. T5 and T6 are turned ON at whatever point a word line WL is enacted for a perused or compose operation, and associate the cell to the complementary data line sections DL and DL. The data is put away at the nodes Q and Q of the cell.

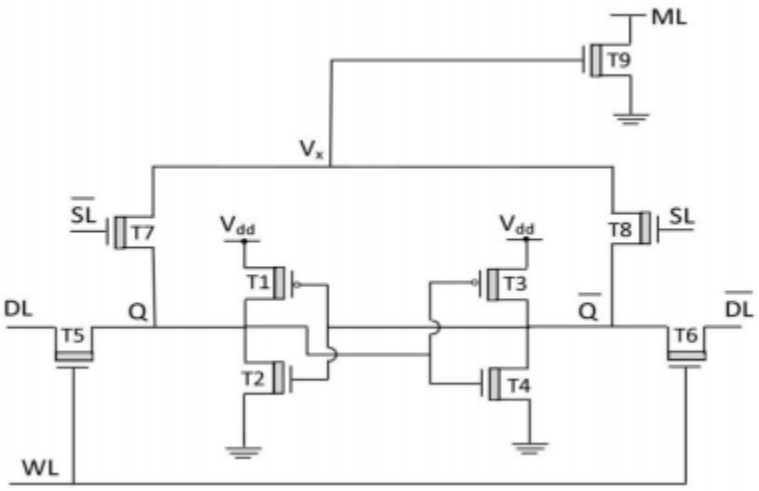


Figure 6.1 Schematic diagram of 9T Binary CAM (BCAM) cell

Read/Write Operation

For read operation, DL and DL lines are precharged to high, and left floating. At the point when WL is high, T5 and T6 are ON and voltage levels of Q and ¯Q are transferred to DL and ¯DL, and data stored in cell is perused. During this operation, both storage nodes Q and ¯Q remain unchanged. For compose operation, wanted data and its supplement is put on DL and DL. At the point when WL is high, T1 and T2 are ON and voltage levels of DL and DL are transferred to Q

and ¯Q, and data is built into the cell. For a successful read and keep in touch with the cell, SRAM transistors ought to be legitimately estimated. The sizing proportion of lock pull-up transistor (T1 and T3) to access transistor (T5 and T6) is taken as 0.5, and the sizing proportion of lock pull-down transistor (T2 and T4) to access transistor (T5 and T6) is taken as 1.5. In CNTFET, sizing is chosen by the quantity of tubes. Thusly, T1 and T3 are utilized with one tube, T2 and T4 are utilized with three tubes, and the quantity of tubes utilized for T5 and T6 is two. The chirality vector for P-CNTFETs (T1 and T3) and N-CNTFETs (T2, T4, T5 and T6) of SRAM cell are picked as (16, 0) and (19, 0) separately, for the best-combined execution as far as stability, power utilization, and compose time of SRAM cell.

SearchOperation

The pursuit system of 9T BCAM cell is designed in view of low-capacitance seek rationale to accelerate think about operation. It contains three transistors T7, T8 and T9 with chirality vector of (19, 0). The quantity of tubes is three. 9T-BCAM looks at the data stored at Q and its supplement (¯Q) with the data set on seek lines SL and its supplement (¯SL), separately. At the point when the esteem stored at Q matches with the incentive at SL, rationale 0 is passed through either T7 or T8 to the hub V_x which is the entryway of T9 and thusly, T9 is turned OFF and coordinate line ML is disconnected from ground for a match condition. Also, when data at Q doesn't coordinate with SL, V_x is charged to 0.9 V (rationale 2) through either T7 or T8, which turns ON T9 and shorts ML with ground for a jumble condition. For instant, whenSL = 1, ¯SL = 0, T7 is OFF and T8 is ON, which exchanges the voltage level of ¯Q to Vx. For Q = 2, Q is rationale 0 and thus, rationale 0 is transferred to V_x for coordinate condition. At the point when Q = 0, ¯Q is rationale 2 and subsequently, rationale 2 is transferred to V_x for jumble case. So also, when ¯SL = 0, ¯SL = 2, T7 is ON and T8 is OFF, which exchanges the voltage level of Q to V_x. For Q = 0, rationale 0 is transferred to Vx for coordinate condition and when Q = 2, rationale 2 is transferred to Vx for befuddle condition.

6.2.2 Ternary CAM (TCAM) Cell

Figure 6.2 demonstrates a schematic diagram of CNTFET-based TCAM cell actualized using 16 transistors and named as 16T TCAM cell. This cell is proficient to store and inquiry three rationale states: 0, 2 and couldn't care less (X). These states are encoded by two bits as appeared

in Table 6.1. 16T TCAM incorporates two SRAM cells for data storage and one analyze arrange for data examination. These SRAM cells store '02', '20', and "22" for the cell storage of 0, 2 and couldn't care less (X), individually. This "X" esteem represents a stored couldn't care less. The state "00" is not utilized and never allowed for data storage. The design parameters of SRAM cell are same as that of 9T BCAM. The read and compose operation of TCAM cell is like BCAM

Table 6.1 Ternary encoding for 16T ternary CAM (TCAM) cell

Ternary State	Stored data		Search data	
	Q_0	Q_1	SL_0	SL_1
0	0	2	0	2
2	2	0	2	0
X	2	2	0	0

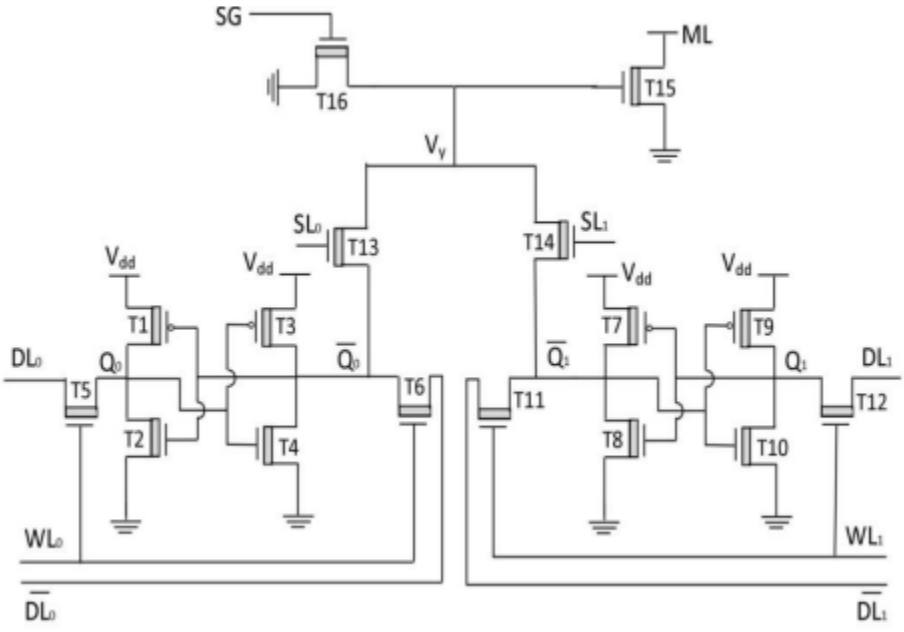


Figure 6.2: Schematic diagram of 16T ternary CAM (TCAM) cell

Search Operation

The think about system of 16T-TCAM utilizes low-capacitance seek rationale keeping in mind the end goal to achieve rapid pursuit operation. It contains four transistors T13, T14, T15 and T16 with chirality vector of (19, 0). The entryway of T16 is connected to one control line indicated by 'SG'. This control line is created by NORing of pursuit line SL0 and SL1, and shared by every one of the cells in a similar section of the memory. The cell looks at data stored at hub Q_0 and Q_1, with the inquiry data set on the SL_0 and SL_1. For worldwide masking, it performs searching with X by setting both SL_0 and SL_1 to 0. The state "22" is not allowed as a searching state. At the point when $SL_0 = SL_1 = 0$, SG line is set to rationale 2 and T16 is turned ON. In this case, T13 and T14 are OFF, and hub Vy which represents door of T15, is connected to ground through T16. Subsequently SG line evacuates floating condition at Vy when bits are globally covered.

A 16T TCAM cell behaves like 9T BCAM cell at whatever point 0 and 2 is stored or being sought. For instance, when $SL_0 = 0$ and $SL_1 = 2$, T13 is OFF and T14 is ON, whichtransfers the rationale level of $\bar{Q}1$ to Vy. For Q0 = 0 and Q1 = 2, $\bar{Q}1$ is rationale 0 and consequently, 0 is transferred to Vy which kills T15 and disconnects coordinate line ML from ground to indicate a match case. At the point when Q0 = 2 and Q1 = 0, $\bar{Q}1$ is rationale 2 and thus, Vy is set at rationale 2 which turns ON T15 and associates ML to ground to indicate a mismatch case. In the same way, when SL0 = 2 and SL1 = 0, T13 is ON and T14 is OFF, which transfers $\bar{Q}_0$ to V_y. For$Q_0 = 2$ and $Q_1 = 0$,Q_0 is rationale 0 and in this way, V_y is set at rationale 0 which kills T15 and disconnects ML from ground indicating a match case. At the point when $Q_0 = 0$ and Q1 = 2, $Q_0$is rationale 2 and along these lines, V_y is set at rationale 2 which turns ON T15 and associates ML to ground to indicate a mismatch case.

At the point when a 16T TCAM stores a X i.e. $Q_0 = Q_1 = 2$, V_y is set at rationale 0 through T13 for $SL_0 = 2$ and $SL_1 = 0$, or through T14 for $SL_0 = 0$ and $SL_1 = 2$, or through T16 for SL0 = 0 and $SL_1 = 0$. This estimation of V_y kills T15 and thus, ML is disconnected from ground. Accordingly, the stored X dependably demonstrates a match independent of the pursuit data. Presently, when there is a look for X i.e. $SL_0 = SL_1 = 0$, both T13 and T14 are OFF. For this situation, control line SG is set to rationale 2 which interfaces V_y to ground through T16. T15 is killed and along these

lines, ML is not shorted to ground and indicates a match paying little heed to the stored data. This match case affirms worldwide masking highlight of 16T TCAM.

6.2.3 Three-Valued CAM (3CAM) Cell

Figure 6.3 shows schematic diagram of proposed CNTFET-based 3CAM cell. This cell is executed using 11 transistors and named as 11T-3CAM cell. It contrasts from TCAM in a way that it takes a shot at genuine esteemed ternary rationale. 11T-3CAM is competent to store and pursuit three rationale states: 0, 1 and 2, where rationale 1 is utilized for couldn't care less state (X). Figure 6.3: Schematic diagram.

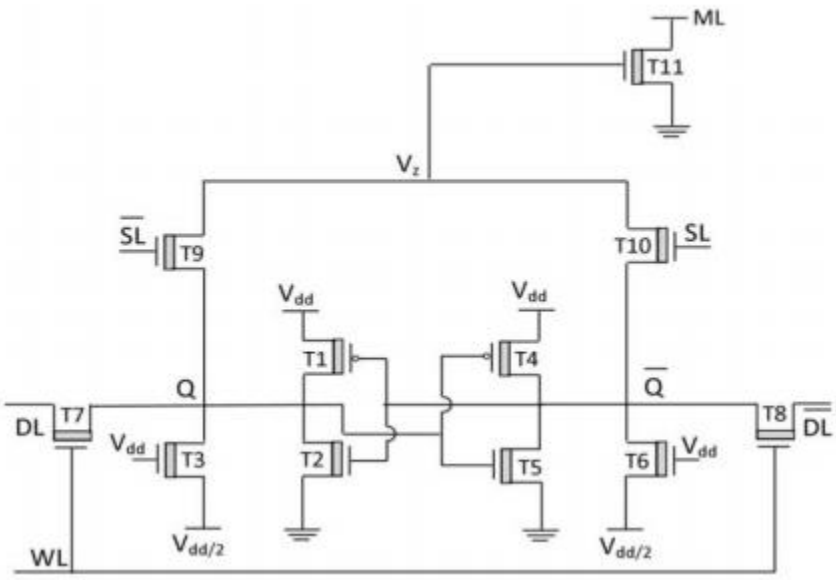


Figure 6.3: Schematic diagram of 11T three-valued CAM (3CAM) cell

Read/Write Operation

11T-3CAM cell utilizes one ternary memory (TMEM) cell of [247] for data storage, and eliminates the requirement for a moment storage cell (i.e. SRAM) normally utilized as a part of traditional TCAM construction. TMEM cell contains two cross coupled static ternary inverters (STIs); STI has one input signal ¯Q which can be at out of three esteems: 0, 1 and 2, and produces a yield Q with a rationale estimation of 2-Q (i.e. 2, 1 or 0, individually). Two STIs contain transistors T1, T2, T3, T4, T5 and T6. They utilize two power supplies: a general supply

voltage (V_{dd}) and a lower supply voltage ($V_{dd}/2$). The chirality vector of T1 and T4 is (8, 2). The quantity of CNTs is eight. The chirality vector of T2 and T5 is likewise (8, 2). The limit voltage of these transistors is 0.599 V with the width of 0.718 nm. The quantity of CNTs is twenty. The chirality vector of T3 and T6 is (10, 0). The edge voltage of these transistors is 0.55 V with the width of 0.783 nm. The quantity of CNTs is two. These transistors are connected between voltage rail $V_{dd}/2$ and hub Q, and $\bar{Q}$, separately. The door of these transistors is connected to V_{dd} causing them to be dependably ON which essentially go about as draw up for rationale 1. Be that as it may, they likewise allow a dc way to exist at whatever point pull up for rationale 2 and draw down for rationale 0 happens. To minimize this fight, T3 and T6 are made weaker by reducing number of tubes to two, lowering the pitch to 10 nm and increasing the channel length to 64 nm. Alongside two cross coupled STIs, TMEM cell contains two access transistors T7 and T8with the chirality vector of (19, 0). The edge voltage of these transistors is 0.289 V and breadth is 1.487 nm. The quantity of CNTs is three. TMEM cell stores data at Q and $\bar{Q}$. For read operation, complementary data line segments DL and DL are precharged to rationale 2 and left floating. At the point when WL is attested, T7 and T8 are ON and voltage levels of Q and $\bar{Q}$ are transferred to DL and $\bar{D}L$, and data stored in cell is perused. During the read operation, both storage nodes Q and$\bar{}$ Q remain unchanged. For compose operation, craved data and its supplement are put on DL and$\bar{D}L$. At the point when WL is declared, T7 and T8 are ON and voltage levels of DL and DL are transferred to Q and $\bar{Q}$, and data is built into the cell.

Search Operation

11T-3CAM contains one new analyze organize for data examination. This think about system uses low-capacitance look rationale to get quick match operation. It comprises of three transistors T9, T10 and T11. 11T-3CAM thinks about complementary ternary data stored at Q and $\bar{Q}$ with the complementary data set on the hunt line SL and $\bar{S}L$. Correct matching is actualized through storing and accordingly searching for either rationale 0 or rationale 2. Example matching is finished with nearby and worldwide masking. In nearby masking, rationale 1 is stored at both Q and Q which represents a stored couldn't care less. Worldwide masking is performed through searching for rationale 1 on both SL and$\bar{S}L$ which represents a sought couldn't care less state. To get coordinate at whatever point rationale 1 is stored or being sought, the limit voltage of T11 is set as 0.55 V using the chirality vector of (10, 0). The distance across

of T11 is 0.783nm. The edge voltage of T9 and T10 is taken as 0.289 V using the chirality vector of (19, 0). The distance across of these transistors is 1.487nm. A 3CAM cell behaves like TCAM at whatever point rationale 0 or rationale 2 is stored or being looked. For instance, when rationale 2 is stored, Q is at rationale 2 and Q is at rationale 0. In the event that there is a look for rationale 2 i.e. SL = 2 and SL = 0, T9 is OFF and T10 is ON, which drives hub Vz to rationale 0, as a consequence T11 is OFF and coordinate line (ML) is not shorted to ground indicating a match condition. On the off chance that there is a look for rationale 0 i.e. SL = 0 and SL = 2, T9 is ON and T10 is OFF, which pulls up Vz to rationale 2, subsequently T11 is ON which makes a association amongst ML and ground to indicate a mismatch condition. For the situation when rationale 1 is stored (Q = Q = 0.45 V), Vz is energized to 0.45 V through T9 on the off chance that SL = 0 (and SL = 2) or through T10 if the SL = 2 (and SL = 0) or through both T9 and T10 if SL= 1 (and SL = 1). In either condition, T11 is OFF because of high limit voltage and thus ML is disconnected from ground and the stored rationale 1 dependably demonstrates a match despite the hunt esteem. Presently, when there is a look for rationale 1, both T9 and T10 are ON. For this situation, Vz sets at 64mV when Q = 0 (and Q = 2) or Q = 2 (and Q = 0), due to voltage struggle amongst T9 and T10. This estimation of Vz kills T11 and in this way ML is disconnected from ground, paying little mind to the stored esteem. In this way, the proposed cell appears coordinate for both nearby and worldwide masking.

6.3 Results and Discussion

In this segment, CNTFET-based CAM cells are examined and assessed using Synopsis HSPICE test system with 32nm Stanford CNTFET model of [117] which considers down to earth non-idealities of CNTFET. Points of interest of the Stanford demonstrate have been given in segment 2.2 of section 2. So as to look at the execution of the proposed designs, CAM cells presented in [250] are imitated and recreated. For reasonable correlations, equal number of CNTs is utilized as a part of CNTFETs of all cells while keeping a similar transistor estimate proportions.

Reenactment Setup

To detect ML during CAM scan operation for generation of match result, current race sensing plan is utilized and appeared in Figure 6.4 [232]. Before a pursuit operation, ML is precharged to low and MLPRE signal is turned ON. As a consequence, transistor T5 is killed and transistor T4

is turned ON, and hub M_SENSE is precharged to high which bodes well enhancer yield MLSO to low. In the meantime, seek lines of memory are set to their new data esteems and thus there is just a single ML/SL pre charge stage. In the assessment stage, MLPRE signal is killed and EN signal is declared to low, which turns ON transistor T2 and interfaces ML to the present source actualized using a one-sided transistor T1. Since ML is disconnected from ground under a match case, it energizes at a higher rate contrasted with a ML having no less than one mismatch. Once the voltage at ML rises over the limit voltage of transistor T5 (sense enhancer), M_SENSE is released to ground and MLSO is locked to high esteem indicating a match. After that EN is changed to a high esteem which kills T2, and disconnects the present source from ML.

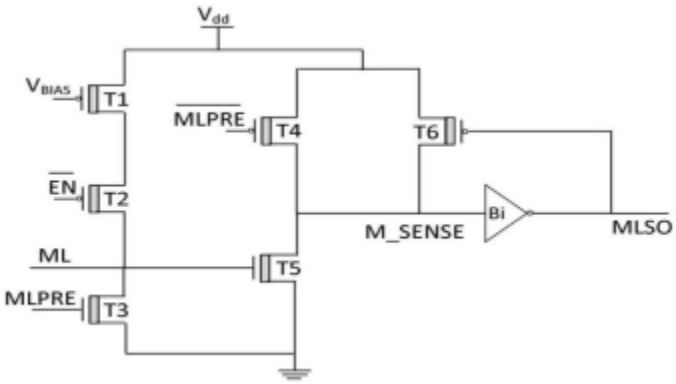


Figure 6.4: Schematic diagram for current race sensing scheme

A current race sensing plan spares power in two ways. To start with, it kills the current when ML achieves the edge voltage of T5 and subsequently, limits the voltage swing of all MLs to roughly 50% of Vd_d (0.45 V). Along these lines, it decreases the ML power dissipation by a factor of two in correlation with that of full swing ML sensing plan. Also, during precharging of ML to ground, seek lines don't should be reset between back to back looks, consequently minimizing SL switching action, a current race sensing plan diminishes SL power dissipation by a factor of two.

For structure of current sensing plan, the chirality vector of (19, 0) is utilized for all transistors with three tubes. V_{BIAS} signal is set to 0.58 V which creates a current of 10 µA in T1 to guarantee that the most extreme voltage on ML if there should arise an occurrence of any mismatch ought to be much littler than the limit voltage of T5.

Every transient reenactment are performed at room temperature with 0.9 V power supply voltage. These recreations have been performed on a 1 × 20 memory exhibit for getting a sensible capacitive loading at ML. The match delay is measured from the time when the ML begins charging till it is hooked by the sense speaker. For normal power, power is measured for each operation.

Functional Verification of CAM Cells

Figure 6.5 shows recreated transient waveform of 11T-3CAM cell for the distinctive hunt data. The main waveform demonstrates a MLPRE signal which goes high to precharge ML and low to assess ML, and rehashes for three cycles. The second and third waveforms represent EN and SL individually. The remaining waveforms demonstrate ML and MLSO for various stored Q values.

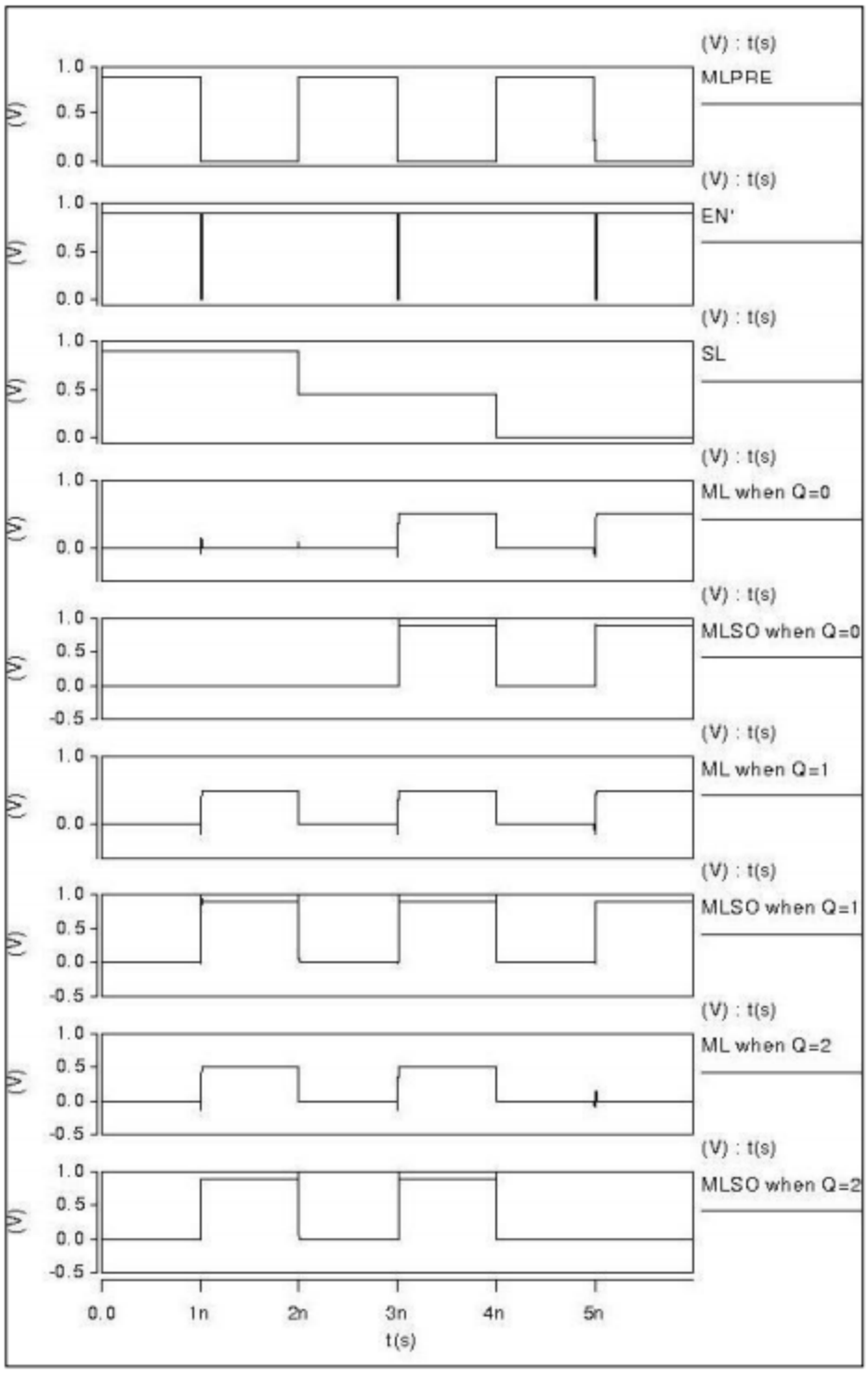


Figure 6.5: Transient waveform of 11T three-valued CAM (3CAM) cell

In the primary hunt assessment cycle when SL = 2 and MLPRE is low, ML and MLSO appear high for Q = 2 and Q = 1, and low for Q = 0, indicating match and mismatch conditions, individually. So also, in the third inquiry assessment cycle when SL = 0 and MLPRE is low, ML and MLSO demonstrate low for Q = 2, and high for Q = 1 and Q = 0, indicating mismatch and coordinate conditions individually. In the second pursuit assessment cycle, when MLPRE is low and SL = 1, ML and MLSO demonstrate high to indicate dependably a match independently of Q, which confirm worldwide masking. Correspondingly, when Q = 1, ML and MLSO demonstrate high indicating dependably a coordinate independently of SL, which check nearby masking. Subsequently, the recreated waveform confirms revise functionally of 11T-3CAM. So also, the reproduced transient waveforms of 9T BCAM and 16T TCAM cells included in Appendix, confirms their right functionality.

Simulation Results

Correlation of the CNTFET-based CAM cells is appeared in Table 6.2. Since coordinate delay is specifically proportional to ML capacitance, lower ML capacitance of proposed designs prompts rapid match operation. 9T-BCAM achieves diminishment in coordinate delay by 74% with 6% saving in power and 10% saving in gadget count contrasted with that of BCAM of [250]. So also, 16T TCAM indicates 73% diminishment in coordinate delay with practically identical power execution than its counterpart.

Table 6.2 Comparison of CNTFET-based CAM cells

Memory Cells	Match Delay ($\times 10^{-11}$ S)	Power consumption ($\times 10^{-6}$W)	Transistor Count
9T BCAM **(proposed)**	0.61	3.34	9
BCAM of [250]	2.41	3.57	10
16T TCAM **(proposed)**	0.60	4.34	16
TCAM of [250]	2.22	4.35	16
11T-3CAM **(proposed)**	0.69	8.8	11
3CAM of [250]	1.95	8.9	12

Since 3CAM cell has an indistinguishable convenience from the TCAM cell, 11T-3CAM is contrasted and TCAM cells additionally alongside existing 3CAM cells. Contrasted with 3CAM 11T-3CAM gets reduction in coordinate delay and transistor count by 64% and 8%, individually, without any misfortune in power execution. Albeit 11T-3CAM has high power utilization than that of TCAM because of voltage conflict happens between the storage of rationale 1 and rationale 0 (or rationale 2), it achieves 69% reduction in coordinate delay and 31% reduction in transistor count. Further, to determine the stability of proposed cell, we quantified the minimum noise voltage present at each of the storage nodes in 3CAM that would flip the condition of the cell by using the technique. The storage cell of proposed 3CAM cell achieves a read margin of 0.12 V and a compose margin of 0.22 V, separately.

6.4 Conclusion

This section has presented design of rapid CAM cells in CNTFET innovation. BCAM and TCAM cells have been designed in light of low capacitance seek rationale. BCAM gives storing and searching of two rationale esteems: 0 and 2, while TCAM give an additional adaptability of example matching with the utilization of couldn't care less (X). Another 3CAM cell has too been produced. 3CAM cell stores three rationale esteems: 0, 1 and 2 in a single ternary SRAM cell and eliminates the requirement for a moment binary SRAM ordinarily utilized as a part of TCAM construction. The proposed 3CAM cell utilizes CNTFETs with two diverse edge voltages (0.289 V and 0.55 V) in implementation of low capacitance look arrange. HSPICE Simulation comes about have affirmed that all presented CAM cells play out the right functionality during the read, compose and seek operations. Contrasted with existing CNTFET-based counterpart, BCAM cell achieves reduction in coordinate delay by 74% with 6% saving in power and 10% saving in gadget count. So also, TCAM indicates 73% reduction in coordinate delay with same gadget count and comparable power execution. 3CAM cell gets reduction in coordinate delay and transistor count by 64% and 8%, individually, without any misfortune in power execution. Subsequently, the watched comes about uncover that the presented CAM cells are proficient to improve the execution of memory systems.

Chapter 7

Conclusion and Future Work

7.1. Conclusion

CNTFET is a promising alternative to the traditional Si MOSFET for superior and low power VLSI circuit. CNTFET demonstrates elegant relationship with ternary rationale. Specifically, the most ideal approach to design ternary circuit is the different limit strategy, and wanted edge voltage can be achieved by utilizing diverse distance across of CNT in CNTFET gadget. Extra, ternary rationale decreases chip region and additionally the many-sided quality of interconnects with increasing their information substance. Further, math and rationale unit (ALU) is the most essential and vital part of processor in a computerized PC. Current PC needs effective implementation of ALU as far as hardware for increased estimation of integration density, speed for high throughput and colossally increased capacities, and power for compact and portable applications. Next, content addressable memory (CAM) is an application particular memory which performs parallel data correlation with data storage. CAM is mainly prominent for realizing organize applications which require a great deal of quick CAM cells to get rapid look-into operation in bigger routing tables. In this proposition, effective ternary ALU (TALU) and fast CAM cell have been produced using CNTFETs.

Design of a 2-bit hardware upgraded TALU (HO-TALU) has been presented in section 3. HOTALU has another viper subtractor (AS) module which performs both expansion and subtraction operations using a snake module just with the assistance of multiplexers. In this way, it eliminates a subtractor module from the conventional design. HO-TALU minimizes ternary function articulations and uses binary gates alongside ternary gates in realization of functional modules: AS, multiplier, comparator and exclusive-OR. As a consequence, the sub-pieces of AS: HAS and FAS utilize about 76% and 82% less transistors, separately, than conventional designs which contain isolate viper and subtractor squares. Multiplier, comparator and exclusive-OR show reduction in gadget count by 64%, 82% and 76%, separately, with deference to their existing counterparts.

Results obtained from HSPICE test system with Stanford model of 32nm CNTFET, have appeared that all HO-TALU modules achieve incredible change (almost two hundred times) in powerdelay item (PDP) as for their CMOS-based counterpart, which checks the potential advantage of CNTFET circuits. In examination with existing CNTFET-based designs, proposed multiplier, comparator and exclusive-OR get reduction in PDP by 75%, 65% and 28%, separately. Be that as it may, PDP of sub-modules HAS and FAS has marginally increased by 2% and 5%, individually. Hence, all HO-TALU modules achieve great hardware effectiveness with a minor misfortune of PDP for expansion and subtraction operations just, regarding CNTFET circuits accessible in the writing. Additionally, design of 2-bit HO-TALU is reached out to build up a 2-bit HO-TALU cut which could be effortlessly cascaded to develop a N-bit HO-TALU.

Ternary full viper (TFA) which is a fundamental sub-piece of AS has been changed using extraordinary circuit methods to enhance their effectiveness as far as PDP, and presented in section 4. Three new designs of TFA have been created. The primary TFA named as HS-TFA contains a symmetric draw up and pull-down systems alongside a resistive voltage divider as its integral part, which is designed using transistors. Contrasted with most vitality productive TFA accessible in writing, HS-TFA has high driving capability and gets reduction in delay by 9% yet, it indicates high power dissipation. The second TFA named as low power TFA (LP-TFA) has been produced using complimentary pass transistors rationale style. This LP-TFA demonstrates reduction in power by 24% with change in PDP by 5%, however it has 20% more delay. The third TFA named as unique TFA (DTFA) has been executed in view of dynamic rationale, which utilizes a ternary attendant to repay charge misfortune because of charge sharing issue. DTFA has high driving capability and achieves reduction in power, delay and PDP by 24%, 15% and 35%, individually. Be that as it may, it needs CNTFET gadgets with littler distance across (0.626 nm) furthermore so as to decrease charge spillage. Every one of the three TFAs have been designed in light of inherent binary nature (0 and 1) of input convey, which prompts decreased gadget count in designs.

Further, new design of 1-bit comparator has been produced using pass transistor rationale with diminished number of stages in basic delay way. This design has been utilized to make 2-bit and

N-bit comparator where a static binary tree design has been used to amend the voltage levels. The proposed 2-bit comparator has high driving capability and achieves 29% reduction in PDP with 34% less gadget count contrasted with that of its counterpart accessible in writing. In any case, it has two yield signals to check more prominent, lesser and break even with conditions, which make the decoding rationale of comparator reaction complex in those applications where three yields (one for each condition) are craved. Aside from these, all new TFAs and 2-bit comparator indicate less weakness to voltage and temperature varieties as for existing designs.

Design of a 2-bit power enhanced TALU (PO-TALU) has been presented in part 5. 2-bit PO-TALU functional modules: viper subtractor-exclusive-OR (ASE) and multiplier have been designed using new complementary CNTFET-based binary computational unit and a low many-sided quality encoder. ASE eliminates an exclusive-OR module and subtractor module from the conventional engineering. Multiplier utilizes another productive square named as convey include (CA) hinder set up of THA.

In examination with existing vitality productive CNTFET-based designs, HSPICE reenactment comes about have demonstrated that the sub-squares of ASE: half snake subtractor-exclusive-OR (HASE) and full snake subtractor-exclusive-OR (FASE) devour 66% and 47% less power. HASE demonstrates reduction in delay and gadget count by 4% and 26%, correspondingly. FASE appears 25% reduction in gadget count however it has 29% more delay. Sub-piece of multiplier module: 1-bit multiplier demonstrates reduction in power, delay and gadget count by 70%, 5% and 37%, separately. ASE and multiplier are less sensitive to voltage and temperature varieties. Design of 2-bit PO-TALU has been adjusted to execute 2-bit PO-TALU cut which could be effectively cascaded to shape an N-bit PO-TALU. Subsequently, TALU designs presented in this proposal can fill in as an effective functional unit for present day ternary microprocessor with CNTFET in nanoscale time. Design of fast CAM cells has been presented in section 6. Binary CAM (BCAM) and ternary CAM (TCAM) cells have been designed in view of low capacitance seek rationale. BCAM gives storing and searching of two rationale esteems: 0 and 2, while TCAM give an included adaptability of example matching with the utilization of couldn't care less (X). Another three-esteemed CAM (3CAM) cell has additionally been created. 3CAM cell stores three rationale esteems: 0, 1 and 2 in a single ternary SRAM cell and eliminates the requirement for a moment binary SRAM commonly utilized as a part of TCAM

construction. The proposed 3CAM cell utilizes CNTFETs with two extraordinary edge voltages (0.289 V and 0.55 V) in implementation of low capacitance seek arrange.

HSPICE Simulation comes about have affirmed that all presented CAM cells play out the right functionality during the read, compose and look operations. Contrasted with existing CNTFET-based counterpart, BCAM cell achieves reduction in coordinate delay by 74% with 6% saving in power and 10% saving in gadget count. Also, TCAM indicates 73% reduction in coordinate delay with same gadget count and comparable power execution. 3CAM cell gets reduction in coordinate delay and transistor count by 64% and 8%, individually, without any misfortune in power execution. Subsequently, the watched comes about uncover that the presented CAM cells are fit to improve the execution of memory systems.

7.2 Future Scope of Work

CNTFET with ballistic transport operation, incredible warm conductivity and high present driving capability, is ended up being a promising alternative to the conventional Si-MOSFET. The design space of CNTFET-based computerized circuit and memory circuit can be conveyed forward for improvement of very productive current electronics. All CNTFET-based TALU designs presented in this proposition perform nine ternary operations. It would be interesting to expand these designs for an increased number of ternary operations with alteration in function select rationale, decoder and functional modules. Along these lines, the presented work can be utilized to design ternary microprocessors with CNTFETs. Moreover, functional modules of TALU, for example, AS and multiplier and so forth are the building squares of numerous different applications including video and picture processing and DSP designs. It is conceivable to explore the utilization of TALU functional modules in effective realization of these applications. A quick and compact 3CAM cell designed using CNTFETs, has been appeared in section 6. This cell has twice power utilization contrasted with that of conventional TCAM cell due to voltage conflict happened between the storage of rationale 1 and rationale 0 (or rationale 2); in this mannerinterchange courses should be found to decrease this. Further, it is conceivable to explore other circuit component of CAM design, for example, sense speaker and match line precharge control circuit by utilizing CNTFETs for ongoing applications like interactive media data transmission. Aside from circuit design domain, it is interesting to explore techniques for format arrangement of presented designs.

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