Journal Homepage: - www.journalijar.com
INTERNATIONAL JOURNAL OF ADVANCED RESEARCH (IJAR)
Article DOI: 10.21474/IJAR01
DOI URL: http://dx.doi.org/10.21474/IJAR01

RESEARCH ARTICLE

National Conference on Innovation in Science, Engineering and Management (NCISEM-2022)
Date of Conference 11-12 March 2022

AN EFFICIENT LOW POWER DESIGN OF SAR BASED ADC USING DEEP SUBMICRON 45NM CMOS TECHNOLOGY

Monu Raju Thool[1], Dr. Girish D. Korde[2] and Prof. Anant W. Hinganikar[3]

1. Research Scholar, VLSI, Department of Electronics & Telecommunication Engineering, Bapurao Deshmukh College of Engineering, Sewagram, Wardha (M.S.).
2. Assistant Professor, Dr. Girish D. Korde, Department of Electronics & Telecommunication, Bapurao DeshmukhCollege of Engineering, Sewagram, Wardha (M.S.).
3. Assistant Professor, Anant W. Hinganikar, Department of Electronics & Telecommunication, Bapurao Deshmukh College of Engineering, Sewagram, Wardha (M.S).

Manuscript Info

Key words:-
ADC, SAR, CMOS Technology, Low Power, Comparator, Digital-To- Analog Converter, Sample-And- Hold, Etc.

Abstract

A 4-bit Successive Approximation Register (SAR) logic based Analog to Digital Converter (ADC) is designed using Up-down counter as SAR logic for low power operation. The advancement in CMOS technology is going on day by day. With this advancement, more & more signal processing functions are incorporated in the digital field for low cost, low power consumption and dissipation. The designed CMOS based ADC structures provide optimum results for all three circuit design challenges as speed, area and power. Among various ADC topologies, we opted to implement up-down counter based Successive Approximation Register (SAR) ADC that is one of the best suited for low power. We target a resolution of 4-bit and a power consumption of few mill watts. The SAR ADC is implemented in 45nm CMOS technology with a power supply of 1V.

Introduction:-

In the past few years, more and more applications are built with very stringent requirements on power consumption [1]. For electronic systems, such as wireless systems or implantable devices, the power consumption is becoming oneof the most critical factors [1]. The stringent requirements on the energy consumption increase the needfor the development of low voltage and low power circuit techniques and system building blocks [2]. Along with thesame, the trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area. VLSI fabrication technology is leading to smaller line widths and feature size and hence to higherpacking density [2].

The scaling down of feature size by the various factors leads to improved performance.Hence, it is important to understand the effects of scaling [2].

Corresponding Author:- Monu Raju Thool
Address:- Research Scholar, VLSI, Department of Electronics & Telecommunication Engineering, Bapurao DeshmukhCollege of Engineering, Sewagram, Wardha (M.S.).

Analog-to-Digital Converters (ADCs) translate the analog quantities into digital language, used in information processing, computing, data transmission and control systems [3]. ADCs are key components for the design of power limited systems, in order to keep the power consumption as low as possible [2].

There is a wide variety of different ADC topologies available depending on the requirements of the application [4][8]. SAR ADCs have a decent conversion speed and take small overall chip area in comparison to flash ADCs, which are fast but take up a large area. SAR ADC design also flows well with the use of a serial output port due to the natureofthe conversion method [4] [5].

In a SAR- ADC, a digital-to-analog converter (internal-DAC) tries to calculate the value of each sample of the input analog signal through successive approximations and comparisons. Based on the ADC resolution, after a specific number of cycles, the digital word being stored in the successive-approximation register (SAR) corresponds to the analog sample with a specific quantization error [5]. It basically generates one bit per clock cycle, the merits are the low area needed for the implementation. ADCs of this type have good resolutions and quite wide ranges.

The up-down counter based SAR architecture allows for high-speed, typically low-power ADCs to be packaged insmall form factors for today's high demanding applications. With Microwind EDA Software tool, we have designed 4bit low power SAR ADC with 45 nm technology.

SAR ADC:-

The SAR-ADC consists of a sample-and-hold (S/H) circuit, a comparator, a digital-to-analog converter (DAC) and logic control unit. These blocks are explained below. The ADC employs a binary-search algorithm that uses the digital logic circuitry to determine the value of each bit in a successive manner based on the outcome of the comparison between the outputs of the S/H circuit and DAC feedback [1][2][3]. When an input signal is applied to the converter, the comparator simply tells whether the input signal is greater or smaller than the DAC output and gives one digital bit at a time starting from the MSB. The SAR stores the produced digital bit and uses the information to alter the DAC output for the next comparison. This operation is repeated until all the bits in the DAC are decided. Figure 1 and 2 illustrates the block diagram and conversion procedure of converter.

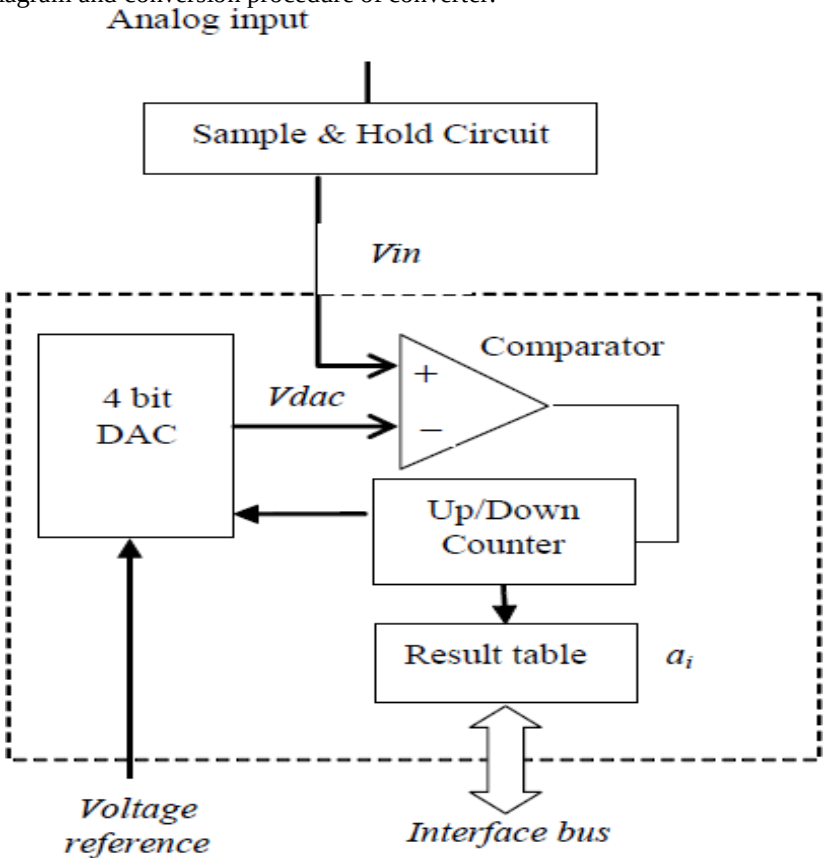

Figure 1:- Block diagram for the Successive approximation Register based ADC.

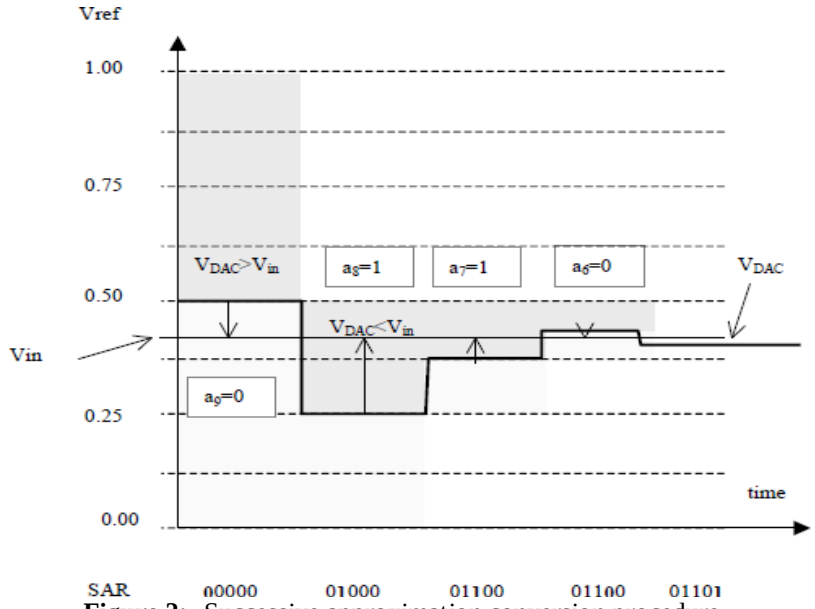

Figure 2:- Successive approximation conversion procedure.

Sample and Hold Circuit

The conversion process of a successive approximation ADC begins at the Sample and Hold circuit. Figure 3 shows the Sample and Hold circuit. Mostly, Sample and hold circuit contains a switch and a capacitor. In the tracking mode,while the sampling signal is high and the switch is connected, it tracks down the analog input signal. In hold mode, itholds thevalue when the sampling signal changes to low [4]. The value of Cstore is dependent on the number of voltage levels to be observed on the output side.

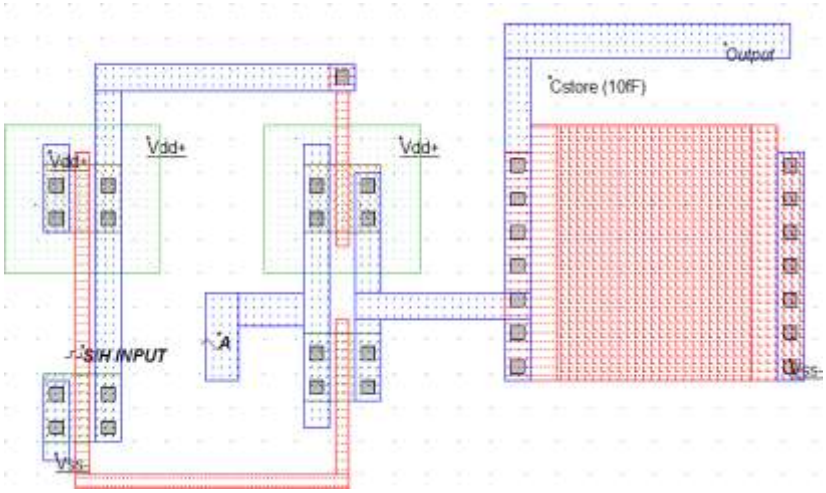

Figure 3:- Physical design of Sample and Hold Circuit.

Comparator

Comparator is the important block of any ADC, It can be said that comparators are fundamental analog to digital converter used to generate one bit of digital data [4] [2]. To optimize the performance of comparator on the basis ofhigh speed, resolution and power dissipation W and L of the used transistors must be taken into consideration. The aspect ratio of this transistor can be calculated by equation given below;

IDS= $K + \frac{W}{L}\left(VGS - VTH - \frac{VDS}{2}\right)VDS$

Where, VDD = Supply Voltage, VT = Threshold Voltage, VGS = Gate Sourse Voltage,

K and

$= un\ COX$

$$gm = \frac{K}{2}\frac{W}{L}(VGS - VTH)$$

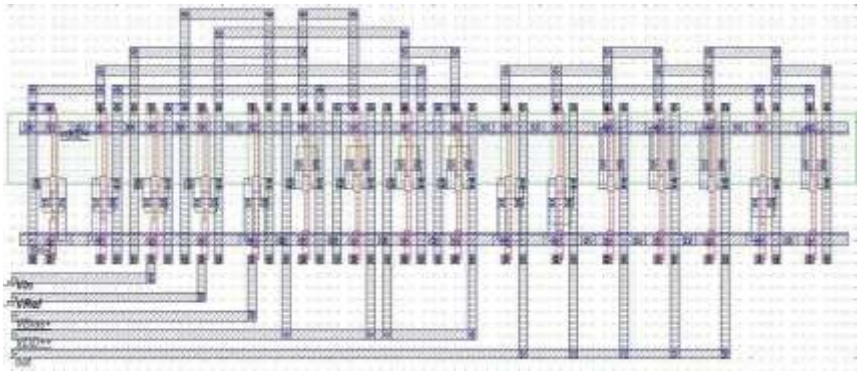

Figure 4:- Physical layout High speed comparator.

Up-Down Counter based SAR Logic Design

The architecture of SAR conversional ADC is shown in Figure.5. A successive approximation register sub block is designed to provide an approximate digital code of Vin to the internal DAC [1] [3]. We proposed a design of SAR counter logic by simplest method, an Up-Down counter to control DAC o/p. It works by starting by binary o/p 8(1000), and then by determining whether Vin is larger or smaller than VDD/2, it decrements or increments. The counter o/p and Vin is compared using comparator which gives the value of that count directly. The comparison is performed for the next count, and so on until all count are checked for below or greater than value 8. The conversion would start with SOC signal and cycle finishes after 8 clock cycles, with active low EOC output.

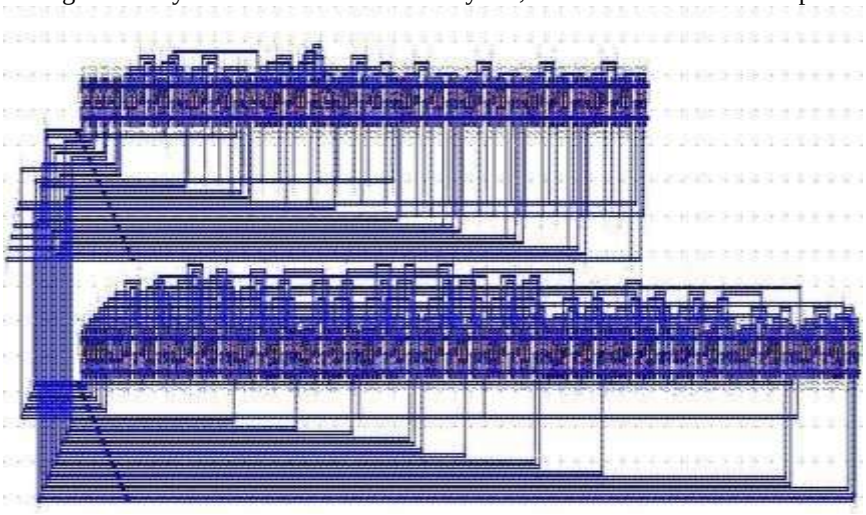

Figure 5:- Physical design of SAR Logic.

Digital To Analog Converter (DAC)

DAC can be implemented using various architectures with varying level of complexity. Each of DAC architecture hasits own merits or demerits. Voltage division methods can be used to convert digital code to analog value. R-2R ladder architecture has two operating modes: current mode R-2R ladder and voltage mode R-2R ladder [10]. In this paper, voltage mode R-2R ladder type DAC is used, shown in figure 6.

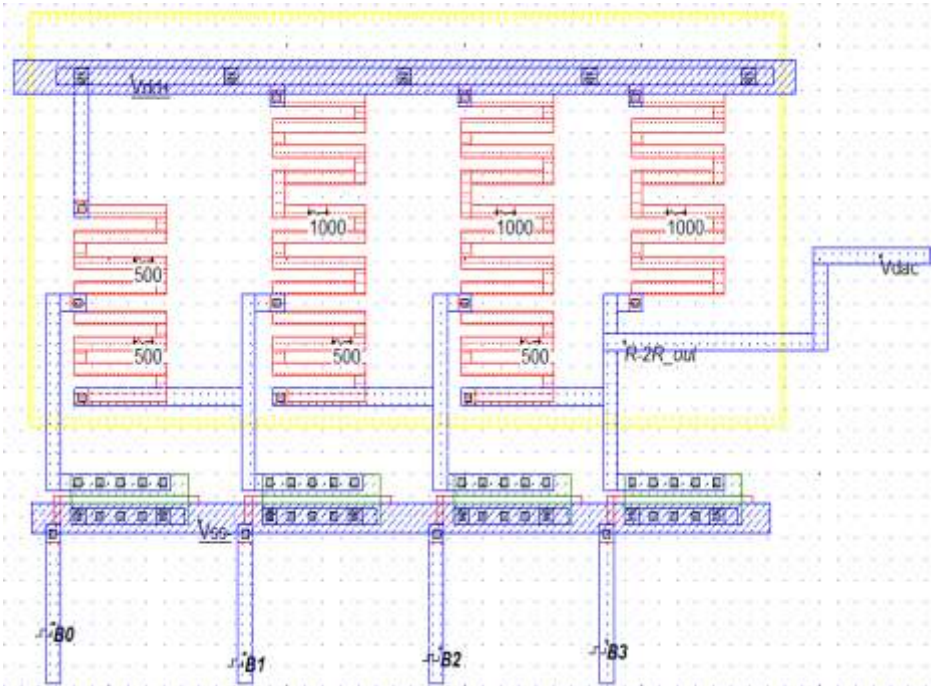

Figure 6:- Physical design of R-2R based DAC.

ADC Design:-

After implementing all the subparts of ADC as sample and hold circuit, comparator, Up-Down based SAR structure and DAC. We need to insert them all on the single substrate. The Figure 7 shows the final physical design of 4 bit CMOS SAR ADC

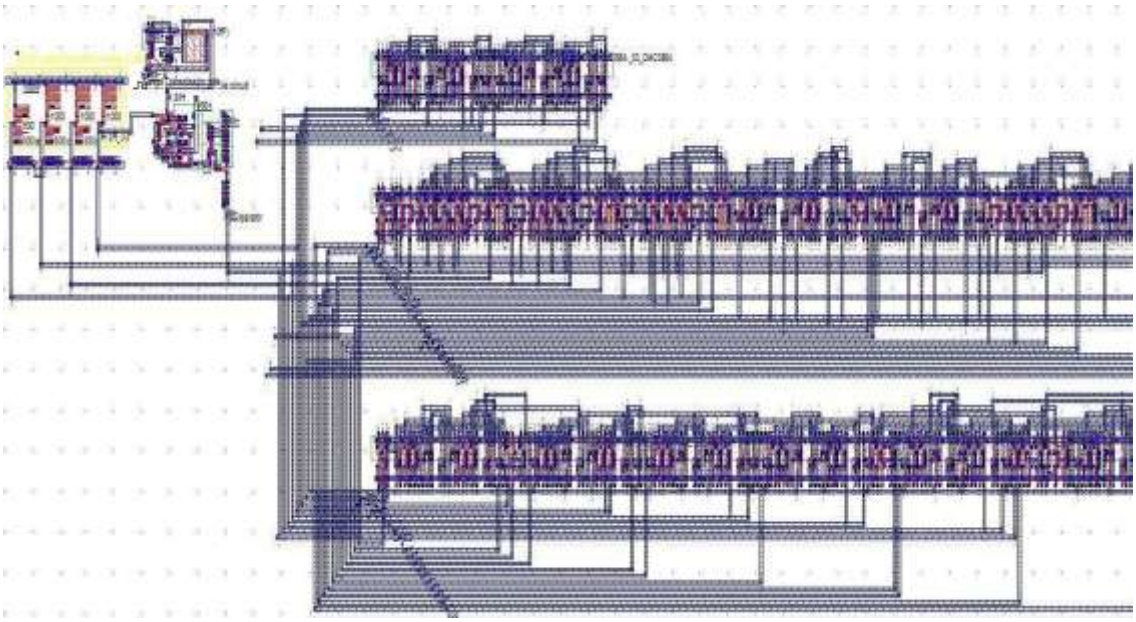

Figure 7:- Physical design Final ADC.

Simulation Result:-

After simulation the output waveforms of sample and hold circuit, comparator, Up-Down based SARstructure and DAC are shown in figures below.

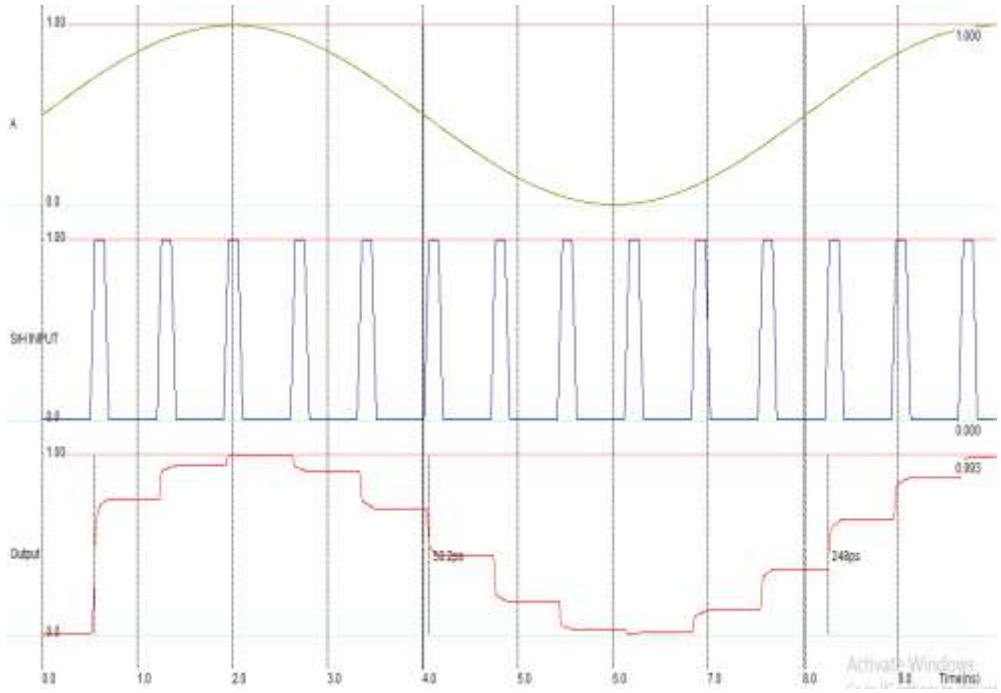

Figure 8:- Transient Response of Sample and Hold circuit.

For Comparator, the simulation result of comparator is given in Figure 9, where VRef is input with some delayed clock timing parameters, Vin is random clock between 0.1V to 0.9V and Vbias is a biasing voltage as 0.5 V. When the input Vin goes high above 0.5 V, the output of the buffer changes states. So the relation for output we are getting is, when Vref > Vin then out = '1' and when Vref < Vin, out = '0'.

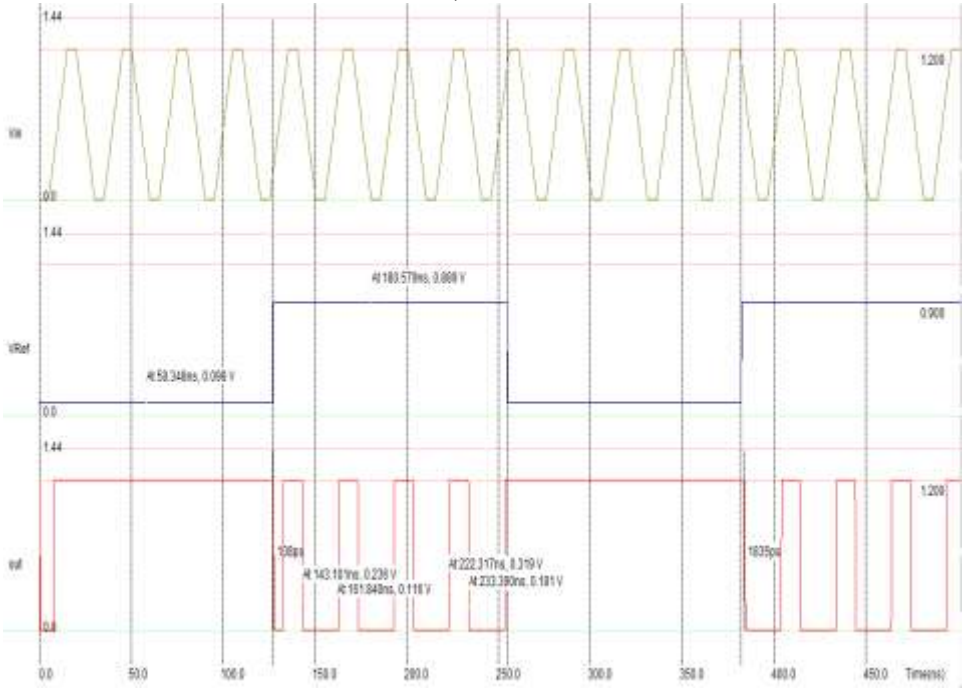

Figure 9:- Transient Response of Comparator.

For the DC analysis, both input and reference voltage are taken as DC voltage source. Input voltage is swept from0Vto 1 V.

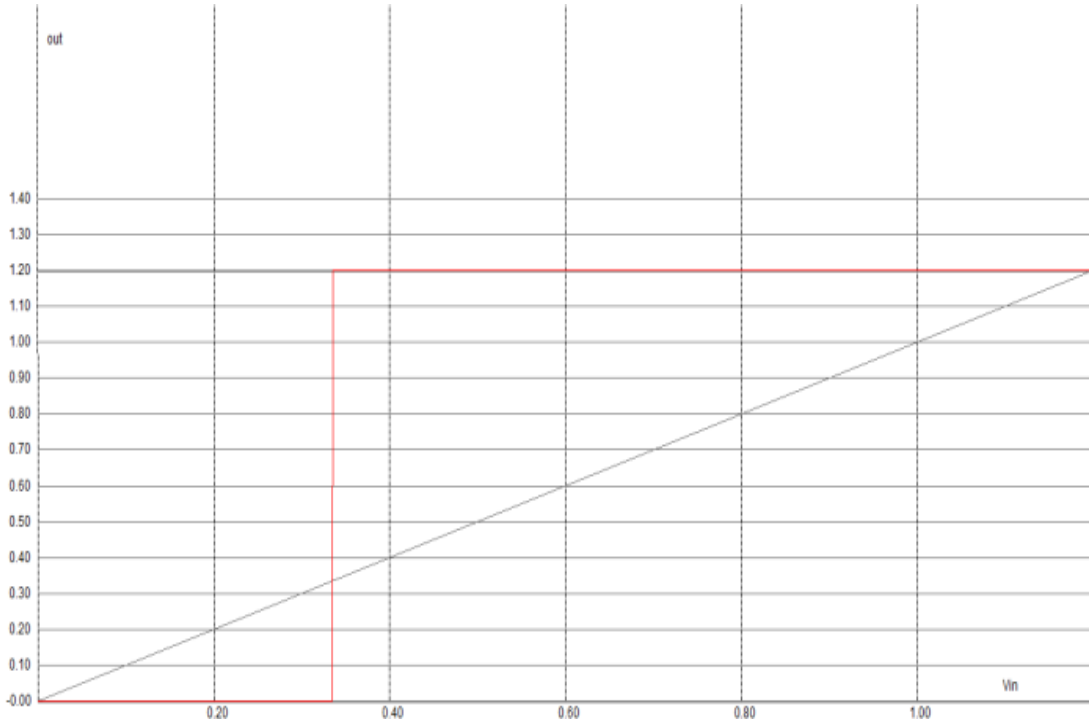

Figure 10:- DC Transfer Response of Comparator.

For R-2R ladder DAC, designed with 45 nm technology and the input given to this converter is from 0000 to 1111. We have achieve simulation result for all 16 combinations of input for 0100 (B3, B2, B1, B0) and 1000 (B3, B2, B1,B0).

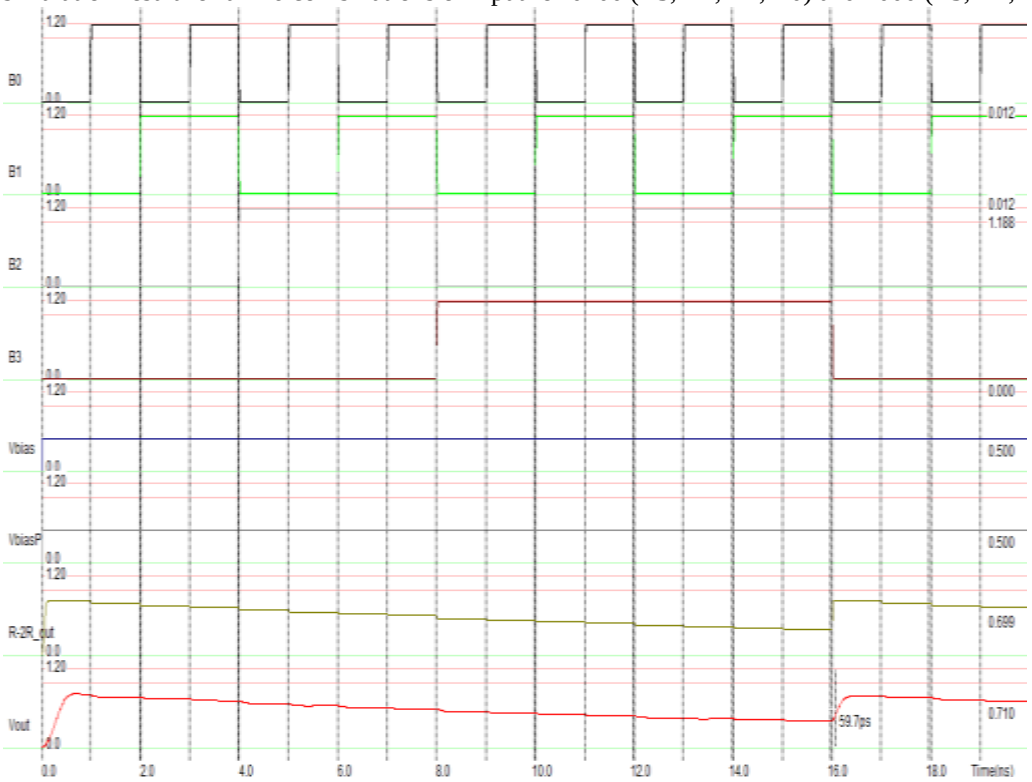

Figure 11:- Simulation Results of R2R Based DAC.

For ADC design simulation, the input Analog Input as a sine waveform.

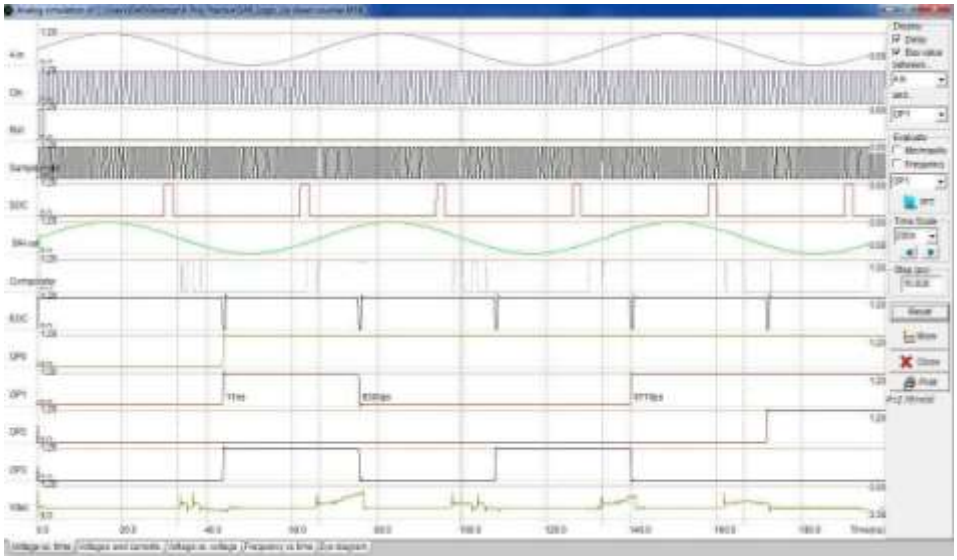

Figure 12:- Simulation result of SAR Based DAC.

Comparison Performance Of SAR ADC:-

Specification	[2]	[5]	**This Work**
Technology Used	45nm	45nm	**45 nm**
Architecture	SAR	SAR	**SAR**
Resolution (bits)	4 bits	4 Bits	**4 Bits**
Supply Voltage (Volts)	1	1	**1**
Power Consumption (mW)	2.7	4	**2.20**

Conclusion:-

A physical design of 4-bit successive approximation Register ADC converter suitable for operation at low supply voltage is designed in a standard 45 nm CMOS technology and compared based on the power dissipation. The physicaldesign for various internal parts are designed and combined to form a CMOS based ADC. On the input side, we designed Sample and Hold circuit with input as an analog signal. We have designed a high speed CMOS comparator circuit where the input voltage is swept from 0V to 1 V as Vdd for 45nm technology is 1V. An area efficient DAC architecture based on the R-2R ladder topology is designed. The Results indicate that the physical design achieves 4- bit conversion. Test results indicate that the circuit is well suited for operation at 1 V. The SAR ADC draws a smallamount of power 2.20 mW and physical area of 829.6µm2.

References:-

1. Devitha P.S, Anuja George "DESIGN OF LOW POWER HIGH-SPEED SAR ADC-A REVIEW" Third International Conference on Computing Methodologies and Communication (ICCMC 2019) IEEE Xplore Part Number: CFP19K25-ART; ISBN: 978-1-5386-7808-4
2. Prof. Chandrakant S. Ragit, Dr. Sanjay Badjate "Design of Up – Down Counter as SAR Logic for High Speed SAR ADC used in Health Care System" 2016 Conference on Advances in Signal Processing (CASP), June 9-11, 2016
3. Rajesh Mehra Mehmood ul Hassa, “Design analysis of 1-bit cmos comparator” International Journal of Scientic Research Engineering Technology, 2015.
4. Manish Singhal, Murari Kumar, “Review paper on minimization of power dissipation, area and set voltage in cmosdynamic comparator for high speed adcs” International Journal of Modern Computer Science (IJMCS), 2014.
5. Nilofar M. A. Shaikh, Prof. Seema H. Rajput, "Design of SAR Logic for Low Power High Speed SAR ADC", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (An ISO 3297: 2007 Certified Organization) Vol. 5, Issue 1, January 2016
6. Mr. A.R. Kasetwar, Miss. V. G. Nasre "Design of low power and high speed components of SAR ADC",
7. International journal of Advances in Electronics Engineering Vol:1 Issue:1 ISSN 2278

8. Babita Diana K and D. Jackuline Moni, “An ultra-low power 8 bit SAR adc suitable for wireless medical applications” International Conference on Communication and Signal Processing IEEE, 2014.
9. Zhangming Zhu, Member, Zheng Qiu, Maliang Liu, and Ruixue Ding,"A 6-to-10-Bit 0.5 V-to-0.9 V Reconfigurable 2 MS/s Power Scalable SAR ADC in 0.18 CMOS", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS.
10. Mon Mon Thin, Myo Min Than, and Theingi Myint,"Enhancement of SAR Algorithm for Analog to Digital Converter", 2015 International Conference on Future Computational Technologies (ICFCT'2015) Singapore, March 29-30, 2015
11. Ms. Kiran P. Kokate, Prof. A. O. Vyas, "DESIGN OF CMOS BASED ADC FOR LOW POWER CONSUMPTION", International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 4, Issue 11, November 2015
12. Anuradha S. Kherde, Pritesh R. Gumble,"An Efficient Design of R-2R Digital to Analog Converter with Better Performance Parameter in (90nm) 0.09-µm CMOS Process", International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-3 Issue-7, December 2013
13. Ms. Kiran P. Kokate, Prof. A. O. Vyas,"Design of Low Power, High Speed ADC by using Submicron Technology", International Journal of Engineering Research & Technology (IJERT) Vol. 3 Issue 2, February - 2014 IJERTIJERT ISSN: 2278-018
14. Razavi “Design of sample-and-hold amplifier for high-speed low- Voltage” IEEE 1997 Custom Integrated Circuits Conference, 1997.
15. Vijay Pratap Singh, Gaurav Kumar Sharma, Aasheesh Shukla "Power Efficient SAR ADC Designed in 90 nm CMOS Technology" 2017 2nd International Conference on Telecommunication and Networks (TEL-NET 2017).