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RESEARCH ARTICLE

LOW POWER OPTIMIZATION OF FULL ADDER CIRCUIT BASED ON GDI LOGIC FOR BIOMEDICAL APPLICATIONS

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Abstract

Advanced Electronic Devices have recently become more prevalent, designers have opted for low power, quick speed, and compact designs and processes. Even though there are numerous design methodologies currently in use for VLSI system design optimization, very few design techniques produce solutions that are optimally optimal. GDI-based circuits are becoming increasingly important since they use less space, power, and energy. The GDI technique ensures minimal propagation delay, power, and area in low-power design strategies. For 45nm technology, the Cadence Virtuoso EDA tool is utilised to determine delay and power. The proposed designs' examination of delay and power performance at 1.0V voltage produced positive findings. The Gate Diffusion Input concept serves as the foundation for the proposed design in this work. In order to achieve a full voltage swing of the output, a 1-bit full adder circuit design using GDI is demonstrated in this work. The GDI with the Full Swing Technique is presented in this work. Applying the suggested way to a 45nm complete adder from 14 Transistors. It is evident from the obtained simulation results that the suggested design uses the least power and the least amount of delay when compared to other full adder circuits that are already in use. Consequently, compared to previous full adder GDI circuit designs, the output voltage swing is in full and the overall power-delay product is improved by 60 percent.

Introduction:-

The GDI cell, which has just two transistors, has a layout that is similar to that of a typical CMOS inverter. Figure 1 and 2 depicts the typical GDI logic cell. It does, however, have three inputs: G, P, and N, unlike the inverter. As illustrated in Table 1, it had been proved that a simple GDI cell can frequently implement many logic operations [1]. This is often accomplished by altering the GDI cell's input. While most of those tasks require more sophisticated implementation using conventional CMOS, employing GDI cells, the design may be completed effectively with just two transistors [2]. The most complicated function, the MUX, will be implemented more effectively with a simple GDI cell than with a CMOS implementation.

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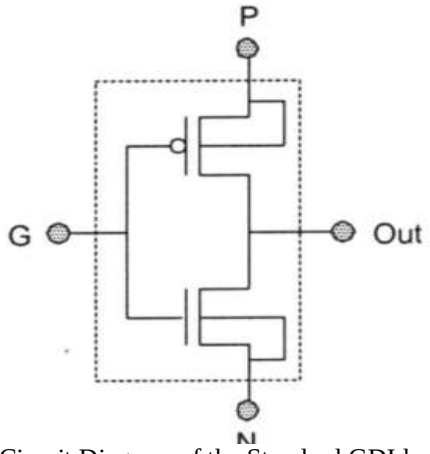

Figure 1:- Circuit Diagram of the Standard GDI logic cell.

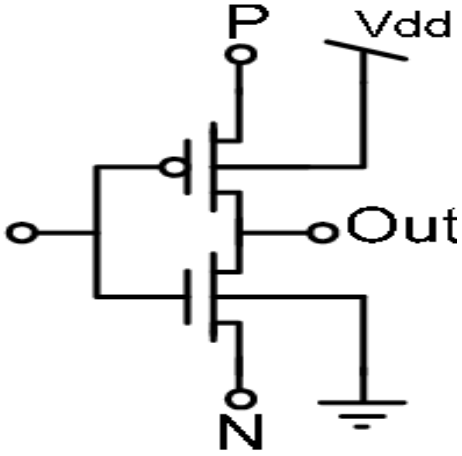

Figure 2:- Circuit Diagram of Standard Modified GDI logic.

Table 1:- Function using a GDI Standard logic cell's input configuration.

N	P	G	OUTPUT	FUNCTION
0	1	A	A’	INVERTER
0	B	A	A’B	F1
B	1	A	A’+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+A’C	MUX
B’	B	A	A’B+B’A	XOR
B	B’	A	AB+A’B’	XNOR

The Full adder is often one of many adders that make up a cascade to add binary numbers. Figure 4.1 depicts the diagrammatic representation of the total adder. It has two output signals: carry and sum. 2 Exclusive OR logic gates, 2 AND logic gates, and 1 OR logic gates will be used to create the one-bit CMOS Full Adder design's circuit schematic [3]. The Carry and Sum output expressions are

SUM=A xor B xor Cin (1)
Carry=(A and B) or (Cin and (A xor B))(2)

Entrance Diffusion Reduced threshold voltage in input gates can lead to decreased current drive, which in turn affects the functionality of the logic gate. The short circuit path power dissipation in the cascaded inverters used for the restoration of the voltage also rises as a result of these decreases. It has been demonstrated that using restoration buffers with a multiple threshold method considerably reduces these effects [4]. According to this method, all pathways where a voltage loss is anticipated should be free of higher threshold transistors. This will result in a minimal voltage loss. This combination can minimize the static power dissipation in the fundamental inverters.

The majority of CMOS universal gates are used in static-based digital designs. The solutions to this problem are known as NAND and NOR gates, each of which can do all of these tasks with just four transistors. The construction of gates like MUX, AND, and OR using the Gate Diffusion Input approach, which is incredibly efficient (Table 1), uses about the same number of transistors as the traditional CMOS method for NAND and NOR logic gates [5].

About FinFET:-

The template FinFET stands for fin field effect transistor. A non-planar dual gate or triple gate transistor called a finFET can be found in silicon architecture and has a very high computational density. FinFET was specifically designed for use with silicon on insulation. The FinFET is named after the undeniable fact that the observed FET structure appears to be a collection of fins. The wrapping of the conducting channel with a thin silicon layer "fin" is the primary distinguishing feature of the FinFET. The device's effective channel length is indicated by the fin thickness [6].

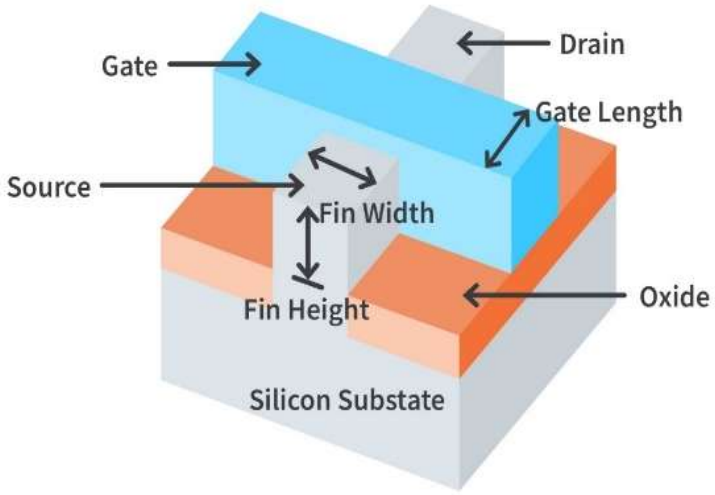

Figure 3:- Finfet Basic Structure [6].

FinFETs have a 3D structure that is positioned above the planar substrate and provides greater room than a planar gate as shown in figure 3. A thin, Fin-shaped silicon structure known as the gate electrode is employed in FinFETs to conduct channels that rise above the insulator. On a single transistor, this gate electrode is active. In contrast to a planar structure, the Fin, the best silicon substrate, integrates the Drain and Source channels in three dimensions [8]. By activating chips to accomplish more performance at a lower cost, the FinFET is an innovative transistor design that aims to solve the issues with short-channel effects that transistors encounter. FinFETs are the best choice for use in situations where increased performance and power are crucial due to a number of fundamental advantages. Some of them perform better at reducing the effects of short channels, switching quickly, increasing drain current, regulating channels, consuming less power, and lowering switching voltage [9].

Literature Survey:-

The most crucial element in the creation of all microprocessors, including digital signal processors (DSP), is the full adder. The foundation of any complicated arithmetic function is an adder. The critical route in the majority of those systems has an adder, which has an impact on the system's overall speed. Therefore, improving the one-bit full adder cell performance is very crucial [1].

The market need for conventional CMOS is decreasing daily since they are difficult to install and subject to short channel effects [2]. The implementation logic styles employed in this study are Gate Diffusion Input (GDI) Design. A complete adder based on FinFETs and using CMOS logic has been created in an effort to eliminate the Short Channel Effects [10].

The straightforward structure depicted in figure1 serves as the foundation for the Gate Diffusion Input Cell technique. First off, the simplest standard cell is similar to a CMOS inverter, however, there are also significant differences: a Standard GDI cell consists of three inputs – N, P, G [11].

Unlike a typical CMOS inverter, the bodies of NMOS and PMOS are biased because they are connected to P or N, respectively. With this design, an appropriate type of logic function can be implemented using just two transistors. By taking into account a tiny cell library, quicker, low-power circuits can be designed while utilising fewer transistors and having improved voltage level swing and static power characteristics [12].

To reduce the number of transistors, overall average power, and latency, modified GDI is used. The Modified GDI approach has the benefit of improving the circuit. The influence of technology scaling and source power may allow the Modified GDI approach to become adapted to overcome the disadvantages. Figure 2 depicts the redesigned GDI's schematic [13][14].

When GDI gates are used in the design, the threshold voltage decreases, which affects the gate's performance by reducing the current drive [15][16]. It shows that by using voltage swing-restoration buffers with a multiple V_H approach, known as MVT, to lower direct-path power consumption within the cascaded inverters used for voltage swing restoration, these impacts can be significantly decreased. In all the paths where a drop is anticipated, this technique recommends using transistors with a lower threshold. The voltage drop at the output will be as little as possible using this technique. As a result, the inverters' direct-path static power is reduced to a minimum [17][18].

Implementation:-
The results of the proposed circuit and the existing designs are simulated using the 45nm Cadence Virtuoso tool. To obtain the necessary values, proper simulations are performed for the specified complete adder circuits at a supply voltage of 1V. As illustrated below, the simulated waveforms are displayed.

Existing Circuit Design:
28 Transistor CMOS one-bit full adder circuit design
In CMOS circuit designs, NMOS and PMOS transistors are mixed together. Pull-down transistors pass a weak "0," while pull-up transistors pass a strong "1." A CMOS circuit design with various techniques was used to calculate the overall average power dissipation [19][20]. In order to get complete swing results and good driving capacities, the circuit was developed utilising 28 transistors, including both pull-down and pull-up transistors. The usage of extra transistors is the only drawback of this circuit design. Input capacitances, dynamic power, and latency all rise as a result. The picture 4 depicts the circuit.

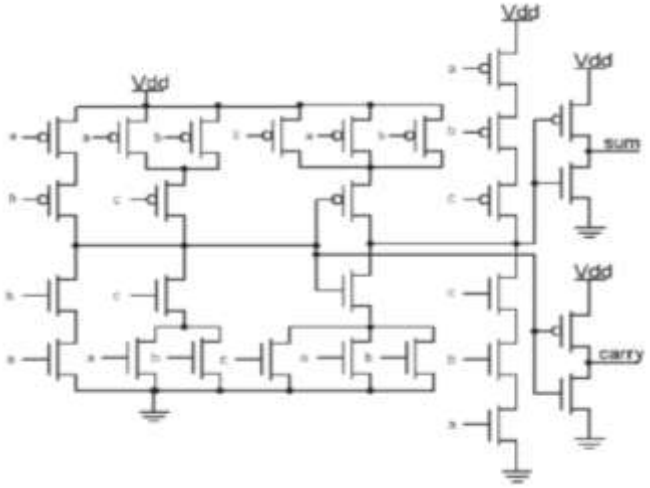

Figure 4:- Circuit Diagram of 28Transistor one bit full adder CMOS Design.

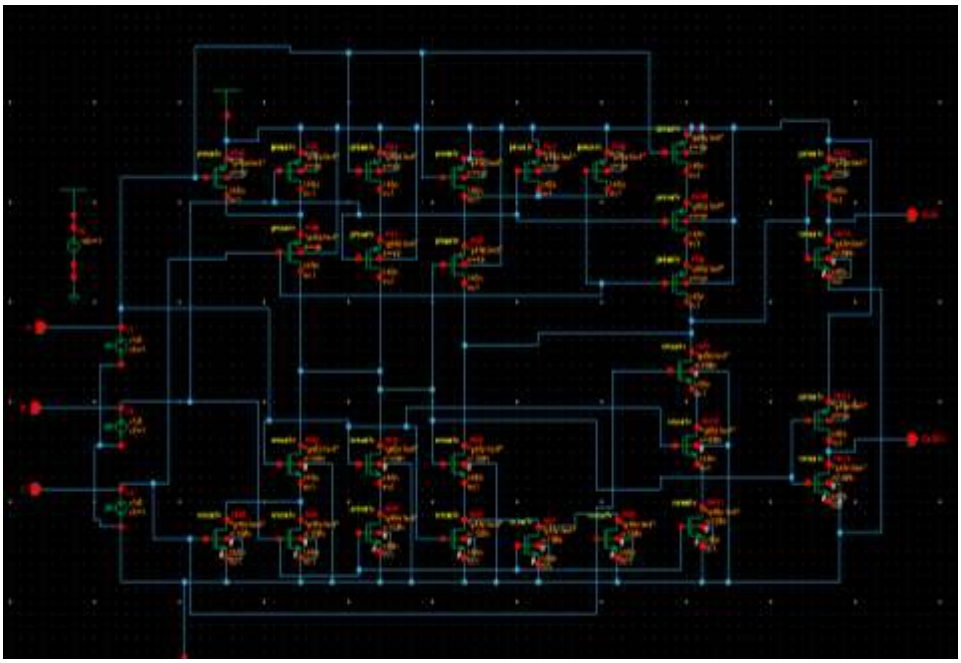

Figure 5:- Schematic of 28Transistor CMOS based Full Adder Circuit Design.

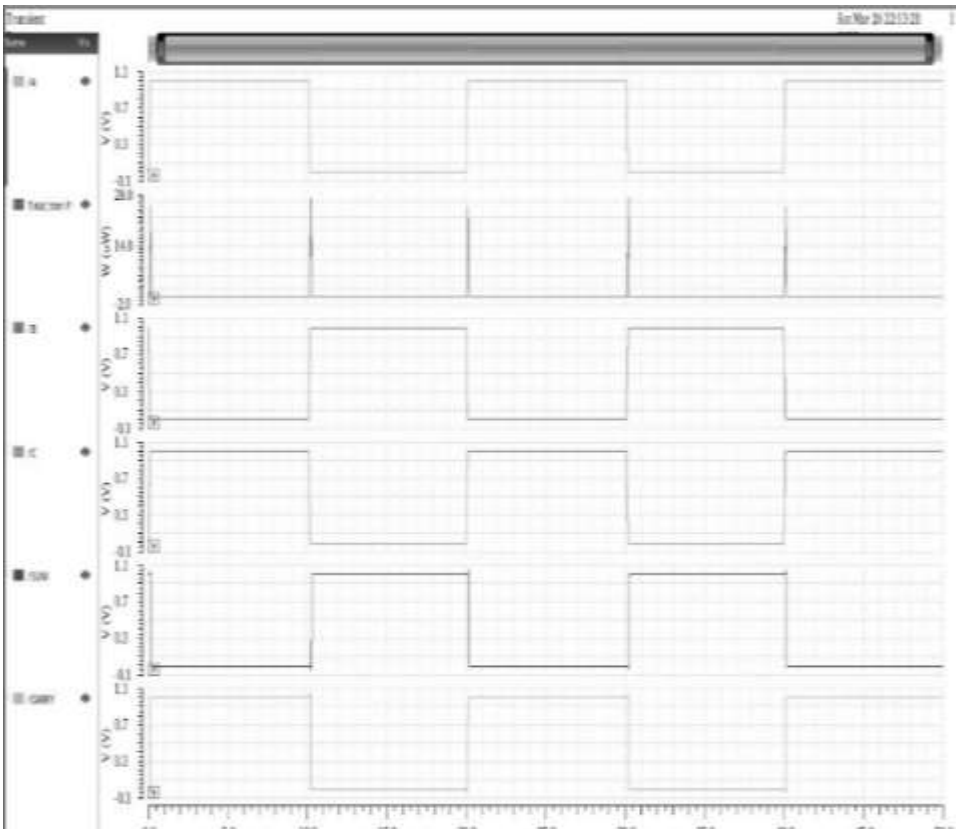

Figure 6:- Simulation waveform of 28Transistor CMOS based Full Adder Circuit Design.

28 Transistor FINFET based one-bit Full Adder Circuit Design

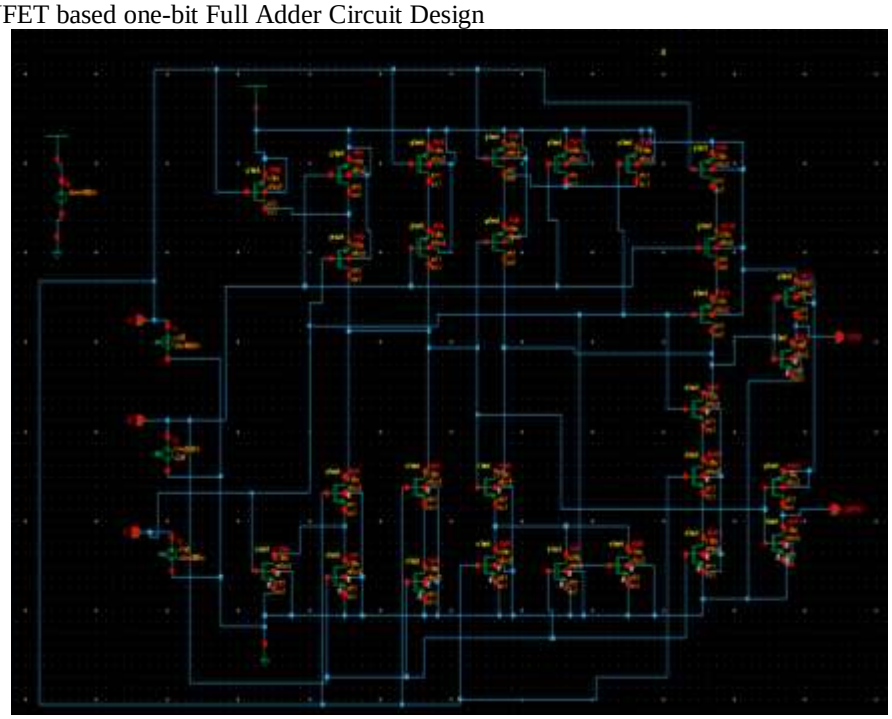

Figure 7:- Schematic of 28Transistor FINFET based Full Adder Design.

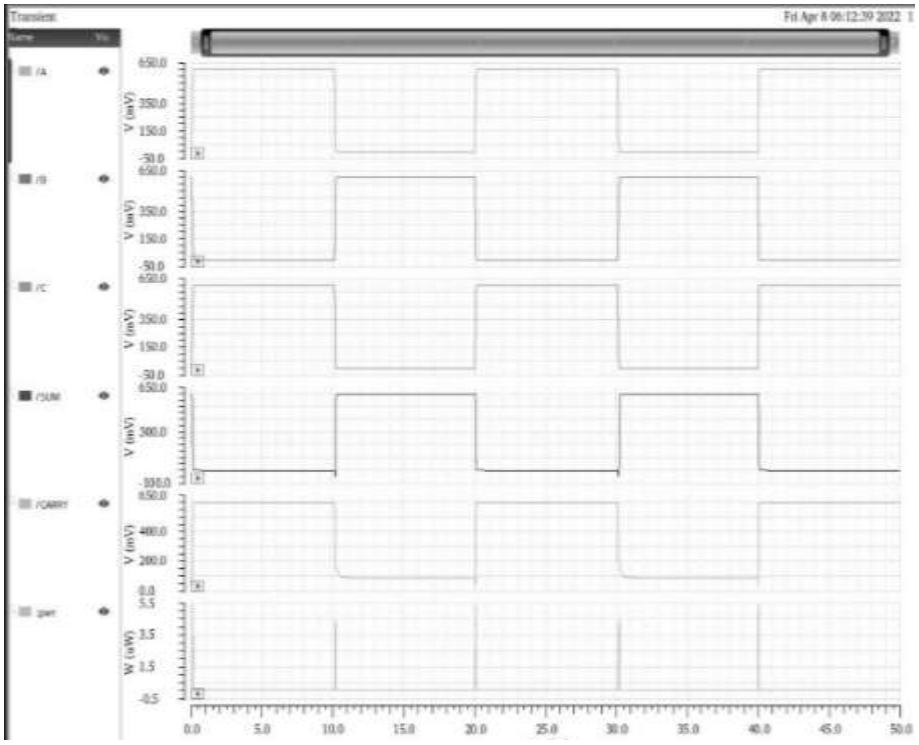

Figure 8:- Simulation waveform of 28Transistor FINFET based Full Adder Design.

10 Transistor GDI one-bit Full Adder Circuit Design

The circuit's primary elements are Mux, Exclusive OR, and Exclusive NOR. There is two mux located at the output stage. Utilizing multiplexer 1 with Exclusive OR logic, carry is acquired, while multiplexer 2 with Exclusive NOR logic yields output sum. The delay is lower since there is just one multiplexer in the carry propagation line [21][22]. The equations are displayed with the circuit schematic in Figure 9.

$$SUM = \overline{C}(A \oplus B) + C(\overline{A \oplus B})$$
$$CARYY = (\overline{A \oplus B})B + (A \oplus B)C$$

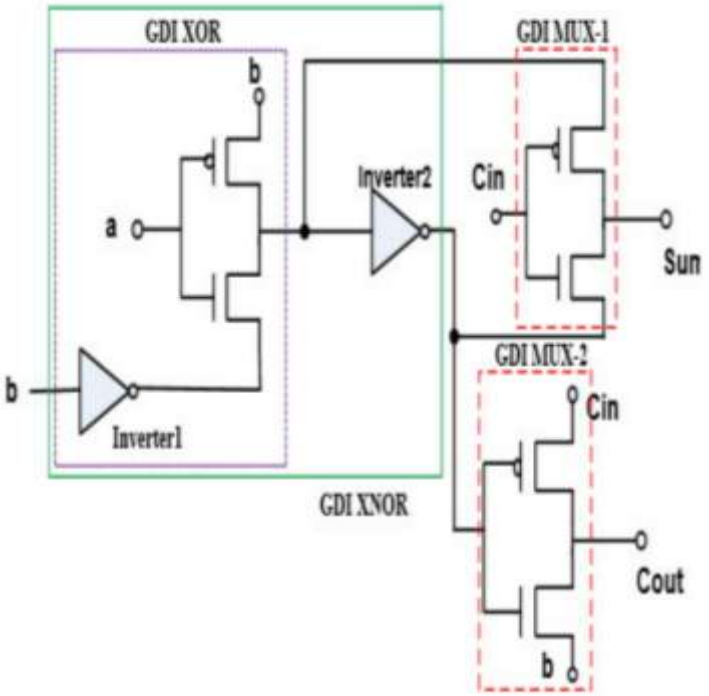

Figure 9:- Circuit Diagram of 10Transistor one bit full adder GDI Design [23].

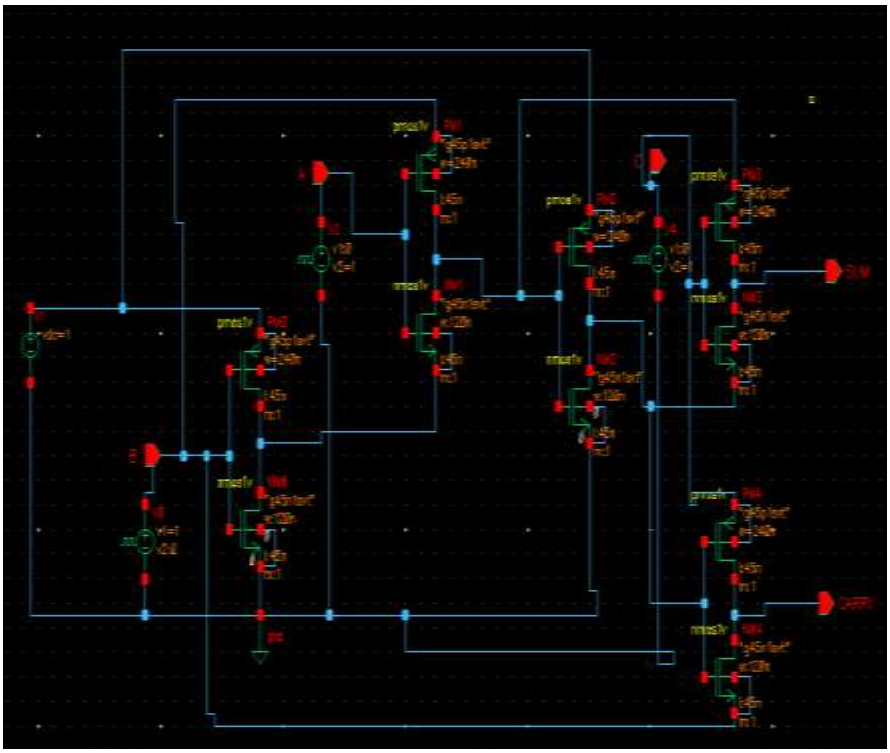

Figure 10:- Schematic of 10Transistor GDI based Full Adder Circuit Design.

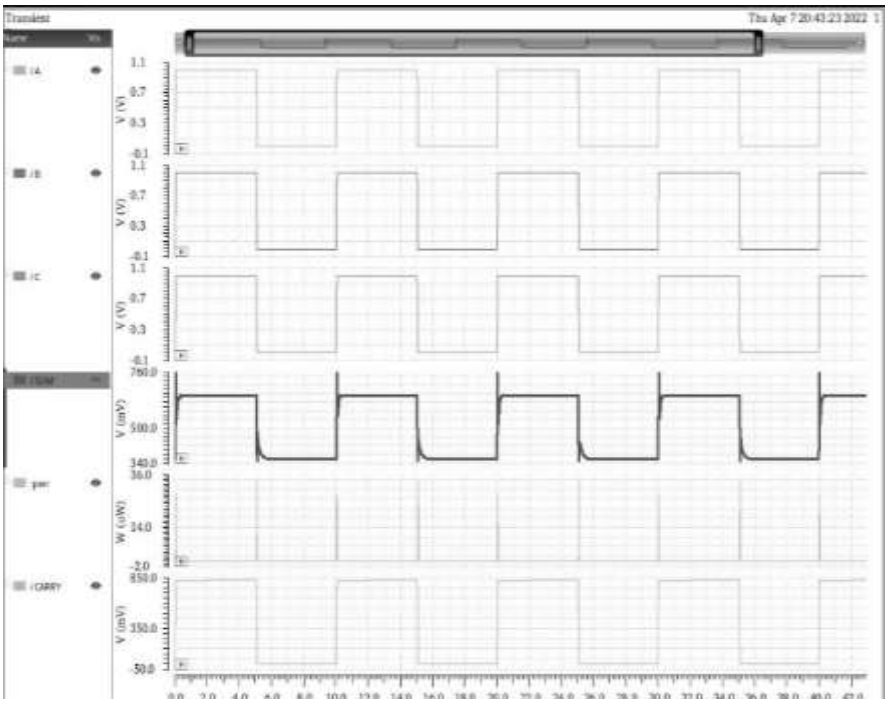

Figure 11:- Simulation waveform of 10Transistor GDI based Full Adder Circuit Design.

Proposed Design:

To increase the output voltage swing, the suggested design employs a single voltage swing restoration circuit. The voltage swing restoration circuit consists of a single inverter and either NMOS or PMOS. Only when the threshold voltage drops at the output end does this transistor turn on. Only one transistor is needed to provide full voltage swing functionality because only one of the logical levels can experience a threshold voltage drop, such as V_{TH} instead of 0 V or V_{DD}-V_{TH} instead of V_{DD} [15]. Figure 12 depicts the suggested design.

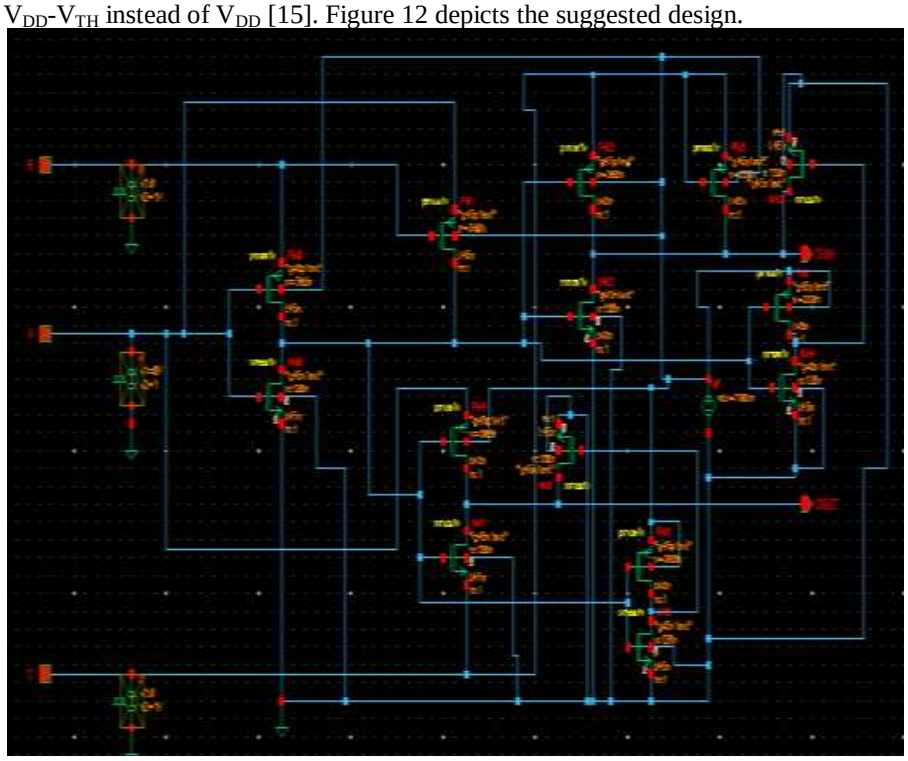

Figure 12:- Schematic of Proposed Design for GDI based logic.

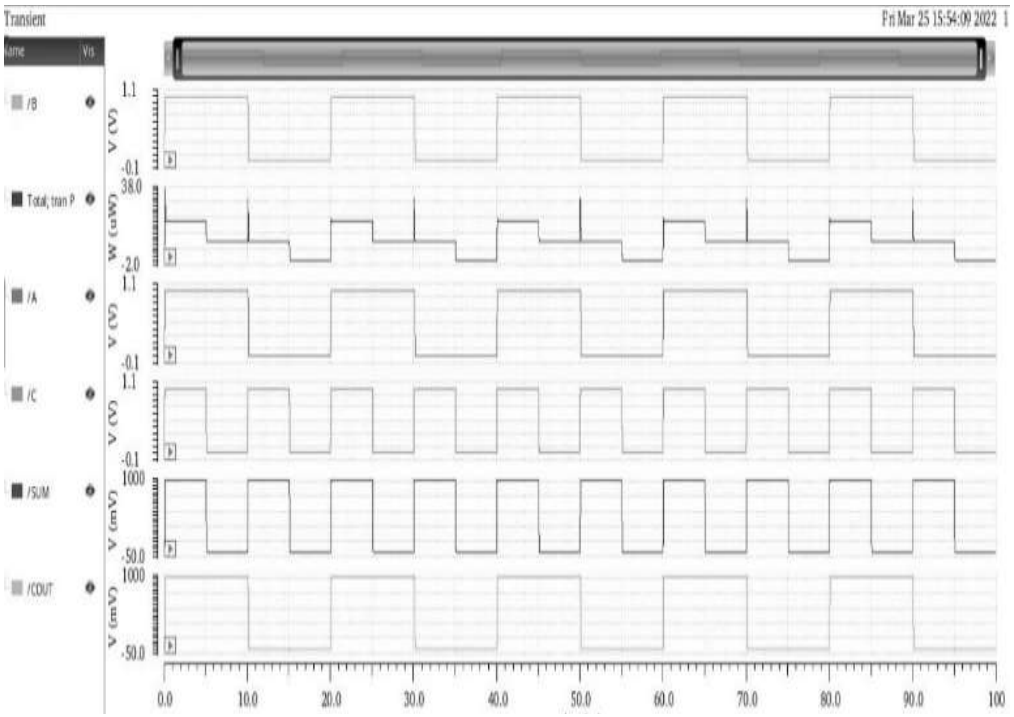

Figure 13:- Simulation waveform of Proposed Design for GDI based logic.

Result Analysis:-

Using 45nm technology, the performance of the circuits is calculated in relation to the quantity of transistors employed, overall power consumption, and latency. Between the Gate Diffusion Input and CMOS-based designs, the amount of transistors used, total average power, and latency are compared. Table 2 shows that the Gate Diffusion Input based design performs significantly better overall than the CMOS-based design in terms of minimal latency and reduced power usage. The suggested design produces significantly better outcomes in terms of full output voltage swing as shown in figure 14.

Table 2:- Performance Comparison of a full adder using 45nm technology.

PARAMETERS	CMOS BASED FULL ADDER	GDI BASED FULL ADDER	PROPOSED DESIGN FOR GDI BASED FULL ADDER
108.3ps	108.3ps	57.326ps	40.2ps
POWER	702nW	156.2nW	120nW
PDP	$7.62*10^{-17}$J	$8.94*10^{-18}$J	$4.824*10^{-18}$J
TRANSISTOR COUNT	28	10	14

The existing circuits, such as the 28T full adder and the 10T GDI-based full adder, are simulated using Finfet 45nm technology in the cadence tool, and performance is evaluated in terms of delay, transistor usage, and power consumption for LVT, SVT, and HVT cells depending on the applications needed. The overall performance of the Gate Diffusion Input based design performs significantly better than the CMOS based design in terms of minimal latency and reduced power consumption is shown Table 3 below.

Table 3:- Performance measure of a full adder using Finfet 45nmtechnology.

	14T GDI BASED FULL ADDER (LVT)	14T GDI BASED FULL ADDER (SVT)	14T GDI BASED FULL ADDER (HVT)
DELAY	20ps	31ps	42.9ps
POWER	86.14nW	39.95nW	30.2nW
PDP	$1.72*10^{-18}$J	$1.23*10^{-18}$J	$1.29*10^{-18}$J

TRANSISTOR COUNT	14	14	14
APPLICATIONS	High speed	Medium speed and Medium power	Low power

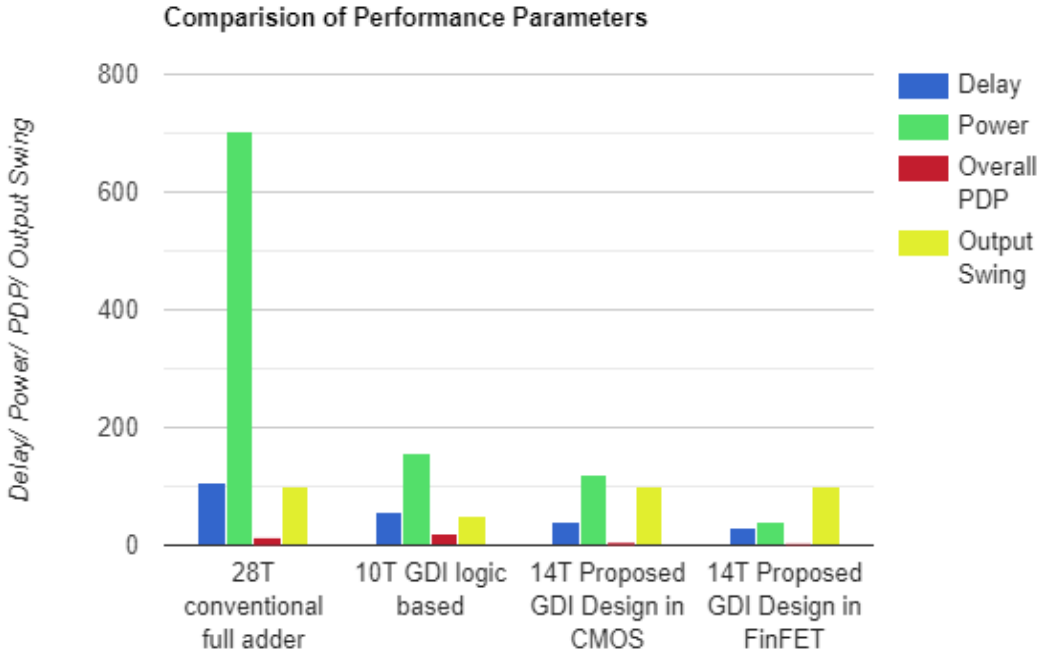

Figure 14:- Performance comparison of the parameters.

Conclusion:-

The proposed design has the smallest power consumption and the smallest delay when compared to other complete adder circuit designs that are already in use according to the acquired simulation findings. In turn, when compared to other complete adder circuits, this enhances the PDP and the output swing. Finfet technology can still be used to achieve more optimization. Therefore, the suggested architecture can be employed for applications requiring fast speed and minimal power.

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