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Survey on Comparison of Booth, Karatsuba and Vedic Multiplier.

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Abstract

The usages of wireless biomedical equipment's are increasing day by day. Most of them are battery-powered and compact in size. The size of these devices is getting smaller and smaller. Moreover that the demand for high-speed devices is also increasing. In that aspect, our aim is to reduce the size and power consumption of the system. In most of the medical equipment the digital signal processing (DSP) block is inevitable. In general, the DPS's in a system board will be one of the highly power hungry modules. So if we reduce the power of that unit will reduce the power on the entire unit. High processing speeds can be achieved only by heavy pipelining and massive parallelization of the circuits inside the DSP block. DSP blocks consist of program and data memory units, ALU, Multipliers, data registers and shifter. Apart from other modules, it is the multiplier which contributes significantly to the critical path. So the selection of multiplier is very important for such DSP applications. The paper deals with an in-depth analysis of different multipliers. Different parameters such as device utilization, delay etc are compared to select an apt multiplier for DSP applications. Design have coded in verilog HDL and synthesized in xilinx ISE 14.2. Implemented on FPGA spartan6

Introduction:-

The Digital signal Processing (DSP) applications request high throughputs and high speed. They have to handle high-resolution moving images, for example, 1024 ×768 pixels or higher at a constant edge rate of 30 edges for each second. High processing speed can be accomplished just by overwhelming pipelining and high parallel circuits.

The design can be easily changed to permit dynamic detail of operand widths, i.e., progressive operations of a given multiplier usage could work upon various word length. The expanded complicated nature of different applications requests quicker multiplier chips as well as more brilliant and proficient duplicating calculations that can be actualized in the chips. It is up to the need of great importance and the application onto which the multiplier is actualized and what tradeoffs should be considered. Generally, the efficiency of the multipliers is classified based on the variation in speed, area, and configuration. Due to rapidly growing system-on-chip industry, not only the faster units but also smaller area and less power has become a major concern for designing very large scale integration (VLSI) circuits. Digital circuits make use of digital arithmetics. Among various arithmetic operations, multiplication is one of the fundamental operations used in DSP.

There are many ways to build a multiplier each providing trade-off between delays and other characteristics, such as area and energy dissipation the objective of a good multiplier and accumulator (MAC) is to provide a physically compact, high speed and low power consuming chip. To save significant power consumption of ASIC design, it is a

good to reduce its dynamic power that is the major part of total power dissipation the multiplier operation is essential and abundant in DSP Applications. Achieving maximum implementation efficiency and clock performance is therefore critical to DSP systems. while maintaining the required maximum performance and resource efficiency. Fully pipelined implementations enable maximum clock frequency performance

Multipliers:-

As the multiplication is nothing but subsequent addition process, the adder is an important block in the design of multiplier. Simple Ripple Carry adder (RCA) can be used for implementing a multiplier. Digital adder has the problem of carry propagation, thus carry select adder is used instead. Carry select adder is known to be one of the fastest adder structures.

The multipliers can be classified as hardware and software multipliers. From that choose the hardware multiplier since final aim is to produce an advanced multiplier to improve the performance of the system. Based on the clocking it is divided as synchronous and asynchronous multipliers. As the application is wireless biomedical we need to communicate many devices simultaneously for controlling the systems we need a clock and we use the synchronous system. Serial and parallel multipliers classification is based on how the input is feed to the system. Serial multipliers are used when the area is a main constraint of the system. But the main drawback with it is the delay. For reduced delay and faster execution we use a parallel multiplier, the thing keep in mind is that area is not that much important.

Throughout this paper, we are discussing the binary multiplication with different bit size. Based on all these criteria the multipliers generally classified as signed and unsigned multipliers. Base on the architceture the multiplier can be divided into three, Truncated Multiplier, Booth Multiplier, Karatsuba multipliers and Vedic multiplier are very some in that categories.

Booth Multiplier:-

Improvement in the multiplier is by reducing the number of partial products generated. The Booth recording multiplier is one such multiplier; it scans the three bits at a time to reduce the number of partial products [13]. These three bits are, the two bit from the present pair; and a third bit from the high order bit of an adjacent lower order pair. After examining each triplet of bits, the triplets are converted by Booth logic into a set of five control signals used by the adder cells in the array to control the operations performed by the adder cells. To speed up the multiplication Booth encoding performs several steps of multiplication at once. Booth's algorithm takes advantage of the fact that an adder-substractor is nearly as fast and small as a simple adder [06].

From the basics of Booth multiplication it can be proved that the addition/subtraction operation can be skipped if the successive bits in the multiplicand are same. If 3 consecutive bits are same then addition/subtraction operation can be skipped. Thus in most of the cases the delay associated with Booth Multiplication are smaller than that with Array Multiplier. However the performance of Booth Multiplier for delay is input data dependant. In the worst case the delay with booth multiplier is on per with Array Multiplier [03].

The method of Booth recording reduces the numbers of adders and hence the delay required to produce the partial sums by examining three bits at a time. The high performance of booth multiplier comes with the drawback of power consumption. The reason is large number of adder cells required that consumes large power [05].

Input a			Partial Product
X_{2i+1}	X_{2i}	X_{2i-1}	**PPi**
0	0	0	0
0	0	1	Y
0	1	0	Y
0	1	1	2Y
1	0	0	-2Y
1	0	1	-Y
1	1	0	-Y
1	1	1	0

Table 1: Booth Encoding For Radix 4 [3],[5]

Karatsuba multiplier:-

Karatsuba algorithm reduces the partial product by splitting the input bit to two or more section based on the size of the input bit. Considering the case of n bit number while performing karatsuba algorithm we will split it into n/2 bits[14].

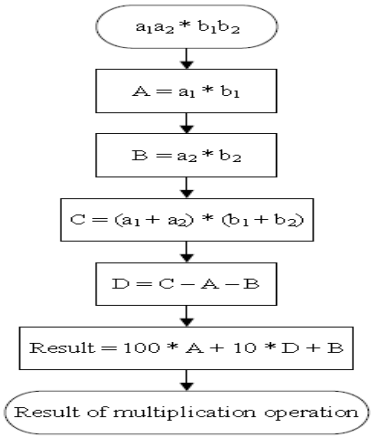

Fig 2: Algorithm for Karatsuba multiplier [14]

Vedic multiplication:-

Vedic mathematics is the name given to the ancient system of mathematics which was rediscovered from the Vedas. It's a unique technique of calculations based on simple principles and rules, with which any mathematical problem-be it arithmetic, algebra, geometry or trigonometry can be solved mentally. It helps a person to solve problems 10-15 times faster [14]. It reduces burden. It provides one line answer. It is a magical tool to reduce scratch work and finger counting. It increases concentration. Time saved can be used to answer more questions. Logical thinking process gets enhanced. Base of Vedic Mathematics Vedic Mathematics now refers to a set of sixteen mathematical formulae or sutras and their corollaries derived from the Vedas [09].

All multiplier contain additions and multiplications. Depending on the number of addition and multiplication the speed, area and delay of the system will vary. From the table it is clear that the Vedic multiplier takes less number of addition and multiplication units

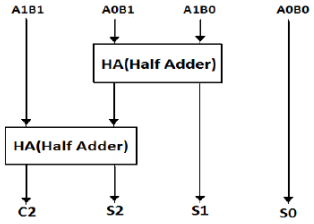

Fig 3: Architecture of Vedic multiplier [2]

Comparison in terms of Addition and Multiplication:-

The number of addition and multiplication decide the speed of operation and the delay. The numbers of these blocks are also capable to increase or decrease the area power etc of the entire design. While considering a multiplier unit

the addition and multiplication is the most repeating unit in them. In the table below we are comparing the number of addition and multiplication. Comparing other multiplier, Vedic multiplier requires less Multiplication and addition steps.

	8x8 bit	16x16 bit	32x32 bit
Booth Multiplier	40M 26A	96M 72A	288M 243A
Karatsuba Multiplier	15M 10A	40M 24A	198M 75A
Vedic Multiplier	8M 4A	16M 8A	32M 16A

Table 2: Comparison in terms of Addition and Multiplication

M – Multiplication
A – Addition

Performance analysis:-

The performance of any system is analyzed based on power consumption, delay, and area. The delay is always calculated as the sum of net delays and gate delays. Power consumption is the total consumed by the entire system. The area can be calculated either based on a number of look-up tables used or area of the entire system. Another major factor in performance analysis is the clock cycles used for the execution. The table below shows the performance analysis of 32-bit input multiplier on Spartan 3E and Spartan 6 board respectively. From the table, it is clear that Vedic multiplier consume more power and area while comparing with Booth and Karatsuba multiplier. But it has reduced delay.

	Power (uW)	Delay (ns)	Area (nm^2)
Booth Multiplier	235.184	6.567	402.320
Karatsuba Multiplier	335.85	5.458	1198.51
Vedic Multiplier	402.32	4.932	974.87

Table 3: Performance analysis

Comparison in Terms of Gate:-

The multipliers consist of a large number of gates for different arithmetic and logic operation. As the number of gates increases the area occupied and the gate delays will also increase sometimes it cause wastage of power by heating up of the component as the number of gates increases the amount of via will also increase. In turn which increase the circuit density and chances for short circuit [7]

	8Bit	16Bit	32Bit
Booth Multiplier	354	1693	7589
Karatsuba Multiplier	411	1803	8659
Vedic Multiplier	294	1545	7268

Table 4: Comparison in terms of gates

From the survey, it is clear that no multiplier can be created as ideal. We will optimize the parameter as per our requirement**.** The Vedic multiplier has less number of gates required hence power dissipation is very small hence low power consumption. As the number of bits increases, gate delay and area increase very slowly as compared to other multipliers. The numbers of devices used in Vedic multiplier are less. The main advantage is delay increases slowly as input bits increase. The Vedic multiplier has the biggest advantage as compared to other multipliers over gate delays and regularity of structures. It has higher throughput operations.

Comparisons in Terms of LUT and Delay:-

	2x2	4x4	8x8
Total no. of LUT	-	24000	28800
LUT used	-	6	20
Delay in (ns)	-	12.85	20.69

Table 5: Results of Booth Multiplier

	2x2	4x4	8x8
Total no of LUT	9112	9312	9582
LUT used	5	14	22
Delay in (ns)	5.658	12.35	17.76

Table 6: Results of Karatsuba Multiplier

	2x2	4x4	8x8
Total no. of LUT	9112	9312	9582
LUT used	4	11	18
Delay in (ns)	5.505	11.35	16.85

Table 7: Results of Vedic Multiplier

LUT - Look Up Table

Conclusion:-

On doing the hardware implementation of the three multipliers I could conclude that the Vedic multiplier is best. If we consider the number of LUTs used by the Vedic multiplier is 22.2 % less than the Karatsuba multiplier and 11.1 % less than the booth multiplier. If we consider the delay of the Vedic multiplier is 30.56% less than the Karatsuba and 22.83% less than the booth multiplier.

While doing a detailed analysis into different Vedic sutras Nikhilam sutra and Urdhva-Tiryagbhyam can be applied to any numbers. And also it is clear that for lower bits the Urdhva-Tiryagbhyam is giving better performance and for higher bits, Nikhilam sutra gives better results.This paper presents a survey on 3 different Multipliers. The requirements of good Multipliers for DSP have been identified. So as a future work, I need to implement Vedic multiplier for Double Precession Floating Point for DSP unit

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