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INTERNATIONAL JOURNAL OF ADVANCED RESEARCH (IJAR)

Article DOI: 10.21474/IJAR01/17183
DOI URL: http://dx.doi.org/10.21474/IJAR01/17183

RESEARCH ARTICLE

DESIGN AND IMPLEMENTATION OF SRAM 6T FOR 2 BYTES

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Manuscript Info

Manuscript History
Received: 26 April 2023
Final Accepted: 31 May 2023
Published: June 2023

Abstract

SRAM has become a significant segment in numerous VLSI Chips because of their huge stockpiling thickness and little access time. SRAM has gotten the theme of impressive research because of the fast improvement for low power, low voltage memory structure during late years because of increment interest for scratch pad, workstations, IC memory cards and specialized gadgets. SRAMs are broadly utilized for versatile and PC applications as both on chip and off-chip recollections, in view of their accessibility and low backup spillage. The fundamental target of this paper is assessing execution regarding Power utilization, deferral and Signal to Noise Margin of existing 6T SRAM cell in 45nm and 180nm innovation.

Introduction:-

6T static arbitrary access memory is a sort of semiconductor memory that utilizationbi stable locking hardware to store each piece. The term static recognizes it from dynamic RAM which must be occasionally re-established. SRAM displays information memory, however is as yet unpredictable in customary sense, that information is inevitably lost when memory isn't powered.

6T Sram Cell Operation

Reserve Mode (the circuit is inert) In backup mode word line isn't attested (word line=0), so pass transistors N3 and N4 which associate 6t cell from bit lines are killed. It implies that cell can't be gotten to. The two cross coupled inverters shaped by N1-N2 will keep on input each other as long as they are associated with the stockpile, and information will hold in the hook.

Understand Mode (the information has been mentioned) In read mode word line is declared (word line=1), Word line empowers both the entrance transistor which will interface cell from the bit lines. Presently qualities put away in hubs (hub an and b) are moved to the bit lines. Accept that 1 is put away at hub a so bit line bar will release through the driver transistor (N1) and the bit line will be draw up through the Loadtransistors (P1) toward VDD, a legitimate 1. Structure of SRAM cell requires read strength (don't upset information when perusing) . Compose Mode (refreshing the substance) Assume that the phone is initially putting away a 1 and we wish to compose a 0. To do this, the bit line is brought down to 0V and bit bar is raised to VDD, and cell is chosen by raising the word line to VDD. Normally, every one of the inverters is planned so that PMOS and NMOS are coordinated, in this way inverter limit is kept at VDD/2. In the event that we wish to compose 0 at hub a, N3 works in immersion.

At first, its source voltage is 1. Channel terminal of N2 is at first at 1 which is pulled somewhere around N3 on the grounds that entrance transistor N3 is more grounded than N1. Presently N2 turns on and P1 turns off, along these lines new worth has been composed which powers bit line brought down to 0V and bit bar to VDD. SRAM to work

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in compose mode must have compose capacity which is least piece line voltage required to flip the condition of the cell.

Literature Survey:-

1. Debasis Mukherjee, Hemanta Kr. Mondal explained the butterfly method to calculate static noise margin, write noise margin and read noise margin of a 6T SRAM cell. In This paper, he explained how the stability of memory cell depends on the values of the pull up ratio and cell ratio.
2. Jan M. Rabaey Anantha ChandrakasanBorivoje Nikolic explained the design of SRAM Based memory with all peripherals like pre-charge, row decoder, sense amplifier, tree decoder for column multiplexing. Monolithic architecture for small memory design is explained in a clear manner.
3. Sung-Mo Kang and Yusuf Leblebici explained the design of the single 6T SRAM such that during read operation it should not allow modification for the stored data and during write operation it should allow modification of the stored data.
4. Kunihiko Yamaguchi, Hiroaki Nambu et al. has developed 64Kb ECL CMOS SRAM based memory. In this thesis he utilizes a blend of ECL word line drivers and CMOS SRAM cell arrays and some write circuits. Without any intermediate voltage level converter the ECL word line drivers and write circuit drives the CMOS SRAM Cell arrays.
5. Rakesh Chandankhede, has proposed a decoupled latch with a current controlled sense amplifier which gives improvement in power Consumption and performance. At the point when EN sign is low, the logic on Bit and Bit-bar grows on the latch output, i.e. differential voltage, however, it is not getting increased as the pull down transistor is off and consequently same logic holds still EN goes high. Here line having low voltage goes to release to ground when EN signals.

Proposed Methodology:-

Semiconductor recollections are characterized taking into account usefulness, access patterns and storage capacity components. They are partitioned into Read Only Memories, Read-Write Memories and Non Volatile Read-Write Memories . The ROM fits in with the class of non-volatile recollections. It encodes data in the circuit topology that is by including or uprooting transistors. Since this topology is hardwired, the information cannot be altered; it must be perused. Detachment of the force supply from the gadget does not bring about the loss of information.

The RAM acronym is utilized to depict Random Access Read-Write recollections. Information can be gotten to from an arbitrary area in any request. In a RAM, the information is put away either in flip-flops or in capacitors. Contingent upon which technique is utilized, they are delegated either Static RAM (SRAM) or Dynamic RAM (DRAM) separately. The DRAM cell comprises of a capacitor to store information and a transistor to get to the capacitor. Cell data, i.e. voltage is corrupted basically because of an intersection spillage current at the storage node. In this way the cell information must be perused and revised periodically. On the other hand SRAM cell consists of a latch, therefore cell data are kept as long as power is turned on and refresh operation is not required.

Static Random access memory (SRAM) is a sort of unpredictable semiconductor memory to store paired rationale "1" and "0" bits. SRAM utilizes bi-stable hooking hardware made of Transistors/MOSFETS to store every bit. In SRAM the information is lost when the memory is not electrically fuelled. SRAM is quicker and more dependable than the more normal DRAM. Due to its high speed SRAM is used in cache memory in computers, similarly DRAM is used in main memory of a computer where density is much more important than its speed.

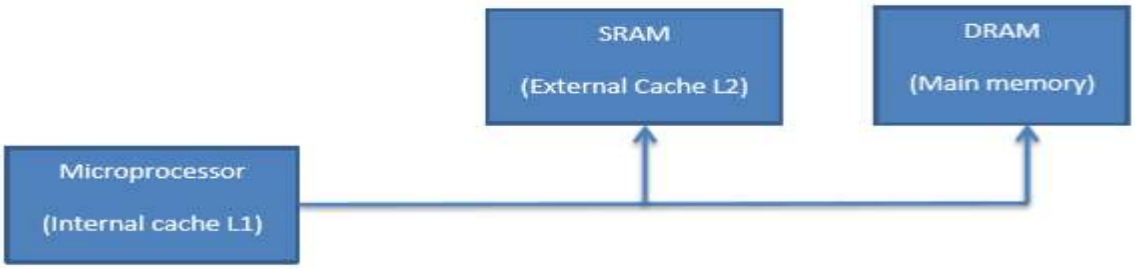


Fig: 3.0.1:- Block Diagram Representation.

A SRAM is intended to fill two requirements: To give an immediate interface the CPU at rates not achievable by DRAMs and to supplant DRAMs in frameworks that oblige low power utilization.

Introduction to SRAM Based Memory:

Depending upon the utilization of a clock, SRAM can be partitioned as synchronous SRAM and asynchronous SRAM. In synchronous SRAM, all the inward flags and timing will be controlled by the clock edge. Information in, control motions and location identifies with the clock signal, it is for the most part utilized as a cache memory while Asynchronous SRAM is autonomous of clock recurrence. All the inner signals and timings are introduced by the location move. The extent of offbeat SRAM fluctuates from 4 KB to 64 MB. Because of the quick access time of Asynchronous SRAM, it is suitable as main memory for cache less embedded processors which are utilized as a part of modern hardware, estimation of frameworks, organizing hardware.

The operation of SRAM can be partitioned into three states, first one is Standby mode, in this mode word line is not initiated, so the address and data lines are kept withdrawn from SRAM memory cells, subsequently cells keep the information as it is and no read and write operation is there. Power consumption in this mode is reduced the most. A second mode of operation is reading data from cells. Assume we are reading data 0 which has already stored in the memory cell. The Read cycle begins with pre-charging the bit line and bit line bar, after pre-charge operation word line gets actuated as by particular row address and one of the bit line starts discharging through the cell. Here logic 0 is stored in the cell initially, hence Bit line voltage starts discharging through the ground and simultaneously bit line bar voltage starts charging to VDD. Then sense amplifier senses the difference between the voltages on two bit lines and gives proper output, i.e. reads 0 or read 1. If the bit line voltage is greater than the bit line, bar voltage than the output of the sense amplifier as logic 1 which indicates read 1 operation.

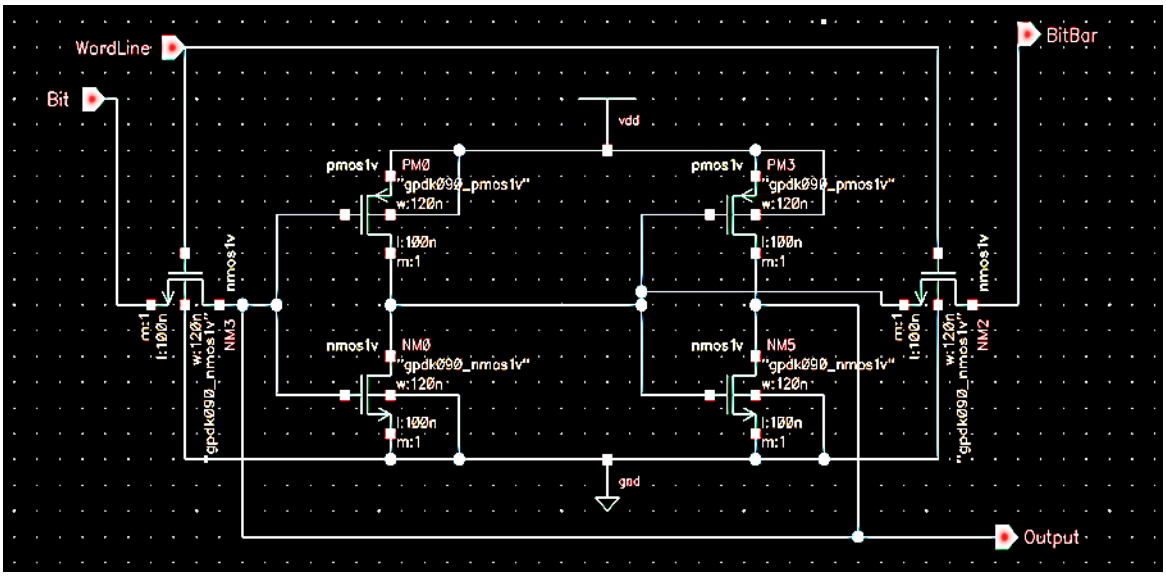


Figure 3.1.1:- Schematic of 1 Bit 6T SRAM.

Similarly if bit line voltage is less than bit line bar voltage then output of sense amplifier indicate read 0 Operation . Presence of sense amplifier increases the speed of operation of memory as it senses the small difference between voltages on bit lines otherwise it takes lot of time to perform any read operation.

The following method of operation of SRAM is writing data in to the SRAM cell. Write operation begins with applying data need to be written on bit lines. Suppose we need to write logic 0, then the bit line will get discharged to 0 and bit line bar voltage is charging to 1. At that point the word line will get actuated, and proper information gets to keep in to the cell.

Peripheral circuitry of SRAM Based Memory:

To get required frequency of operation efficient peripherals has to be designed, since the memory core exchanges performance and reliability for diminished area, memory plan depends exceedingly on the peripheral hardware to recuperate both speed and electrical integrity.. In this section we discuss the row decoders, word line drivers, pre-charge circuit, column multiplexers/Decoders, Sense amplifiers and write drivers. Generally for Smaller memory

designs monolithic architectures are preferred, but in the Design of bigger memories monolithic architecture will not give efficient performance.

The frequency of operation of the circuit is reduced by a factor of two as the number of rows doubles. Similarly the frequency of memory, reduced by a factor of four as the number of 42 columns doubles, hence in bigger memory designs memory portioning technique is used which is known as memory banking.

Row decoder:
At whatever point memory takes into consideration arbitrary address based access address decoders must be available. The Boolean function of the decoder is comparable to n-input AND logic gates, where the extensive fan-in AND operation is actualized in a various leveled structure. The configuration of these decoders has a noteworthy impact on the speed and power dissipation of the memory. Two classes of decoders that is row decoder, whose task is to empower one memory row out of , where M is the width of particular fields in address word. While considering these decoders, it is imperative to keep the complete memory floor plan in context.. When the number of inputs is more than or equal to four then the speed of operation of the decoder is effected so pre-decoders are to be used which reduces the large fan-in such that the speed of the decoder is improved. The principal level is the pre decoder where two groups of address inputs and their complements are first decoded toinitiate one of the pre-decoder yield wires separately to obtain the partially decoded outputs.

The pre-decoder yields are consolidated at the following level to enable the word line. The decoder delay comprises of word line wire delay, interconnect delay of pre-decoder and gate delays in the critical path. As the wire RC delay develops as the square of the wire length, the wire delays inside the decoder structure, particularly of the word line, gets to be critical in extensive SRAMs. From delay analysis, it was observed that the NOR based decoder is quicker than the NAND based decoder.

Monolithic Cell Array:
SRAM cell array size and its introduction are most imperative to consider before the start of circuit configuration. For the outline of bigger memories with specific operating frequency, we have to plan the small blocks of memory which fulfil the frequency prerequisite and numerous utilization of such small blocks will give the bigger memories.

Array size can be defined as the number of rows and columns and the frequency of operation is mainly depends on the number of rows and columns. Frequency of operation is reduced bya factor of two as the number of rows doubles whereas frequency is reduced by a factor of four as the number of columns doubles. Hence, to increase the speed of memory, number of rows and columns are to be decreased.

Word Line Driver:
As word lines have large parasitic capacitance the output of decoder cannot drive the last cell in a memory row. So there must be a buffer exists between decoder and monolithic memory array to drive the last cell in a row. If the word line driver is capable to drive the worst case, i.e. last cell, then we can access all cells in a row.

The schematic of the typical word line driver. It is a circuit which is nothing but the cascading connection of the AND gate with an even number of inverters [13]. To drive the word line which is having a large parasitic capacitance we need to design a stack of inverters with increase in size such that it should capable to drive the worst case cell.

Pre-charge Circuit:
This circuit is used to pre-charging the both bit lines voltages to supply voltage and pre-charging operation should perform before every write and read operation. The pre-charge circuit which consists of pull up PMOS transistors and an equalizer which is used to equalize the voltage on both bit lines. The pull up PMOS transistors are controlled by PR signal i.e. The Transistor M3 shown in the schematic of Pre-charge is an equalizer which is used to equalize the voltage on both bit lines. Pre-charge circuit should provide large driving current to drive the bit lines which are having large parasitic capacitances, so the transistor sizes of pre-charge circuit need to be increased.

Sense Amplifier:
Sense Amplifiers plays a crucial role in the design of memories to achieve performance, reliability and functionality of memory circuits. Normally sense amplifiers perform various operations like voltage amplification, reduction in delay, power reduction and restoration of original signal. Generally sense amplifiers are used in the memories to speed up the read operation. Sense amplifier takes the small signal difference bit line voltageas input and gives full swing single ended output [17]. Access time and power consumption of memory is affected by the sense amplifier hence the performance of memory is improved by reducing both sensing delay and power dissipation.

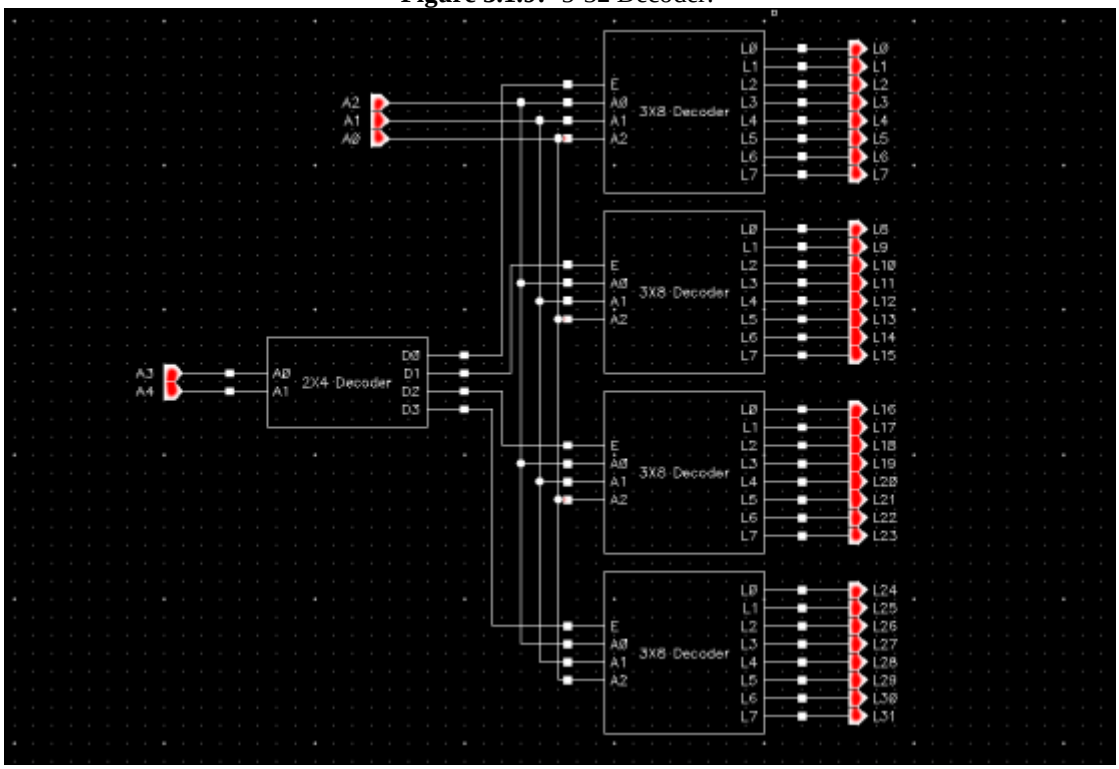
When SE is logic low then both bit line voltages are charges to supply voltage , when SE is logic high then sense amplifier is getting ON and one of the bit line voltage discharges to ground via pull down transistor ,. It takes BL and voltages as an input and generates single ende d output. When BL voltage is greater than the voltage then current through is increases and simultaneously current through decreases to maintain as a constant, then the drop across is decreases hence output voltage increases, which interprets output as the logic 1.Similarly when BL voltage is less voltage then it indicates output as thelogic 0. In this way, Sense amplifier plays a crucial role in the memory read operation.

Write Driver:
The tremendous bit line swing can bring about huge power dissipation in write operation and during read operation, the bit line voltage swing is normally limited to 180mV, and consequently the write cycle can consume around 1/8th more power than a read operation. Initially, before write operation both bit line voltages are charging to supply voltage and the write operation is performed by enabling WR_EN signal. Suppose if we want to write logic 0 in to the memory cell, then the BB line voltage charges to supply voltage VDD and BT line voltage is discharges to lower potential i.e. ground.

The data stored in bit line, BT and bit line bar, BB is accessed by enabling word line. The sizing of transistors in write driver is quiet large to provide large driving current.

Column Decoder/Mux:
This circuit is used to select particular column in the memory array.The typical column decoder/Mux in which the outputs of 2 to 4 decoder are used to enable pass transistors.

Figure 3.1.9:- 5-32 Decoder.



Depending on the output of decoder only of the bit line or bit line bar is selected and the above circuit acts as a 4 to 1 multiplexer. COL_EN signal is used to enable the column decoder/Mux circuitry. As we discussed earlier the frequency of operation of memory is strongly affected by number of columns as well as number of rows. Hence to maintain good frequency of operation and an aspect ratio of 32×32, we are using DWL (Divide Word line Architecture). Consider the design of 1Kb array, there is totally 32 numbers of SRAM cells present in a cell row and these 32 cells are divided into 4 portions such that the output of SRAM memory is having a size of 8 bits. So 4 to1 multiplexer is used to select one of the portion out of 4 portions.

In this way peripherals design plays a vital role in the design of any memory and efficient peripheral leads to achieve good frequency of operation. In this thesis all the above peripherals are designed and layouts of all circuits are drawn .Layout and post layout simulations of all peripherals are performed and a frequency of 8GHz, 1Kb SRAM is designed. Finally using Banking Method 16Kbmemory is designed which operates at a frequency of 1GHz.

Project Description

Depending on the type of load used at the inverter of Flip-Flop, the SRAM Cells are classified into three categories such as 4-Transistor cells, 6-Transistor cell and Thin-Film Transistor (TFT) cell. Out of these three types 6-Transistor SRAM is widely used. SRAM cells stored the data as long as power supply is given, and it lost its stored data once power supply is removed. It doesn't require any periodic refreshment operation like DRAM because in SRAM data is stored in Flip-flop rather than in a capacitor.

The data storage Static Random Access Memory cell contains a latch circuit which is usually stores the data of one bit and the memory cell contains two stable points at nodes A and B.

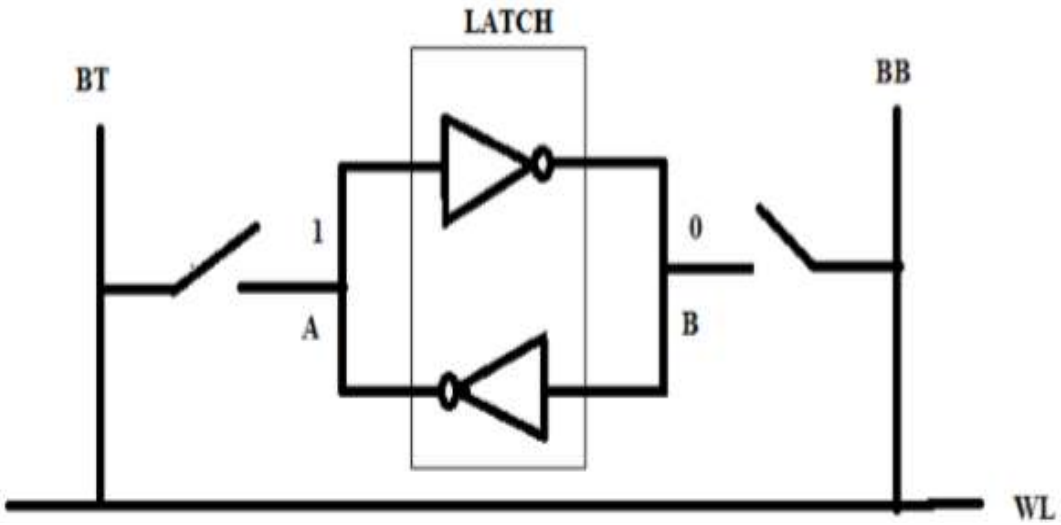


Figure 4.0.1:- Basic SRAM Memory Cell.

Word line is used to access the data stored in the memory cell via complementary bit lines. Complementary data is stored at two bit lines which will enhance the performance of memory with respect to noise immunity and speed of operation.

6T Cmos Sram Cell:

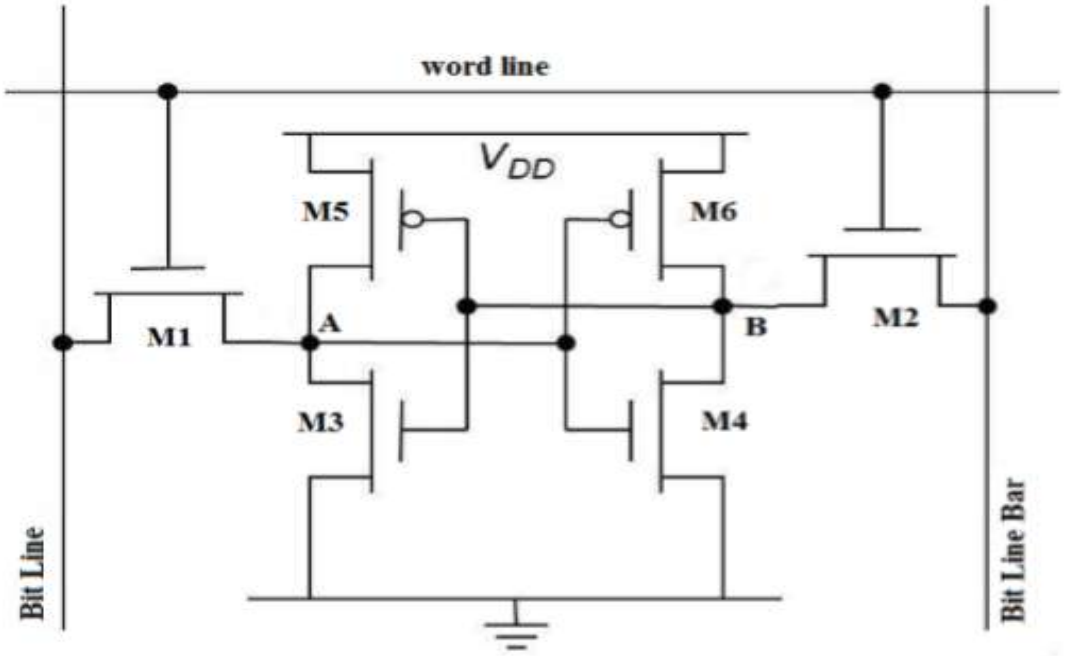


Figure.4.1.1:- 6-Transistor SRAM Memory cell.

Now a day's 6T SRAM is widely used in the design of SRAM Based memories because of its advantages with respect to other cells. Low power SRAM cell design can be done by the back to back connection of two CMOS inverters which is having lot of advantages.

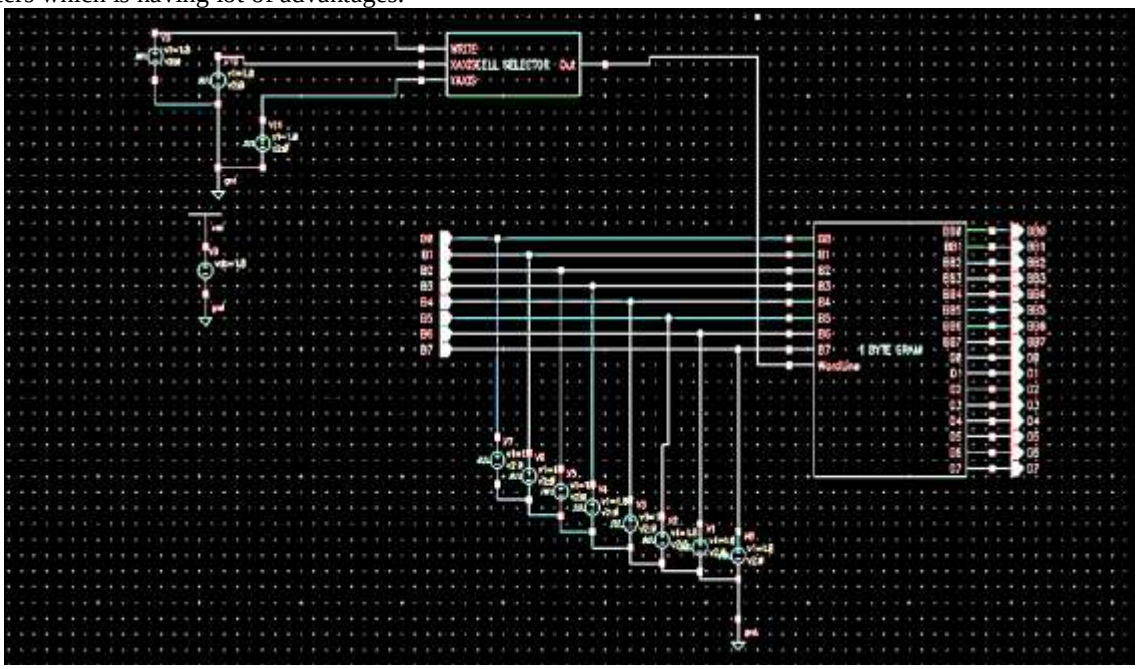


Figure 4.1.2:- 6T SRAM for 1 Byte.

To focus the sizes of the transistors in 6-T cell, various outline criteria must be taken into account such that it should not destroy the information present in the cell during read operation and similarly it should allow modification of data in write operation. So design of proper of transistors is must to satisfy above two requirements. The stability and speed of SRAM cell can be increased by increasing the supply voltage but increase in supply voltage leads to increase in the power dissipation of circuit as power dissipation varies with square of supply voltage. So always

there exists a trade-off between power and speed. So we have to design a SRAM cell such that it consumes less power with better speed. The operation of SRAM memory is classified into three modes i.e. standby mode, write mode and read mode.

Standby mode:
In this mode word line is not activated, so both the access transistors are disconnected from memory cell, hence in this mode memory cell retains its previous data as long as power supply is provided. Here the column capacitances are charges to supply voltage, though. In this mode memory cell consumes less power.

Write Mode:
Suppose if we want to perform write zero operation by assuming initial stored data in memory cell as logic one. So in the beginning of write operation the voltages present at two nodes A and B are VDD and 0V respectively hence initially the two transistors are operated in cut off mode whereas the transistors are operated in linear region. Now by using write driver circuit the column voltage of bit line is forced to logic zero.

Now the pass transistors are activated by using word line whose address is given by row decoder. In order to achieve basic requirements which we discussed earlier, we should have why because the bit line voltage is less than the bit line bar voltage. The necessary condition to be satisfied in the read operation is given as follows,

$$\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} < \frac{\mu_n}{\mu_p} \frac{2(V_{DD}-1.5V_{T,n})V_{T,n}}{(V_{DD}+V_{T,p})^2} \quad \text{---------- (A)}$$

The following Figure4.1.3 depicts the operation of write zero.

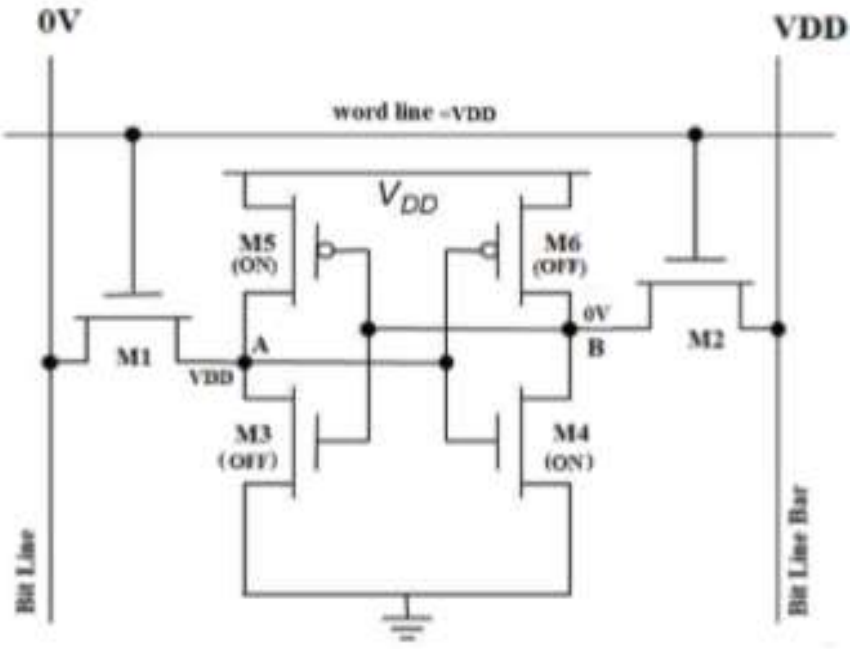


Figure 4.1.3:- Write Mode operation.

Read Mode:
Before the Read operation the two bit line voltages charge to supply voltage VDD. During read mode, suppose if we want to perform read 0 operations, then assume initial data stored in the memory cell is logic 0.The figure 4.4 depicts the read zero operation of 6T SRAM Cell and the initial voltages present at the storing nodes A and B is 0V and VDD respectively.

Hence transistorsare operated in cut-off region whereas the transistors are operated in linear region. The pass transistors are activated by using word line which is controlled by row decoder circuit. Now there is no current flow in transistor why because the voltages at node B and bit line bar voltages are almost equal which is equal to VDD. On the other hand, the transistors will exhibit a nonzero current and the bit line voltage is discharges to ground from VDD.

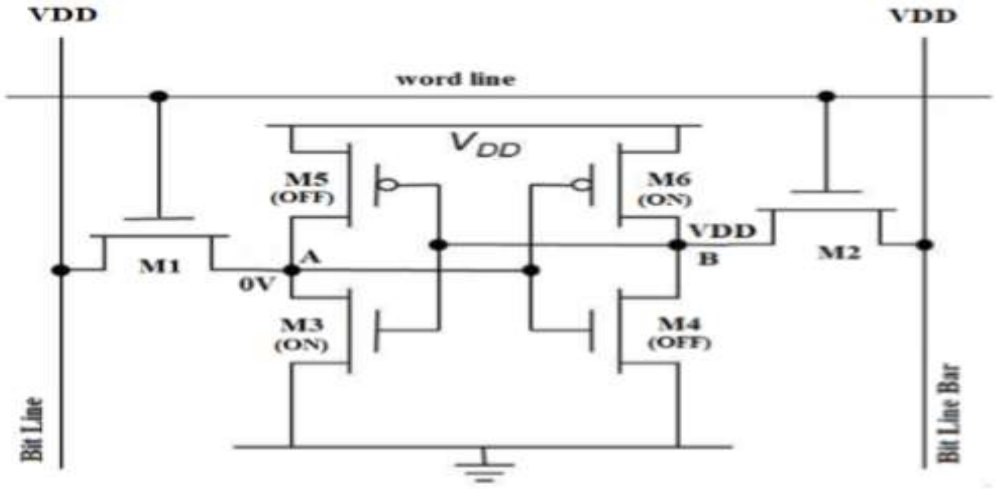


Figure 4.1.4:- Read Mode operation.

Now both the bit line voltages are given to the inputs of sense amplifier and it will produce logic 0 as output why because the bit line voltage is less than the bit line bar voltage. The necessary condition to be satisfied in the read operation is given as follows,

$$\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_3} < \frac{2(V_{DD}-1.5V_{T,n})V_{T,n}}{(V_{DD}-2V_{T,n})^2} \quad \text{----------(B)}$$

By using above two conditions (A) and (B) mathematically, we can design the 6T-SRAM cell. Otherwise the below condition needs to be satisfied which is obtained from practical observation in order to perform correct operation i.e. either read or write operation.

$$\left(\frac{W}{L}\right)_{pull-up} < \left(\frac{W}{L}\right)_{access} \ll \left(\frac{W}{L}\right)_{pull-down} \text{----------(C)}$$

So finally the following transistor sizes will satisfy all the above conditions (A),(B)and (C) and perform correct read and write operations i.e.

$$\left(\frac{W}{L}\right)_{pull-up} = \frac{120}{100}, \left(\frac{W}{L}\right)_{access} = \frac{120}{100} \;\&\; \left(\frac{W}{L}\right)_{pull-down} = \frac{180}{100}$$

The schematic of 6T-SRAM Cell and symmetrical layout structure of 6TSRAM Cell with cell area of cell is 4.066but standard layout has an area of 7.7125. So for an array of size 32×32, the area saving in symmetrical structure compared to standard structure is around 47.21%.

Results:-

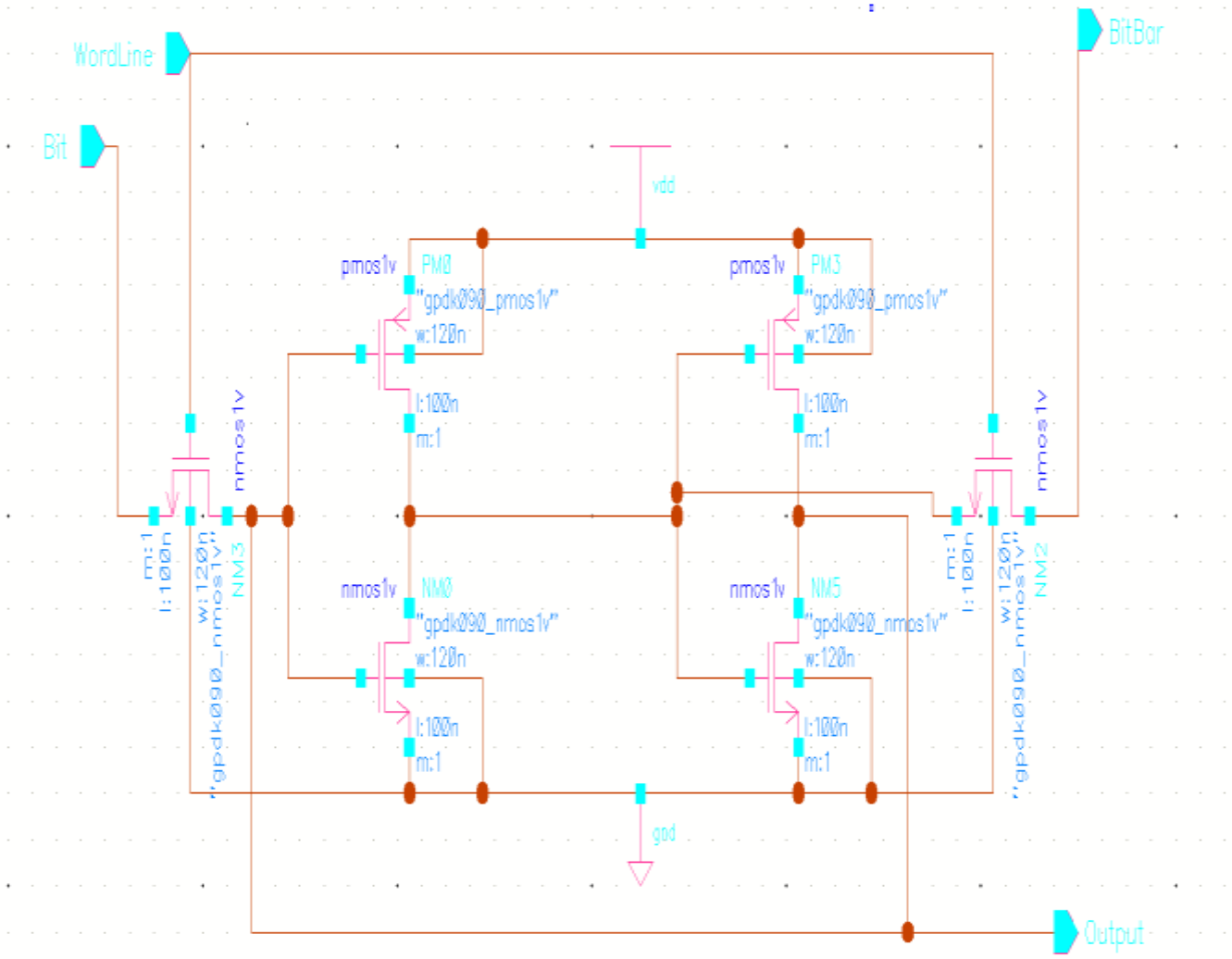


Figure 5.1:- Schematic of 1 Bit 6T SRAM.

Figure 5.2 Schematic of 1 Bit 6T SRAM Symbol

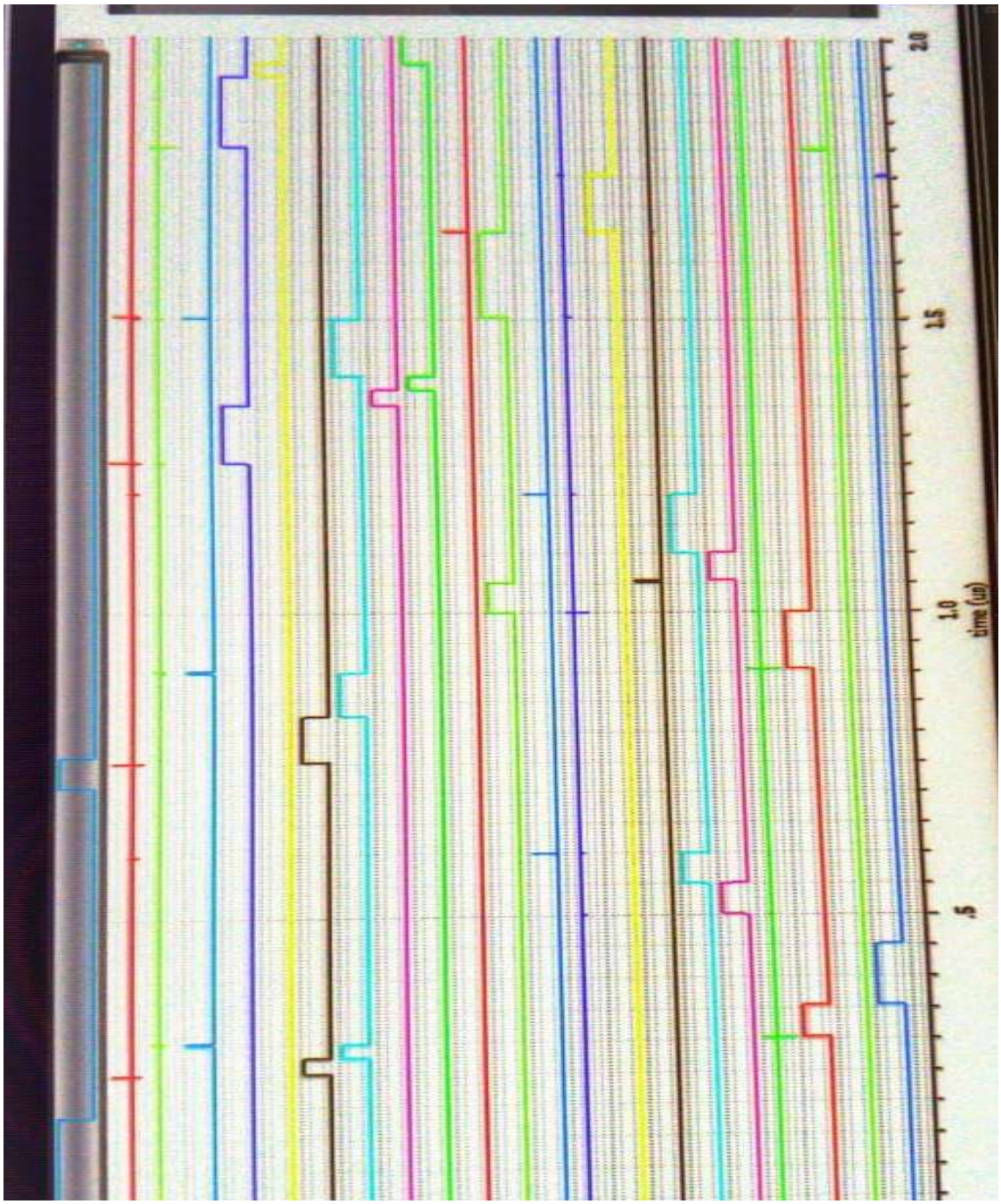


Figure 5.3:- Output Simulation of 1 BYTE SRAM.

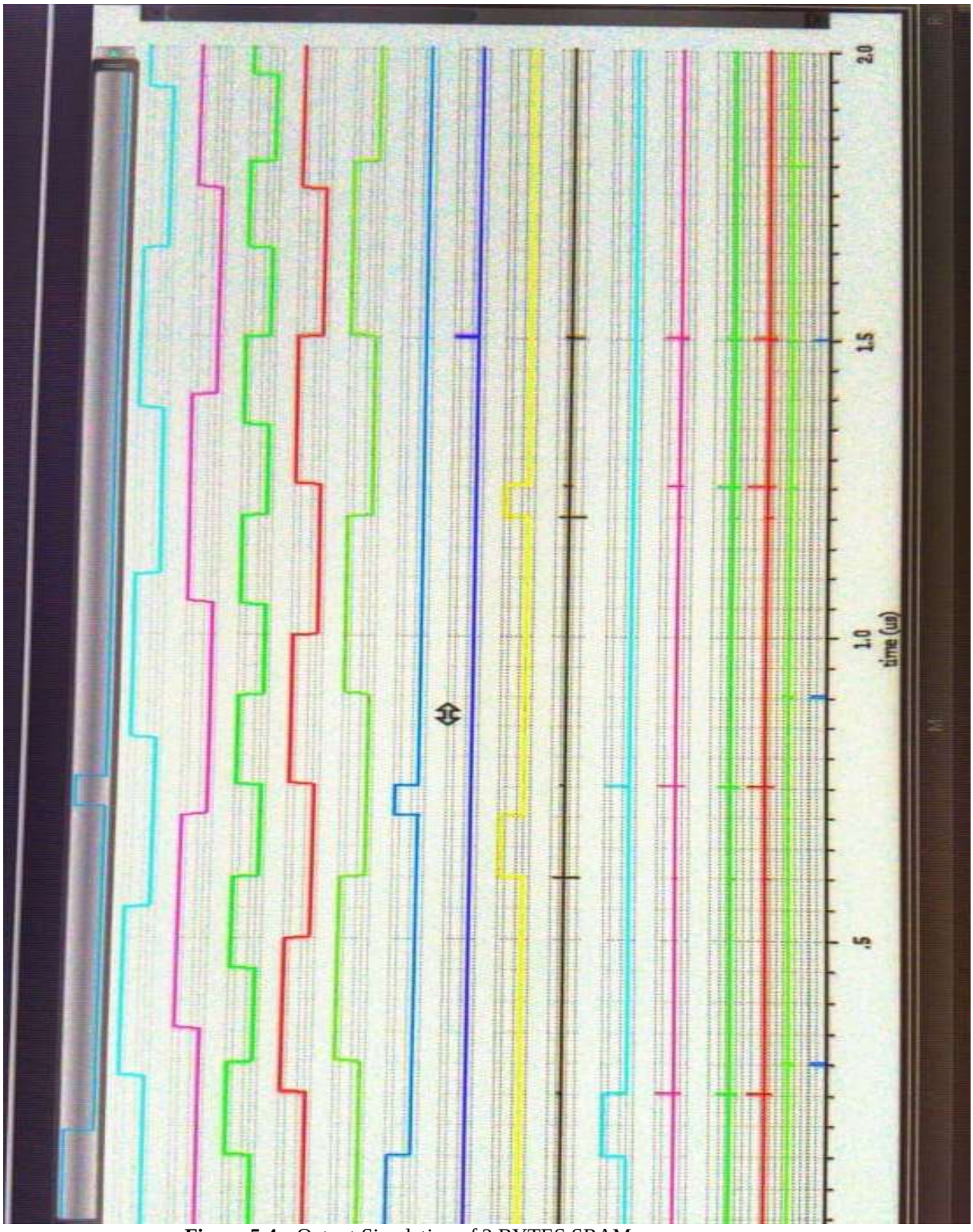


Figure 5.4:- Output Simulation of 2 BYTES SRAM.

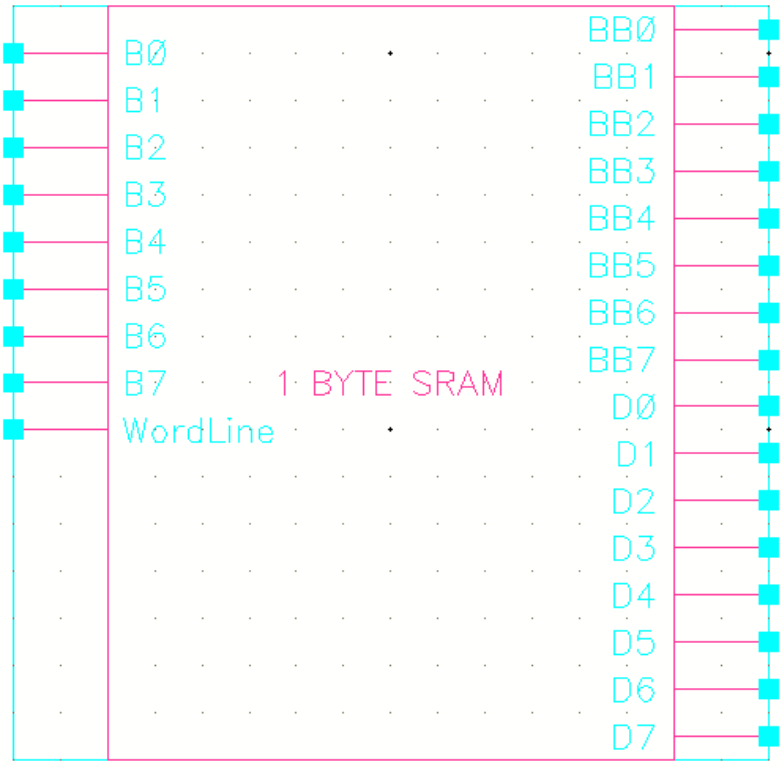


Figure 5.5:- Symbol Representation of 1 BYTE.

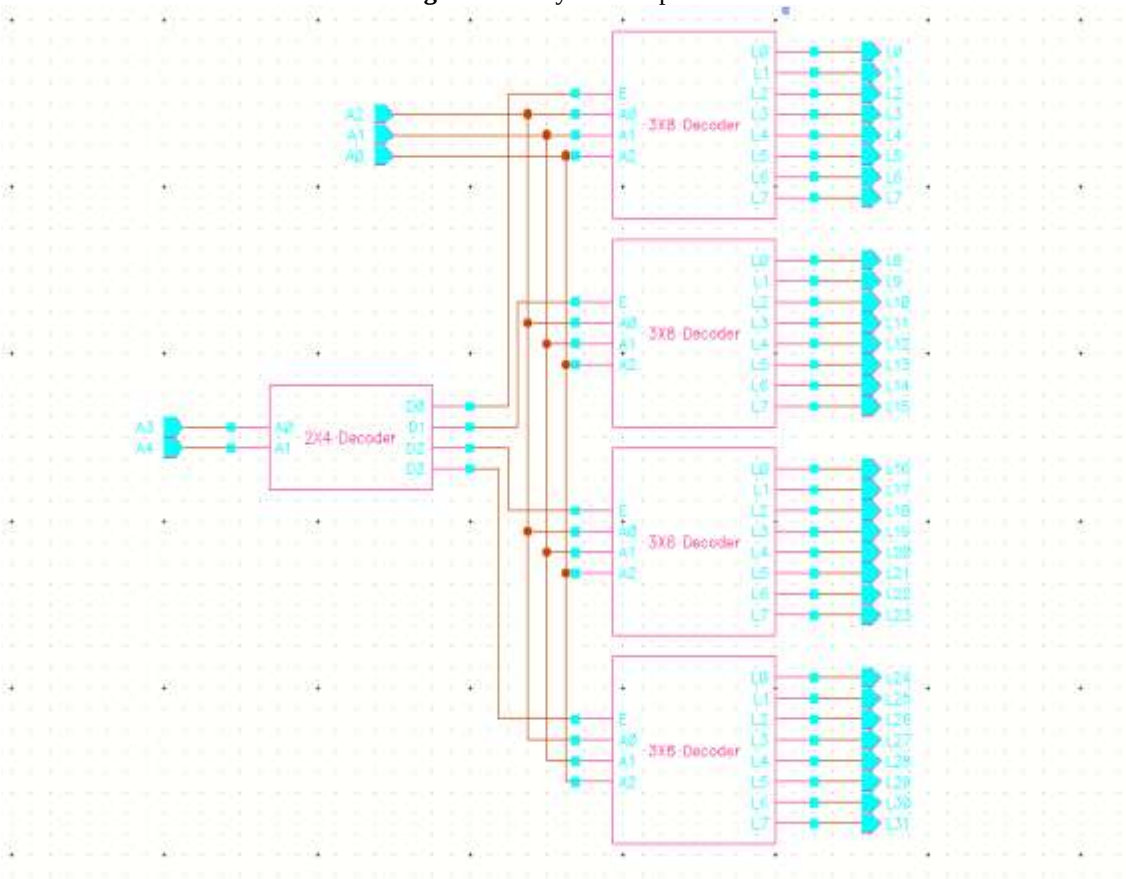


Figure 5.6:- Decoder 5-32.

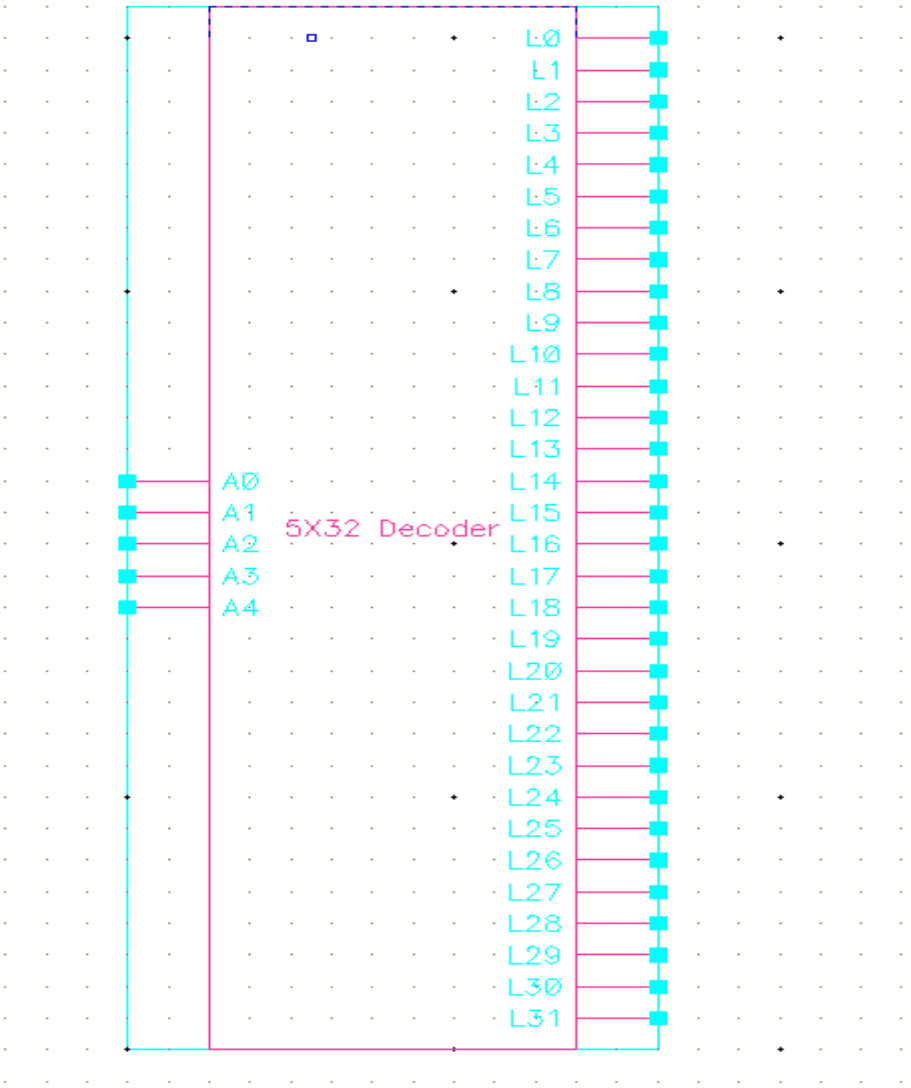


Figure 5.7:- Symbol Representation of Decoder 5-32.

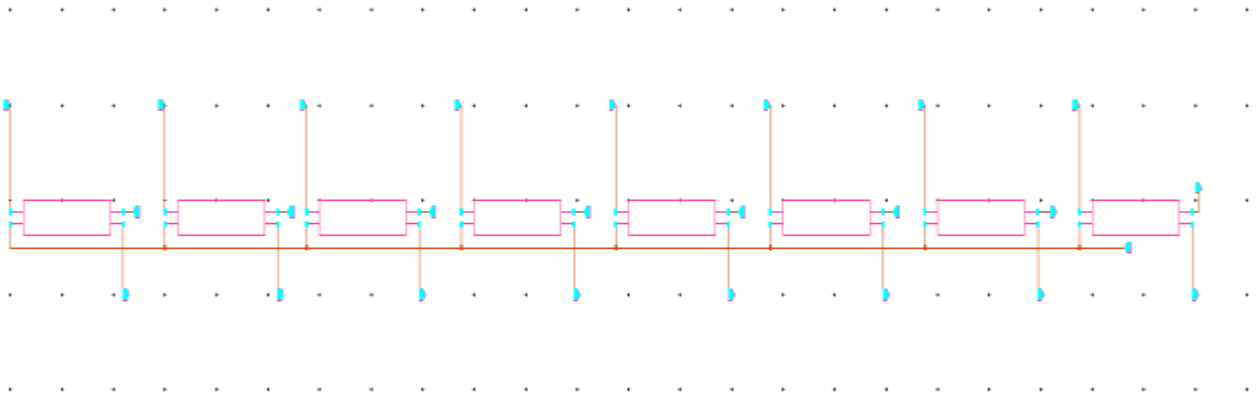


Figure 5.8:- 8 BITES=1BYTE 6T SRAM Representation.

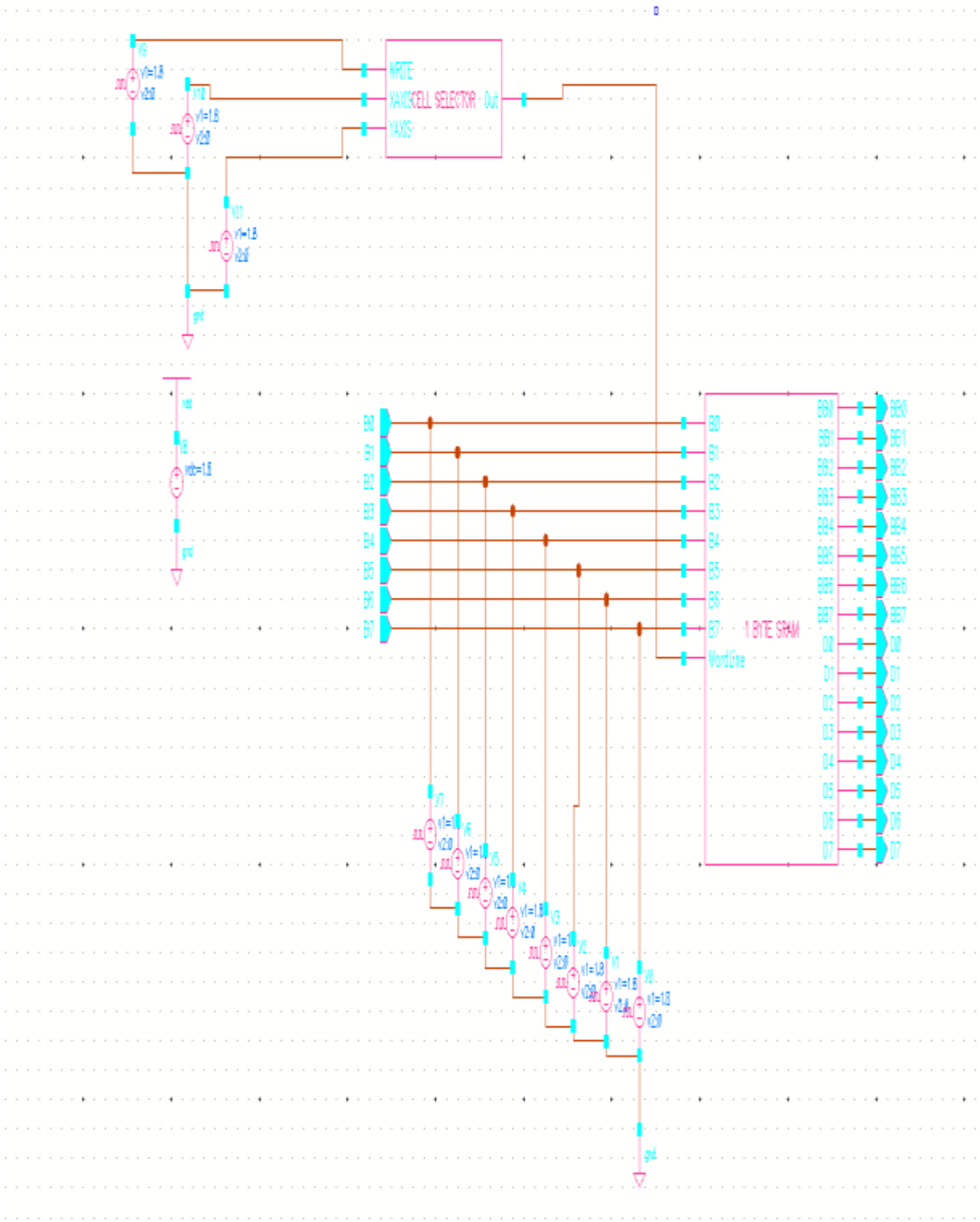


Figure 5.9:- Schematic Representation of 6T 1 Byte SRAM.

Conclusion& Future Scope:-

In this we structured 2 Bytesmemory utilizing memory banking technique which gives better execution contrasted with solid design. The SRAM is isolated in 2 parts.For example, peruse information way and another is push decoder way. The format of complete plan is drawn in an advanced way, with the end goal that we can accomplish

least deferral in over two parts. Post Format reenactments are finished and researched the power examination of complete structure.

At first single 6T SRAM cell is planned which works at a recurrence of 8GHz and PVT examination for the 6T cell is performed in light of the fact that the structure of SRAM cell is the core of entirety structure. Dependability examination for single 6T SRAM is performed and structured 6T cell with static clamor edge, Read Noise Margin and Write Noise Margin of 240mV,115mV and 425mV separately for an inventory voltage of 1V. The Layout of single cell is attracted a symmetric way, to such an extent that contacts of one cell are imparted to contacts of another cell while making a cell column and cell exhibit. Subsequently format territory of cell cluster is limited which results decrease in the power dissemination of circuit.

All peripherals like pre-charge, push decoder, word line driver, segment multiplexer, compose driver and sense speaker are planned .The designs of every above fringe are drawn in an improved way and individual recreations of all plans are performed. The Recurrence of memory is influenced with number of lines and segments for example recurrence of activity is partitioned by a factor of two as number of columns pairs and also recurrence is decreased by a factor of four when number of segments copies, thus memory banking strategy is utilized in the structure of 1Kb to accomplish better recurrence of activity.

To perform the write operation in the SRAM cell to flip the data value , nearly full voltage swings is required on three bit line. This full voltage swing on the capacitive bit lines will continue a great amount of power according to law of CV^2f .this voltage swing. Reduction is an effective way to decrease the power dissipation. the current mode sensing technique isalso proposed method the layout and simulation is done for the one bit pair for free different methodologies. The bit line interference of selection cell with adjacent selected and non-selected cell is also checked out.

The dynamic power of SRAM is mainly due to charging and discharging of highly capacitive lines. In view of all these ,the future course of action involves effective reduction of leakage in an SRAM cell. It is proposed here that appropriate leakage reduction techniques would be developed with an emphasis on the reduction of gate leakage .Leakage reduction in SRAM is also possible using self-controllable switch either at the upper end of of cell to reduction supply voltage (USR scheme) or at the lower end of the cell to raise the potential of the ground node (LPR scheme).This method would also be tested for its efficiency when this work is advance.

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