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RESEARCH ARTICLE

DESIGN AND SIMULATION OF CASCADED H-BRIDGE MULTILEVEL INVERTER WITH STATCOM FOR INDUSTRIAL APPLICATIONS.

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Abstract

This paper presents an investigation in power system for compensation of reactive power and harmonics of 13-level cascaded H-bridge (CHB) inverter. Due to their many advantages in terms of low power dissipation on power supplies, low harmonic contents, the topologies of multilevel inverters are being used in medium and high power applications such as an active power filter, FACTS devices and a machine current. To control the multilevel inverter, the selected switching techniques play an important role on elimination of harmonic distortion in generated output voltage. We can use 's' dc sources for 2s+1 level for calculating the number of levels. This model is used to calculate the instantaneous reactive power and design a control scheme using abc coordinates for reactive power compensation. The simulation result of MATLAB/Simulink software indicates the superior performance of the proposed control system as well as the precision of the proposed models.

Introduction:-

The concept of multilevel inverters has been introduced since 1975 [1]. The term multilevel began with the three level inverters. Subsequently, several multilevel inverter topologies have been developed. To achieve higher power the concept of a multilevel inverter is used in series of power semiconductor switches with several lower voltages dc sources to perform the power conversion by synthesizing a staircase voltage waveform [8]. Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. Today, it is very difficult to connect a single power semiconductor switch directly to medium voltage grid (2.3, 3.3, 4.16 or 6.9KV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. It is troublesome to connect only one power semiconductor switch directly for a medium voltage grid. As a result a multilevel power inverter structure has been introduced as an alternative in high power and medium voltage situations and it is also enable for renewable energy sources. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. As the number of levels increases in an inverter, which produces a staircase wave that approaches a desired waveform as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels increases. As the number of levels increases, the voltage that can be spanned by remaining multiple voltage levels also increases.

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Multilevel Inverter Topologies:-

Diode Clamped Multilevel Inverter:-

Nabae, Takahashi and Akagi in 1981 introduced a 3-level diode-clamped inverter also called the neutral clamped inverter [1]. In the 1990's several researchers published articles that have reported results for 4, 5 and 6-level diode clamped inverters. After reading [1]-[6], we conclude that a set of two switches is on at any given time for a 1-Φ three-level diode clamped inverter. This type of inverter is suitable on an AC transmission line for transmission of DC current or variable speed motors.

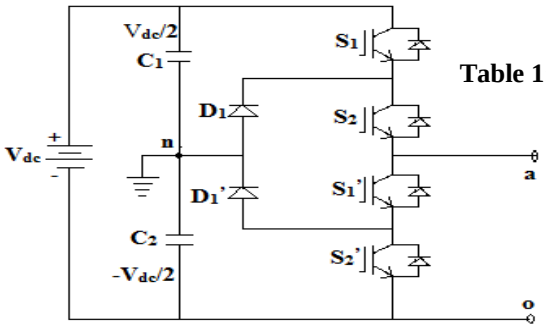


Table 1:- Switching pattern for 3-level Diode-Clamped inverters

Sequence of Switches (ON)	Load Voltage
S_1, S_2	$+V_{dc}/2$
S_1', S_2'	$-V_{dc}/2$
S_2, S_1' or S_1, S_2'	Zero

Figure 1:- Three level Diode-clamped Inverter

In Figure 1, the dc output voltage is split into three levels by two bulk capacitors C_1 and C_2 in series form. The middle point of these two capacitors 'n' is called the neutral point. These two diodes D_1 and D_1' clamp the switch voltage to half the level of the dc-bus voltage. When switches S_1 and S_2 turn on, the voltage across $V_{ao}= V_{dc}$. D_1' balances the sharing voltage between S_1' and S_2' with S_1' blocking the voltage across and blocking the voltage across C_1 and S_2' blocking the voltage across C_2. Note that the output voltage V_{ao} is dc and V_{an} is ac. The difference between V_{an} and V_{ao} is the voltage across the capacitor C_2. The circuit becomes a dc/dc converter which has three output voltage levels: V_{dc}, $V_{dc}/2$, and 0 as shown in table 1 when the output is removed out between *a* and 0. The dc bus capacitor is split into two providing a neutral point on the dc side of the inverter. The diodes connected to the neutral point are called the clamping diode.

Flying Capacitors (Capacitor-Clamped) Multilevel Inverter:-

Meynard and Foch introduced a flying capacitor based inverter in 1992 [8]. This inverter structure is similar design to a diode-clamped inverter. The clamping diodes have however been replaced with capacitors. The circuit topology of the flying capacitor multilevel inverter is shown in figure 2. The design requires only two switch combinations to create a voltage output. Tracking the output of all the capacitors is complicated, as is pre-charging all of the capacitors [8].

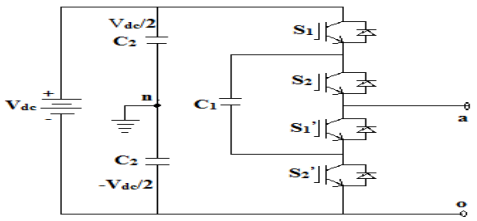


Figure 2:- Three level Capacitor–Clamped Inverter

In Figure 3, the inverter provides a three-level output across *a* and *n*, i.e., $V_{an}= V_{dc}/2$, 0, or $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{dc}/2$, switches S_1' and S_2' need to be turned on; and for the 0 level, either pair (S_1, S_1') or (S_2, S_2') needs to be turned on. When S_1 and S_1' are turned on, clamping capacitor C_1 is charged and when S_2 and S_2' are turned on, it is discharged. The charge of capacitor C_1 can be balanced by proper selection of the zero-level switch combination.

Cascaded H-bridge multilevel inverter:-

In Figure 3, dc power source is connected to an H-bridge inverter. The single inverter has four switches. By using different combinations of switches, the single inverter can produce three different ac voltage outputs, $+V_{dc}$, 0, $-V_{dc}$. In contrast, in this paper, each phase of a cascade multilevel inverter requires 's' dc sources for (2s+1) level in applications that involve real power transfer. For the interest purpose we can use of a single dc power source (e. g. battery, fuel cell) with the remaining (s-1) dc sources being capacitors.

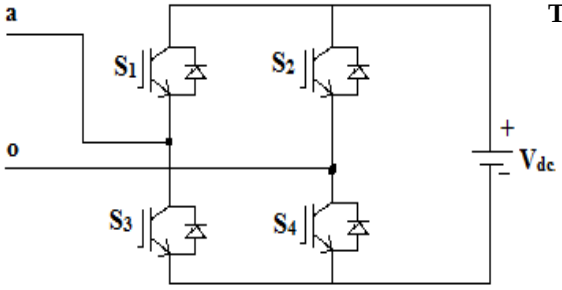


Figure 3:- H-Bridge Inverter

Table 3: Switching Pattern for H-bridge Inverters

Sequence of Switches (ON)	**Load Voltage**
S_1, S_4	$+V_{dc}$
S_2, S_3	$-V_{dc}$
S_1, S_4 or S_2, S_3	Zero

Consider a simple cascade multilevel inverter with three H-bridges:

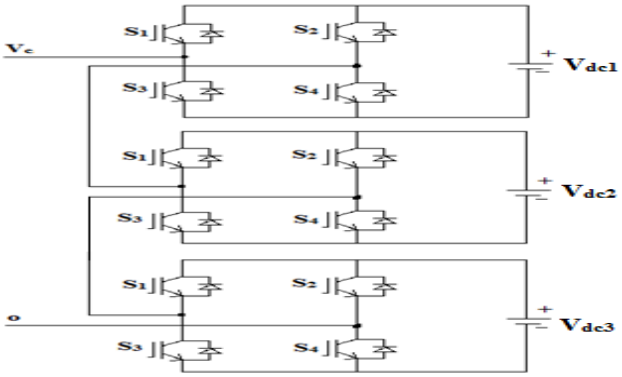


Figure 4:- 7-level Cascaded H-Bridge Inverter

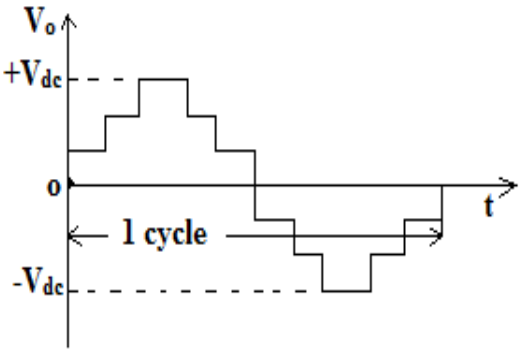


Figure 5:- Output Phase Voltage v/s Time

A three-phase structure of a 7-level CMI with 3 SDCSs is illustrated in Figure 6. Multilevel inverter topology has the minimum components for a given number of levels. Cascaded H-bridge MLI topology is based on the series connection of H-bridges with separate dc sources. The need of several sources on the dc side of the inverter makes multilevel technology attractive for photovoltaic applications. For simplicity of the circuit and advantages, Cascaded H-bridge topology is chosen for the simulation work.

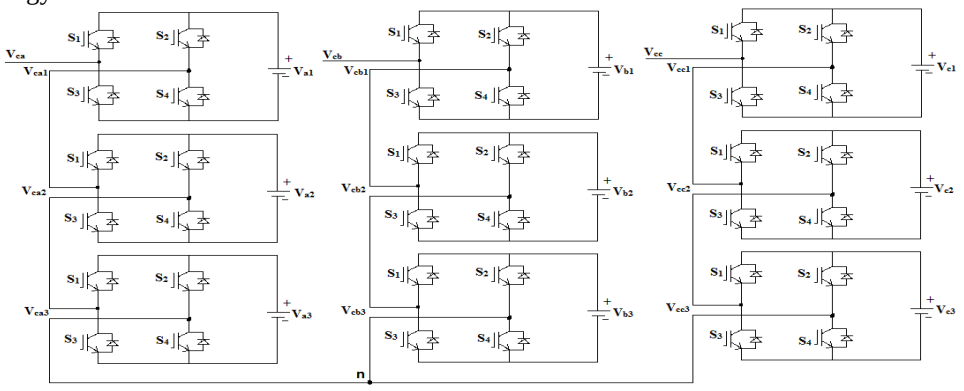


Figure 6:- 3-Φ, 7-level Cascaded H-Bridge Inverter

The phase output voltage is synthesized by the sum of individual inverter outputs, i.e. the phase 'a' voltage for 7-level cascaded inverter is:

$V_{ca}=V_{ca1}+V_{ca2}+V_{ca3}$…… (1)
The phase voltage for m-level cascaded inverter is,
$V_{ca}=V_{ca1}+V_{ca2}+V_{ca3}+V_{ca4}+$ …… $+V_{cam}$…… (2)
IGBT/diode has been chosen as the power semiconductor switches in each H-bridge, since it has more features than other power semiconductor switches.

Cascaded 13-level Inverter:-
For 13-level cascaded H-bridge inverters, it will have 6 SDCSs per leg; this means that six H-bridge inverters are used for 1-Φ structure.

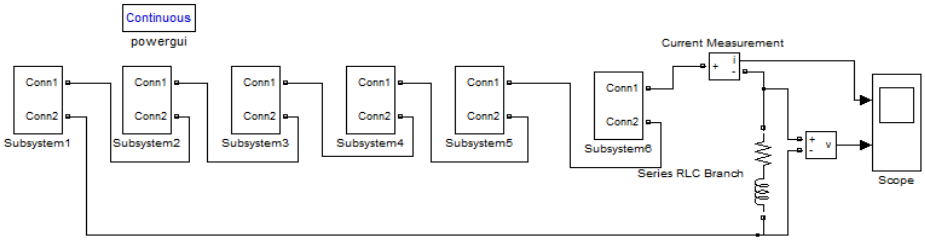


Figure 7:- 1- Φ, 13-level cascaded inverter (Simulation circuit)

One of the terminal of each single phase 13-levels cascaded H-bridge multilevel is connected as star, while the other terminal of each single phase cascaded H-bridge multilevel inverter is connected to a 3- Φ series load [9]. This type of cascaded H-bridge multilevel inverter has been designed and simulated using MATLAB SimpowerSystems. A 3-Φ cascaded 13-level cascaded multilevel inverter circuit shown in figure 8 has been developed and tested.

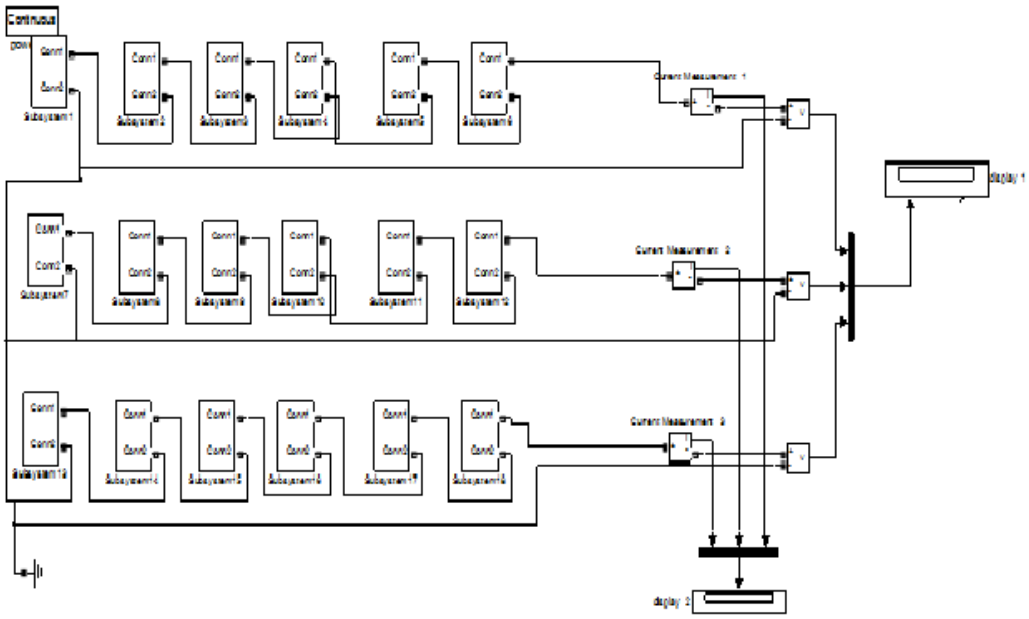


Figure 8:- 3- Φ, 13-level cascaded inverter (Simulation circuit)

The output phase voltage is synthesized by the individual sum of inverter output voltage i.e.
Van = V1+V2+V3+.....+Vn ---------- (1)
Therefore, the phase voltage for 13-level cascaded inverter is,
Van = V1+V2+V3+V4+V5+V6 ---------- (2)
The magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows:
$H(n)=\frac{4}{\pi n}\sum_{n=1}^{\infty}[\cos(n\theta_1)+\cos(n\theta_2)+\cdots+\cos(n\theta_s)]$ ---------- (3)
Where, n = 1, 3, 5, 7… and the conducting anglesθ_1, θ_2…….. θ_s can be chosen such that the voltage total harmonic distortion is a minimum and conducting angles for 13-level inverter is-

$\theta_1 = 0°$ $\theta_2 = 15°$ $\theta_3 = 30°$ $\theta_4 = 45°$ $\theta_5 = 60°$ $\theta_6 = 75°$

Static Synchronous Compensator (STATCOM):-

The STATCOM is the first power-converter-based shunt-connected controller. A representative of converter based VAR compensators is STATCOM. It is a self-commutated AC/DC power converter connected in parallel with the power system through coupling reactors. Figure 11 shows the basic circuit for a Static Synchronous Compensator (STATCOM) and Figure 12 shows its voltage current characteristics. A STATCOM is a voltage source converter (VSC)-based device, with the voltage source behind a reactor. However, its active power capability can be increased if a suitable energy storage device is connected across the dc capacitor. The reactive power at the terminals of the STATCOM depends on the amplitude of the voltage source. If the ac voltage at the point of connection is lower than the VSC terminal voltage, the STATCOM generates reactive current; in other words, when the ac voltage is higher than the amplitude of the voltage source, it absorbs reactive power. The response time of a STATCOM is shorter than that of an SVC, mainly due to the fast switching times provided by the IGBTs of the voltage source converter. The STATCOM also provides better reactive power support at low ac voltages than an SVC, since the reactive power from a STATCOM decreases linearly with the ac voltage.

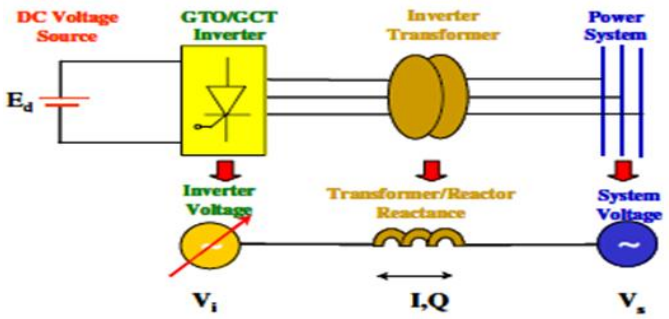


Figure 9:- Static Synchronous Compensator (STATCOM)

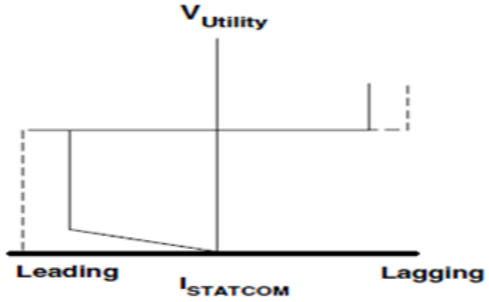


Figure 10:- V-I characteristics of a STATCOM

System Modeling Configuration:-

A. A 13- level, 3-Φ STATCOM based on the cascading configuration is illustrated in Figure 11.

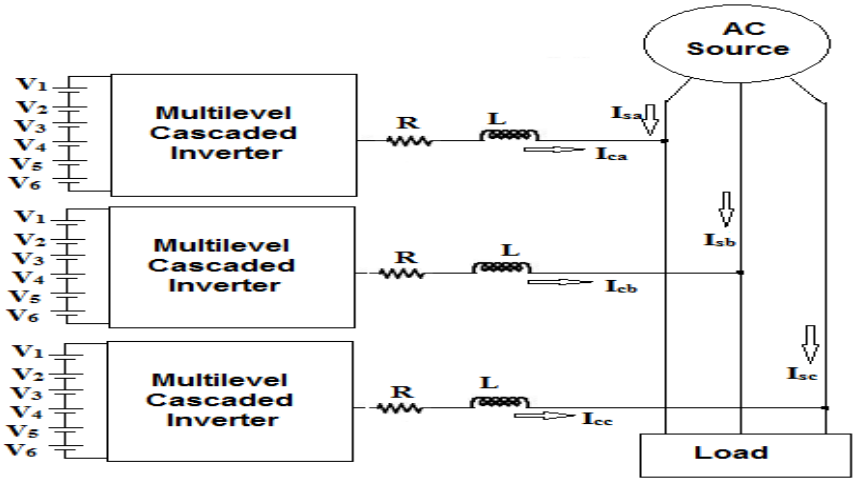


Figure 11: Structure of the STATCOM with Cascade Multilevel Inverter

Figure 11 illustrates the connection diagram for a wye connection 13-level inverter using the cascade voltage source H-bridge inverters. When the ac system voltage is lower than the cascaded inverter output voltage, the reactive current is leading drawn from the system (vars are generated). When the ac system voltage is higher than the cascaded inverter output voltage, the reactive current is leading drawn from the system (vars are absorbed). When the cascaded inverter output voltage is equal to the AC system voltage reactive power exchange is zero. Figure 12 shows a 1-Φ equivalent circuit of the STATCOM, where V_S is the source voltage phasor, V_C is ac output of STATCOM, and L and R represent respectively a set of linked ac reactor and equivalent resistance including

STATCOM losses. The ac voltage controlled STATCOM can control the amplitude of ac voltage by causing a small amount of active power to power flow into or out of the STATCOM. In Figure 12, it is in phase with V_S, so that a small amount of active power flows into SVC, thus the dc capacitor is charged. In the case where V_C leads V_S, a small amount of active power flows out, thus the dc capacitor is discharged as shown in Figure 12. Accordingly, a large amount of reactive power drawn by the STATCOM can be controlled by adjusting the phase angle by the small amount.

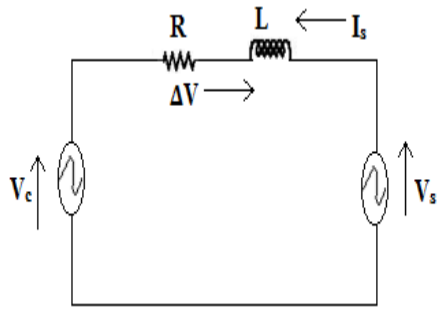
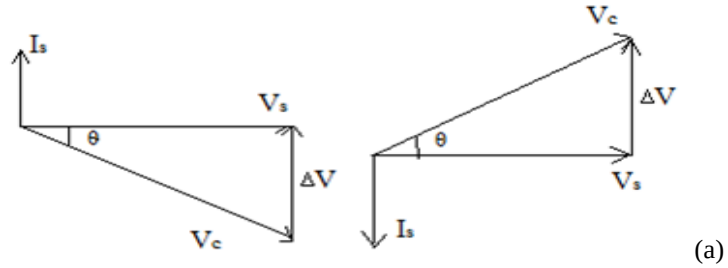


Figure 12: 1-Φ Equivalent Circuit



(a) Leading current (b) Lagging current

Figure 13: Phasor Diagram of the STATCOM

B. System Modeling

From figure 10, the ideal three phase power supply is given by-

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \sqrt{\frac{2}{3}} V_{sl} \begin{bmatrix} \sin(wt) \\ \sin(wt - 2\pi/3) \\ \sin(wt + 2\pi/3) \end{bmatrix} \text{ ---------- (4)}$$

Where, the Vsl and w denote the rms line to line voltage and frequency of source voltage. Using the figure 12, one obtains the following equation.

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \left(R + L\frac{d}{dt}\right) \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} + \begin{bmatrix} V_{ca} \\ V_{cb} \\ V_{cc} \end{bmatrix} \text{ ---------- (5)}$$

Under the assumption that harmonic components generated by switching pattern are negligible, the switching function S can be defined as follows:

$$S = \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} = \sqrt{\frac{2}{3}} M \begin{bmatrix} \cos(wt+\propto) & \cos\left(\text{wt}+\propto -\frac{2}{3}\pi\right) & cos\left(wt+\propto +\frac{2}{3}\pi\right) \\ \sin(wt+\propto) & sin\left(wt+\propto -\frac{2}{3}\pi\right) & sin\left(wt+\propto +\frac{2}{3}\pi\right) \\ \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} \end{bmatrix} \text{-------- (6)}$$

Where $\propto$ is the phase angle which relates the phase difference between output voltage of source voltage and cascade multilevel inverter.

Now, the output voltage of the cascade multilevel inverter and capacitor dc current can be expressed as follows:

$V_{c,abc} = S \times 3V_{dc}$ ---------- (7)

$i_{dc} = S^T i_{abc}$ ---------- (8)

Where, when the capacitance of the HBI module is same as C, the total capacitance is C/5 for 13-level because one is dc source.

Capacitor DC current is given by:

$i_{dc} = \frac{C}{5}\frac{d5V_{dc}}{dt} = C\frac{dV_{dc}}{dt}$ ---------- (9)

C. Control of reactive power-

It is well known that the amount and type of reactive power for inductive and capacitive load exchange between the STATCOM and the system can be adjusted by controlling the magnitude of STATCOM output voltage with respect to that of system voltage. The reactive power supplied by the STATCOM is given by equation (10),

$Q = V_{statcom} - V_s$ ---------- (10)

Where, $V_{statcom}$ and V_s are the magnitudes of STATCOM output voltage and system voltage respectively and X is the equivalent reactance between STATCOM and the system. When reactive power Q is positive, the STATCOM supplies reactive power to the system. Otherwise, the STATCOM absorbs reactive power from the system.

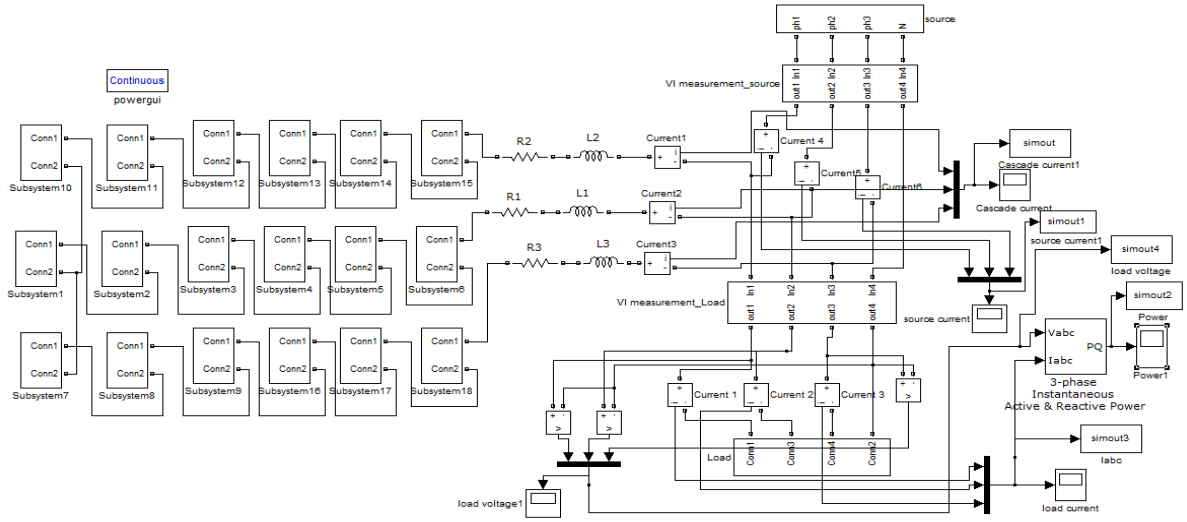


Figure 14:- Simulated circuit of the STATCOM with 13-level cascaded multilevel inverter

Simulation Results:-

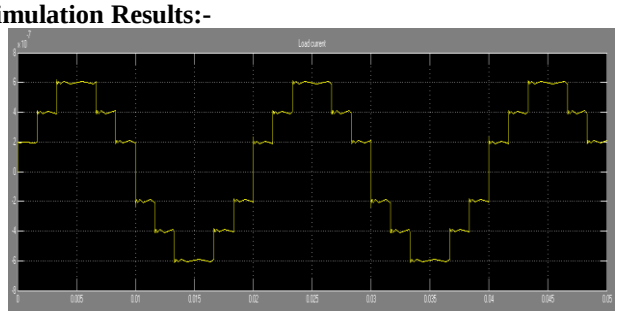


Figure 15:- Output Current Waveform of 1-Φ, 7-level CMI v/s time

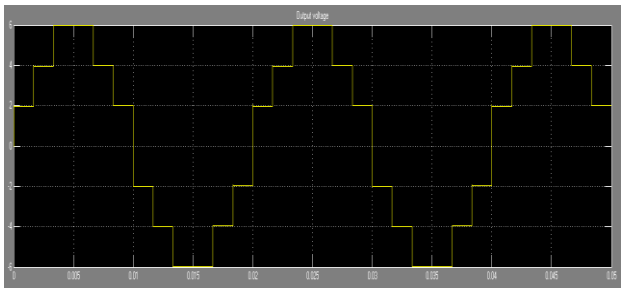


Figure 16:- Output Voltage Waveform of 1-Φ, 7-level CMI v/s time

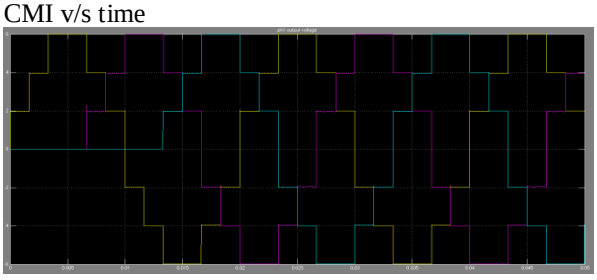


Figure 17:- Output Phase Voltage Waveforms of 7-level CMI v/s time

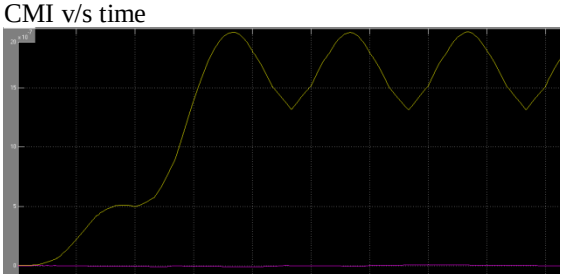


Figure 18:- Active and Reactive Power Measurement for 7-level CMI v/s time

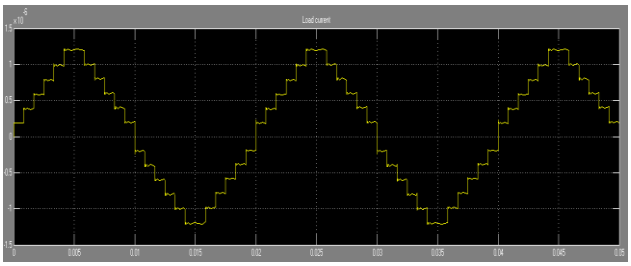


Figure 19:- Output Current Waveform of 1-Φ, 13-level CMI v/s time

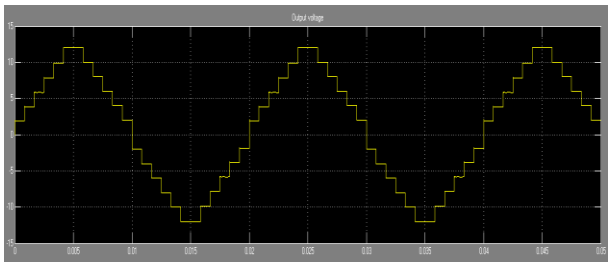


Figure 20:- Output Voltage Waveform of 1-Φ, 13-level CMI v/s time

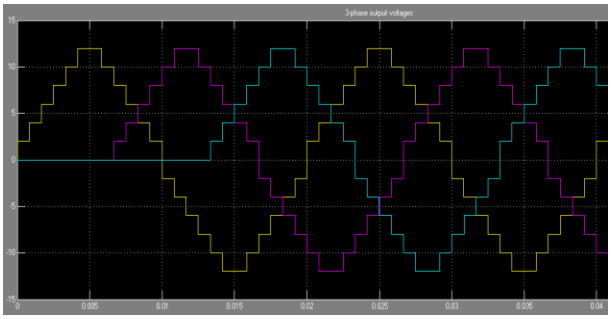


Figure 21:- Simulated 3-phase Output voltage waveforms of 13-level cascaded inverter with separate DC sources

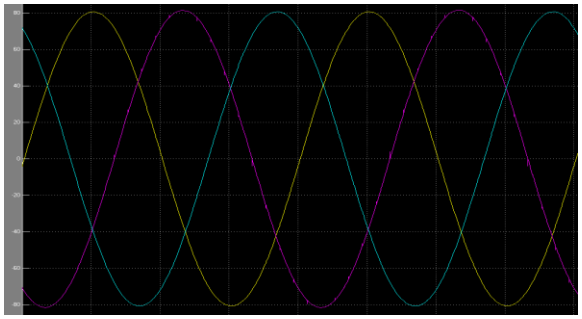


Figure 22:- 3-Φ ac supply voltage in STATCOM v/s time

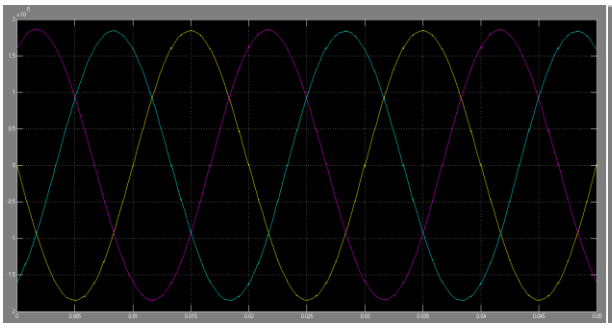


Figure 23:- Cascade Current in STATCCOM v/s time

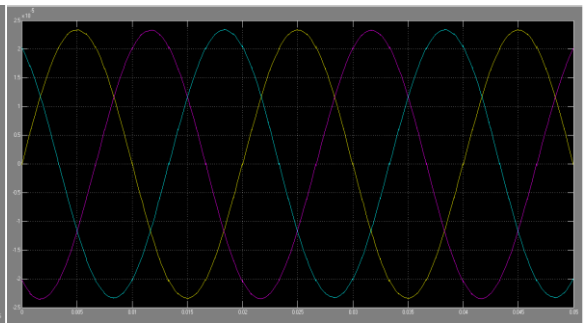


Figure 24:- 3-Φ ac source current in STATCOM v/s time

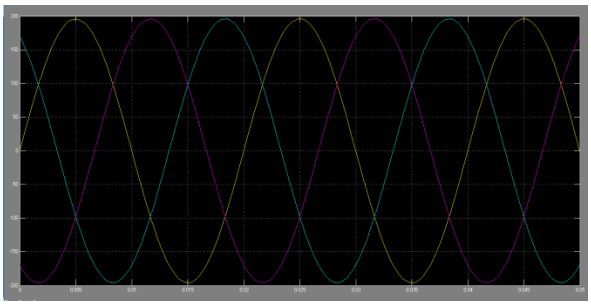


Figure 25: 3-Φ load output measured voltage v/s time

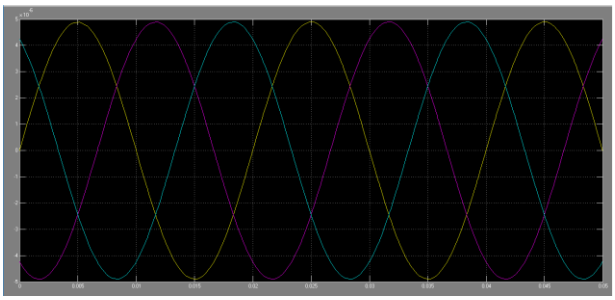


Figure 26: 3-Φ load output measured current v/s time

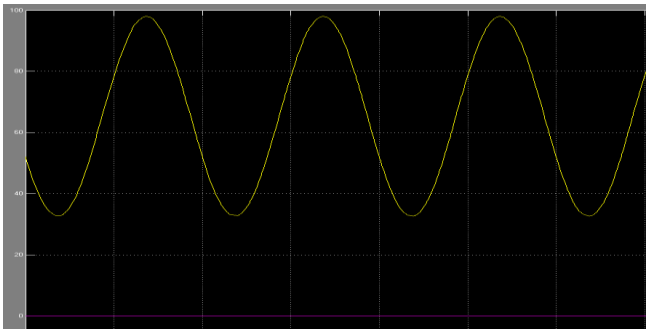


Figure 27: Reactive power in 3-phase cascaded 11-level inverter based STATCOM

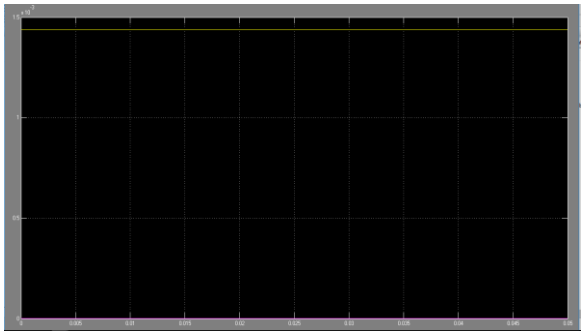


Figure 28: Active and Reactive power in 3-Φ cascaded 13-level inverter based STATCOM

Conclusion and Future Work:-

In conclusion, among the topologies of multilevel inverter, the cascaded-multilevel VSC is the most promising alternative for the FACTs applications. It requires the least number of components to achieve the same number of output voltage levels. The Cascaded multilevel inverter can flexibly expand the output power capability and is favorable to manufacturing with its modularized structure. Control complexity of the Cascaded Multilevel Inverter is, however, directly proportional to the number of H-bridge inverters. As the number of voltage levels increases, the voltage-imbalance problem becomes more of a concern. The simulation of the STATCOM with 13-level cascaded inverter is performed in the Simulink environment and the results are presented. In future, sliding mode control (SMC) can be used as a controller in STATCOM based cascaded multilevel inverter.

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