ISSN NO. 2320-5407

Journal homepage: http://www.journalijar.com

INTERNATIONAL JOURNAL OF ADVANCED RESEARCH

RESEARCH ARTICLE

Asynchronous Data Sampling in Double Edge Triggered Flip-flops with Clock Gating

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Manuscript Info

Manuscript History:

Received: 19 August 2015
Final Accepted: 22 September 2015
Published Online: October 2015

Key words:

Asynchronous Sampling, Clock Gating, Flip-flops

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Abstract

For synchronous designs, a large portion of the total power consumption of integrated circuits is mainly due to the storage elements and clock distribution. Normally storage element will be flip-flops. In low power circuit design, clock elements play an important role in energy efficiency. One technique to reduce power consumption is to use double edge triggered flip-flops which provides the same throughput as the single edge triggered flip-flop while only using half of the clock frequency. Another technique to reduce power consumption is clock gating. However incorporating clock gating with double edge triggered flip-flops to further reduce power consumption introduces asynchronous data sampling which means that the output changes between the clock edges. Along with asynchronous data sampling, a method to avoid the same is designed. These circuits are designed in 180nm CMOS technology and simulated using Cadence Virtuoso software.

INTRODUCTION

Flip-flops are widely used in finite state machine controllers and also as storage elements. Flip-flops are designed as basic element and it provides great benefits for integrated circuits. In single edge triggered flip-flops, half of the clock edges remain inactive. Double edge triggered flip-flops can utilize these idle edges also. Therefore double edge triggered flip-flops can double the throughput or maintain the throughput while operating at half of the clock frequency as that of the single edge triggered flip-flops. Double edge triggered flip-flops can be classified into two types such as Latch-Mux and Pulsed Latches. The Latch-Mux consists of two latches in parallel. In which each of them is transparent on opposite levels of the clock. In the Pulsed Latches type, the pulse generator responds on both edges and it causes the latch to sample an input for each clock edge. Power-reducing techniques have been added to double edge triggered flip-flops in order to save the power dissipation. Clock-gating is one of the major techniques to reduce power dissipation. For a large digital system, clock-gating technique is used to reduce the power consumed on idle circuitry. To further reduce the power consumption, one can couple the clock-gating technique with double edge triggered flip-flops. However, the combination of clock-gating and double edge-triggered techniques can create an asynchronous sampling under certain circumstances which causes output to change in-between the clock edges. In a clock-gated system, the internal clock controls the gated circuits and during the gated periods, the internal clock is separated from the global clock. Two gating circuits are proposed for double edge triggered flip-flops, and these circuits are evaluated for their effectiveness to address the asynchronous data sampling. Two approaches are designed to filter out the asynchronous data sampling.

Asynchronous Data Sampling

The asynchronous data sampling occurs mainly due to the discontinuity between the global and internal clock. If the internal clock differs from the global clock, then the internal clock event is transmitted immediately when clock gating is discontinued. This section describes the analysis of a design that produces asynchronous data sampling. The transmission gate based double edge triggered flip-flop produces asynchronous data sampling when clock gating is introduced. This flip-flop is built using transmission gates with the Latch-Mux structure (Figure 1).

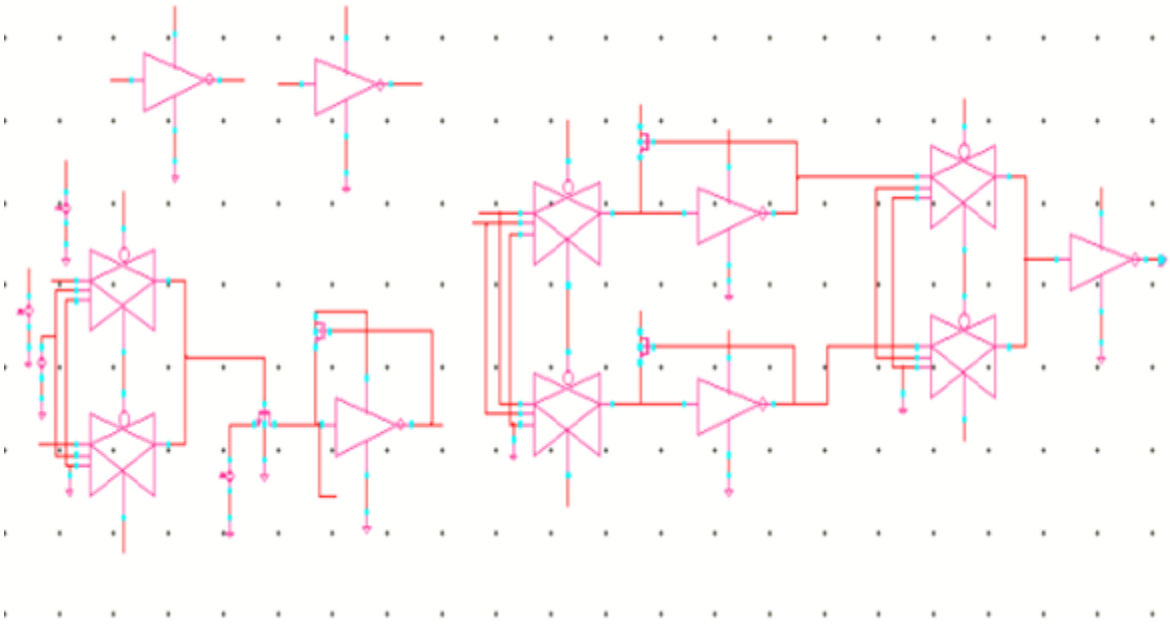

Figure 1: Transmission gate based flip-flop with clock gating

The circuit includes both the clock gating and flip-flop circuitry. The circuit on the left part is the clock gating circuit and that on the right part is the flip-flop circuitry. There are two parallel data paths. The upper path triggers on the rising edges and the lower path triggers on the falling edges of the clock signal. These two data paths monitor the input alternately and provide the output, which means the input is always preloaded into the flip-flop (only one clock edge away from the output). The clock gating part was designed to toggle the internal gating clock whenever the data input changed in order to eliminate power consumption for unneeded transitions. During the gating periods, the internal clock signal preserves the last used value before being gated. This clock gating technique uses the clock signal in a more efficient way that is better suited for double edge triggered flip-flops when compared to other clock gating techniques. If the value of internal clock does not equal the global clock when the circuit deactivates the clock-gating function, then the asynchronous sampling issue appears for the gated double edge triggered flip-flop.

When the front transmission gate is closed inorder to hold the logic level an inverter and a PMOS transistor are used together. When the data signal is high, the inverter switches the signal to low, which will make the PMOS transistor to pull the data up to high. When data signal is low, the inverter switches the signal to high, which will then isolate the data from voltage source and keep the value low. A comparator is implemented by transmission gates, to avoid weak logic generated by pass transistors causing improper circuit operation. When the data signal and the output are equal, the comparator sends out a logic low signal. Then the clock signal is disabled by the NMOS transistor, and

the gated clock stays the same. When the input data signal and output are different, the comparator sends out a logic high signal which keeps the NMOS transistor open, and the clock signal is passed to the flip-flop. As soon as the output changes its value, the clock signal will be disabled again.

The figure 2 shows the simulation result for the transmission gate based double edge triggered flip-flop. The plot includes the clock signal clk, input data signal d, output signal q and the clock gating signal cg.

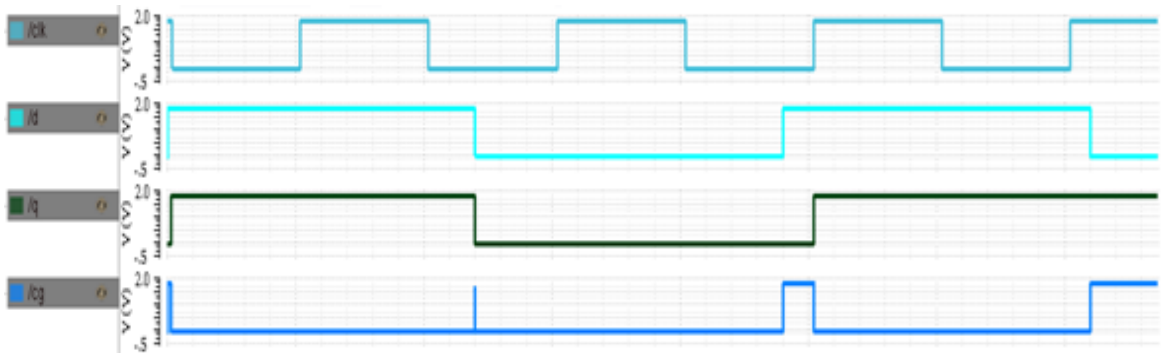

Figure 2: Simulation results for transmission gate based double edge triggered flip-flop

In figure 2 after the second falling edge of the clk, when the input data d changes before the next rising edge the output q is also changing, causing asynchronous sampling that means an unwanted transition occurs at the output.

Method to avoid asynchronous data sampling

There is a method that can avoid asynchronous data sampling. When the gating signal is deasserted, then only resume the connection of global clock to internal clock during when both are equal, which avoids the asynchronous transition in internal clk.

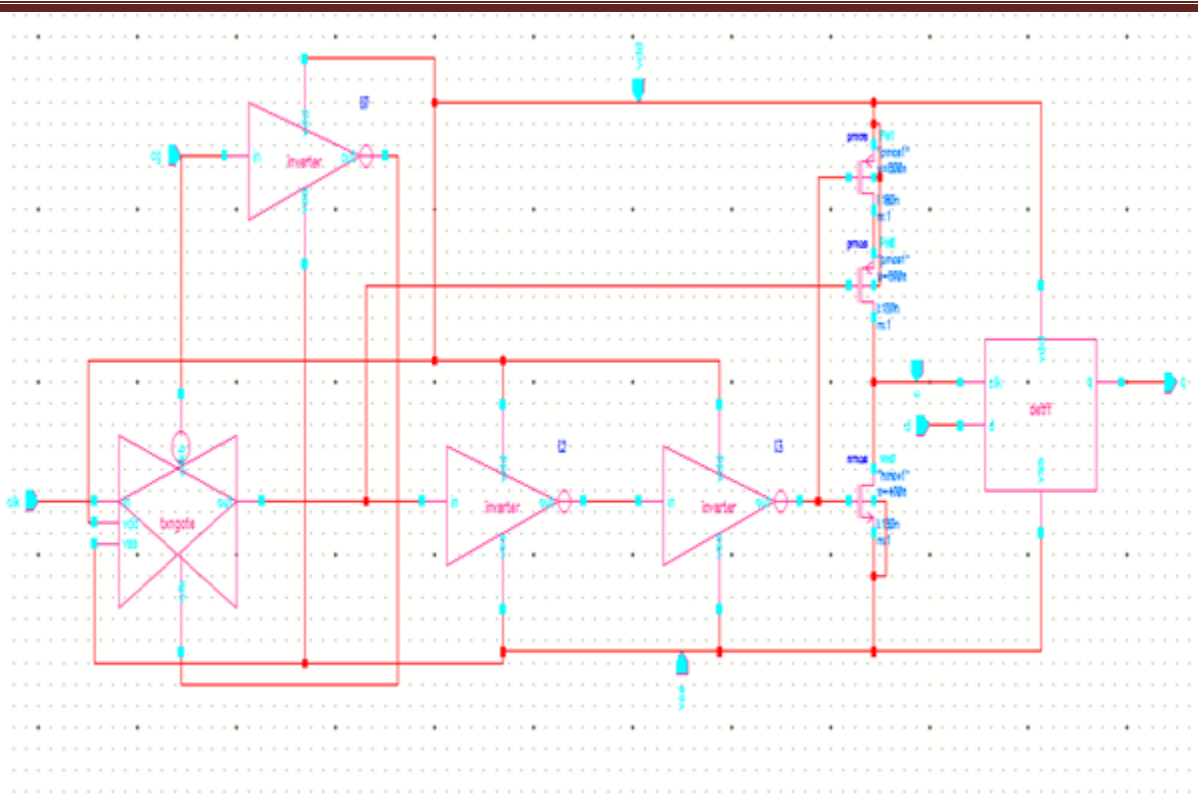

Figure 3: Method to avoid asynchronous data sampling

For the scheme in figure 3 the asynchronous sampling is avoided by the following mechanism. The internal clock signal normally stays at 0. When the data changes while the global clock is 1, PMOS transistor, the one closer to the global clock clk (i.e., directly fed), will be turned OFF immediately, and internal clock will remain the same. When the global clock goes back to 0 (i.e., a falling edge), PMOS transistor closer to the global clock will turn ON, and because of the delay element, other pmos transistor will stay ON for the time needed to trigger the flip-flop. The clock gating signal controls the flow of clock signal. If the clock gating signal is low, then the transmission gate is ON and passes the clock signal. If the clock gating signal is high, then the transmission gate is off and the clock signal will get blocked.

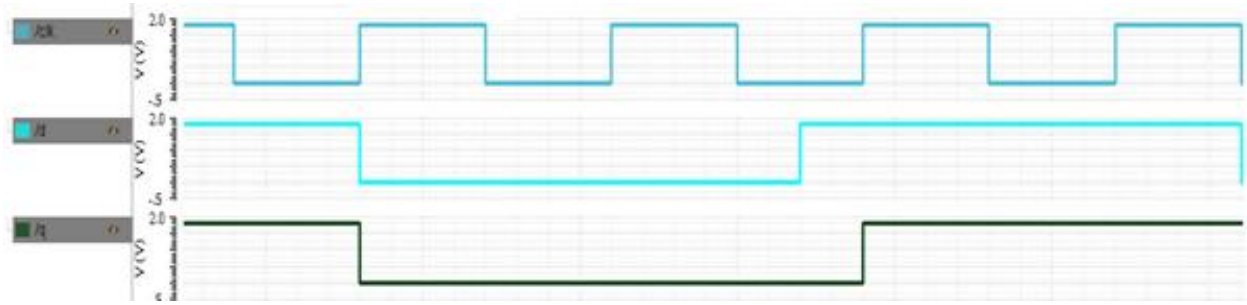

Figure 4: Simulation result for the method to avoid asynchronous data sampling

The simulation result for the method to avoid asynchronous data sampling is shown in figure 4. In figure 4.12 clk is the clock signal. Correspondingly d and q are input and output data. In the waveforms it can be seen that the input data has a low to high transition after the third falling edge and before the next rising edge. But the output data has this transition only at the next rising edge, thus avoiding asynchronous data sampling.

Conclusion

The double edge triggered flip-flops and clock gating are two methods to reduce dynamic power consumption, and both of these circuits are successful when they are used separately. However, when clock gating is applied into a double edge triggered flip-flop, a data transition error may appear at the output between clock edges due to asynchronous data sampling. The asynchronous data sampling is a general and universal potential error condition which is associated with the clock-gated double edge triggered flip-flop. The main reason for the occurrence of the asynchronous data transition is the uncertainty of the clock value when the clock-gating signal is deasserted. An asynchronous data transition will occur if the global clock value is not in phase with the internal clock (i.e., the effective clock for the flip-flop), then the internal clock will change immediately. A solution to asynchronous data sampling is also provided in this paper.

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